datasheet

PRODUCT SPECIFICATION

1/2" color CMOS 64 megapixel (9248 x 6944) image sensor
with PureCel®Plus-S technology

OV64B40

color CMOS 64 megapixel (9248 x 6944) image sensor with PureCel®Plus-S technology

datasheet (COB)
PRODUCT SPECIFICATION

version 2.11
november 2020

To learn more about OmniVision Technologies, visit www.ovt.com.

applications

- smart phones
- video conferencing
- PC multimedia

ordering information

- **OV64B40-GA5A-002A** (color, chip probing, 150 µm backgrinding, reconstructed wafer with good die)

features

- automatic black level calibration (ABLC)
- programmable controls for frame rate, mirror and flip, binning, cropping, and windowing
- support for dynamic DPC
- supports output formats: 10-bit RGB 4C non-HDR and 10-bit RGB Bayer non-HDR
- supports horizontal and vertical subsampling
- supports typical images sizes: 9248x6944, 7680x4320, 4624x4320, 3840x2160, 1920x1080, and 1280x720
- standard serial SCCB interface
- up to 4-lane MIPI TX interface with speed up to 3.0 Gbps/lane
- 2/3 trio C-PHY interface, up to 2.45 Gsps/trio
- supports type 2 2x2 ML PDAF
- 4-cell support:
  - 4-cell binning
  - 4-cell full
- HDR support:
  - stagger HDR 2/3 exposure timing
- on-chip 4-cell to Bayer converter
- three on-chip phase lock loops (PLLs)
- programmable I/O drive capability
- built-in temperature sensor
- 0.702 µm pixel

key specifications (typical)

- **active array size:** 9248x6944
- **power supply:**
  - core: 1.1V
  - analog: 2.8V
  - I/O: 1.8V
- **power requirements:**
  - active: 647 mW (64 MP @ 15 fps)
  - XSHUTDOWN: <10 µA
- **temperature range:**
  - operating: -30°C to 85°C junction temperature (see **table 7-2**)
  - stable image: 0°C to 60°C junction temperature (see **table 7-2**)
- **output formats:** 10-bit RGB RAW
- **input clock frequency:** 6~27 MHz
- **lens size:** 1/2"
- **lens chief ray angle:** 34.55° non-linear (see **table 9-3**)
- **maximum image transfer rate:**
  - 9248x6944: 15 fps (see **table 2-1**)
- **maximum exposure:** VTS - 24 for full resolution, VTS - 12 for downsample mode
- **minimum exposure:** 8 for full resolution or 4 for downsample mode
- **sensitivity:** 1550 e⁻/Lux-sec (1C), 6200 e⁻/Lux-sec (4C)
- **max S/N ratio:** 34.64 dB (1C), 39.06 dB (4C)
- **dynamic range:** 71.48 dB (1C), 77.13 dB (4C)
- **scan mode:** progressive
- **pixel size:** 0.702 µm x 0.702 µm
- **image area:** 6514.56 µm x 4897.152 µm
- **die dimensions:** 7689.6 µm x 5538.6 µm (COB), 7739.6 µm x 5588.6 µm (RW) (see **section 8**)

note Pixel performance and power consumption shown are target values. These values are subject to change based on real measurements.

note COB refers to whole wafers with known good die and RW refers to singulated good die on a reconstructed wafer. Die size differs between COB and RW.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV64B40 image sensor. The die information is shown in **section 8**.

figure 1-1 pad diagram

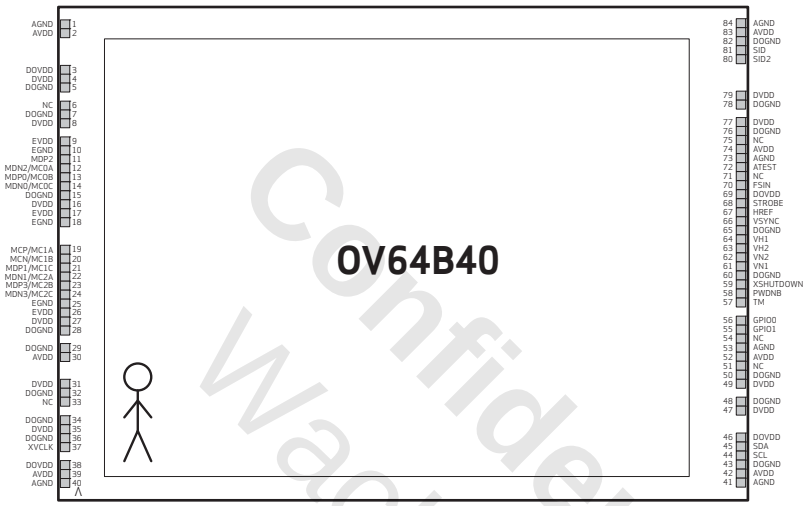


table 1-1 signal descriptions (sheet 1 of 4)

pad number	signal name	pad type	description
1	AGND	ground	analog ground
2	AVDD	power	analog power
3	DOVDD	power	I/O power
4	DVDD	power	digital circuit power
5	DOGND	ground	I/O ground
6	NC	–	no connect
7	DOGND	ground	I/O ground
8	DVDD	power	digital circuit power
9	EVDD	power	MIPI digital circuit power
10	EGND	ground	MIPI ground
11	**MDP2**	output	MIPI data positive output
12	**MDN2/MC0A**	output	MIPI data negative output

table 1-1 signal descriptions (sheet 2 of 4)

pad number	signal name	pad type	description
13	**MDP0/MC0B**	output	MIPI data positive output
14	**MDN0/MC0C**	output	MIPI data negative output
15	DOGND	ground	I/O ground
16	DVDD	power	digital circuit power
17	EVDD	power	MIPI digital circuit power
18	EGND	ground	MIPI ground
19	**MCP/MC1A**	output	MIPI clock positive output
20	**MCN/MC1B**	output	MIPI clock negative output
21	**MDP1/MC1C**	output	MIPI data positive output
22	**MDN1/MC2A**	output	MIPI data negative output
23	**MDP3/MC2B**	output	MIPI data positive output
24	**MDN3/MC2C**	output	MIPI data negative output
25	EGND	ground	MIPI ground
26	EVDD	power	MIPI digital circuit power
27	DVDD	power	digital circuit power
28	DOGND	ground	I/O ground
29	DOGND	ground	I/O ground
30	AVDD	power	analog power
31	DVDD	power	digital circuit power
32	DOGND	ground	I/O ground
33	NC	–	no connect
34	DOGND	ground	I/O ground
35	DVDD	power	digital circuit power
36	DOGND	ground	I/O ground
37	**XVCLK**	input	system clock input
38	DOVDD	power	I/O power
39	AVDD	power	analog power
40	AGND	ground	analog ground
41	AGND	ground	analog ground
42	AVDD	power	analog power

table 1-1 signal descriptions (sheet 3 of 4)

pad number	signal name	pad type	description
43	DOGND	ground	I/O ground
44	**SCL**	input	SCCB interface input clock
45	**SDA**	I/O	SCCB interface data pin
46	DOVDD	power	I/O power
47	DVDD	power	digital circuit power
48	DOGND	ground	I/O ground
49	DVDD	power	digital circuit power
50	DOGND	ground	I/O ground
51	NC	–	no connect
52	AVDD	power	analog power
53	AGND	ground	analog ground
54	NC	–	no connect
55	**GPIO1**	I/O	general purpose I/O
56	**GPIO0**	I/O	general purpose I/O
57	**TM**	input	test mode (active high, input with pull-down resistor)
58	**PWDNB**	input	power down, active low
59	**XSHUTDOWN**	input	reset and power down (active low with pull-down resistor)
60	DOGND	ground	I/O ground
61	VN1	input	reference
62	VN2	input	reference
63	VH2	input	reference
64	VH1	input	reference
65	DOGND	ground	I/O ground
66	**VSYNC**	I/O	video output vertical signal
67	**HREF**	I/O	video output horizontal signal
68	**STROBE**	output	frame exposure output indicator
69	DOVDD	power	I/O power
70	**FSIN**	I/O	frame sync input
71	NC	–	no connect
72	ATEST	output	analog test pin

table 1-1 signal descriptions (sheet 4 of 4)

pad number	signal name	pad type	description
73	AGND	ground	analog ground
74	AVDD	power	analog power
75	NC	–	no connect
76	DOGND	ground	I/O ground
77	DVDD	power	digital circuit power
78	DOGND	ground	I/O ground
79	DVDD	power	digital circuit power
80	SID2	input	secondary SCCB ID select
81	SID	input	primary SCCB ID select
82	DOGND	ground	I/O ground
83	AVDD	power	analog power
84	AGND	ground	analog ground

table 1-2 configuration under various conditions (sheet 1 of 2)

pad number	signal name	RESET[a]	after RESET release[b]	software standby[c]	hardware standby[d]
11	MDP2	high-z	high	high by default (configurable)	high by default (configurable)
12	MDN2/MC0A	high-z	high	high by default (configurable)	high by default (configurable)
13	MDP0/MC0B	high-z	high	high by default (configurable)	high by default (configurable)
14	MDN0/MC0C	high-z	high	high by default (configurable)	high by default (configurable)
19	MCP/MC1A	high-z	high	high by default (configurable)	high by default (configurable)
20	MCN/MC1B	high-z	high	high by default (configurable)	high by default (configurable)
21	MDP1/MC1C	high-z	high	high by default (configurable)	high by default (configurable)
22	MDN1/MC2A	high-z	high	high by default (configurable)	high by default (configurable)

table 1-2 configuration under various conditions (sheet 2 of 2)

pad number	signal name	RESET[a]	after RESET release[b]	software standby[c]	hardware standby[d]
23	MDP3/MC2B	high-z	high	high by default (configurable)	high by default (configurable)
24	MDN3/MC2C	high-z	high	high by default (configurable)	high by default (configurable)
37	XVCLK	high-z	input	input	input
44	SCL	high-z	input	input	high-z
45	SDA	open drain	I/O	I/O	open drain
55	GPIO1	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
56	GPIO0	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
57	TM	input	input	input	input
58	PWDNB	input	input	input	input
59	XSHUTDOWN	input	input	input	input
66	VSYNC	high-z	high	high by default (configurable)	high by default (configurable)
67	HREF	high-z	high	high by default (configurable)	high by default (configurable)
68	STROBE	output zero	output zero by default (configurable)	output zero by default (configurable)	output zero by default (configurable)
70	FSIN	high-z	input	input (configurable)	input (configurable)
80	SID2	input	input	input	input
81	SID	input	input	input	input

a. XSHUTDOWN = 0

b. XSHUTDOWN from 0 to 1

c. sensor set to sleep from streaming mode

d. sensor set to hardware standby from streaming mode by pulling PWDNB = 0

table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

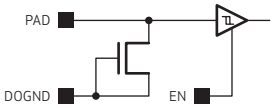
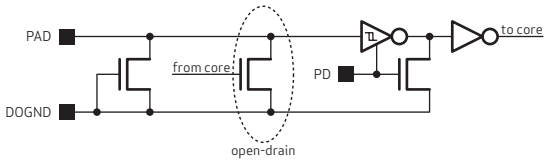
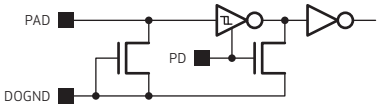
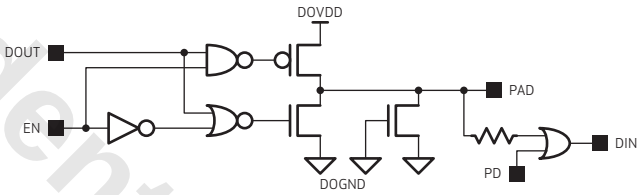
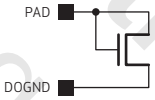
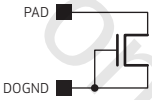
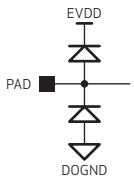
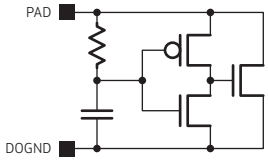
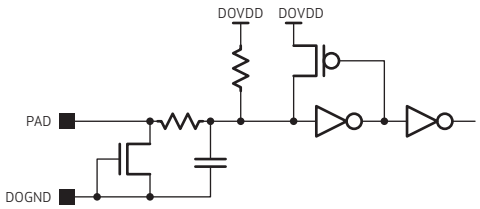
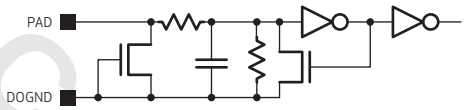
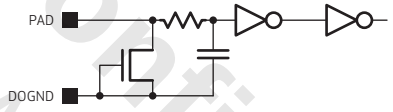
symbol	equivalent circuit
XVCLK	
SDA	
SCL	
VSYNC, STROBE, FSIN, GPIO0, GPIO1, HREF	
VN1, VN2	
VH1, VH2, EGND, AGND, DOGND	
MCN, MCP, MDN[3:0], MDP[3:0]	
AVDD, EVDD, DOVDD, DVDD	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
PWDNB	
XSHUTDOWN, TM	
SID, SID2	

2 system level description

2.1 overview

The OV64B40 color image sensor is a high performance, CMOS, image sensor with a 4-cell color filter, using stacked die technology that delivers 64 megapixels (9248x6944) at 15 fps. It provides options for multiple resolutions while maintaining full field of view. Users can program image resolution, frame rate, and image quality parameters. Camera functions are controlled using the industry standard serial camera control bus (SCCB).

The OV64B40 is capable of delivering 60 fps (30 fps with HDR 2-exposure output), allowing burst photography at 16 megapixel resolution. With a complete 64 megapixel image array, the OV64B40 contains all of the image management functions to ensure high quality imaging solutions for high resolution mobile smart phones.

All required image processing functions are programmable through the SCCB interface. In addition, OmniVision image sensors utilize proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

2.1.1 identifying the sensor's revision ID

For the OV64B40, the sensor's revision ID can be read out from the first few bytes in bank 0 of one-time program (OTP) memory. To read out data from OTP, perform the following steps:

```
6C 0100 01

6C 3D84 00

6C 3D81 01
```

Then, verify that register 0x7001 = 0x64, register 0x7002 = 0x0B, register 0x7003 = 0x04, register 0x7004 = 0x22, and register bits 0x700E[7:6] = 2'b00.

2.2 architecture

The OV64B40 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV64B40 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, precharging and sampling rows of the array sequentially. In the time between precharging and sampling a row, the charge in the pixels decrease with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following the analog processing, the ADC outputs 10-bit data for each pixel in the array.

figure 2-1 OV64B40 block diagram

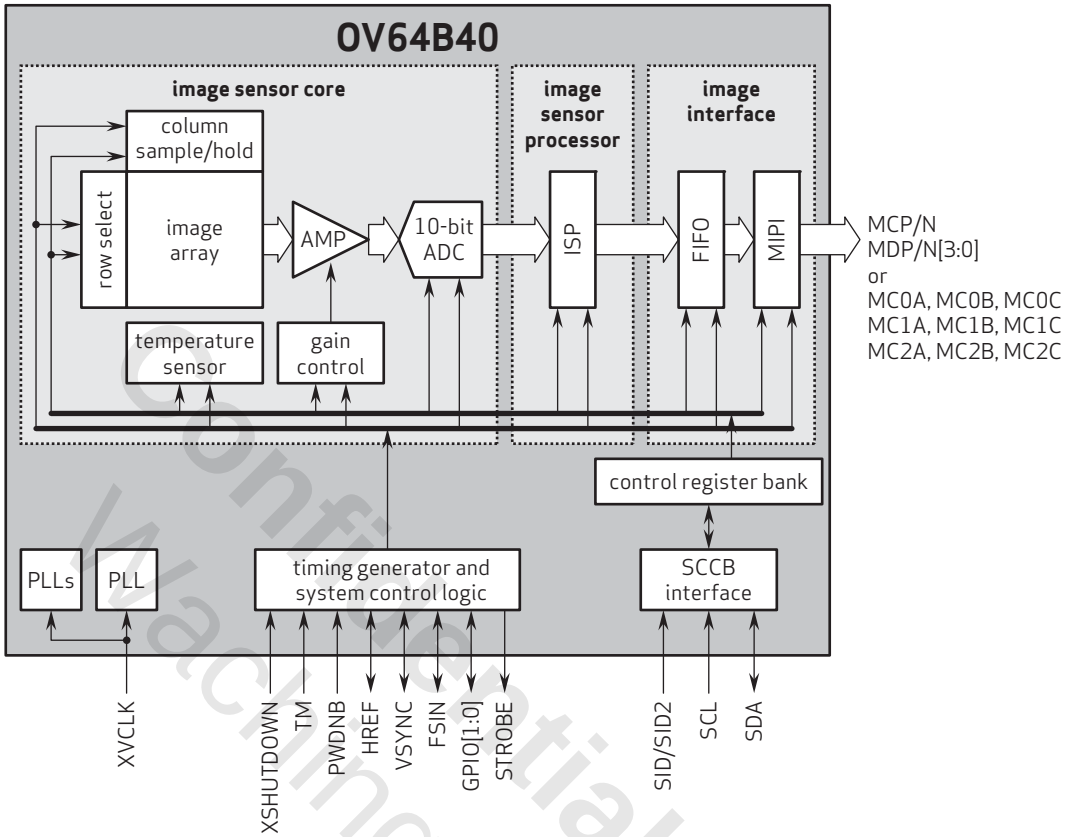
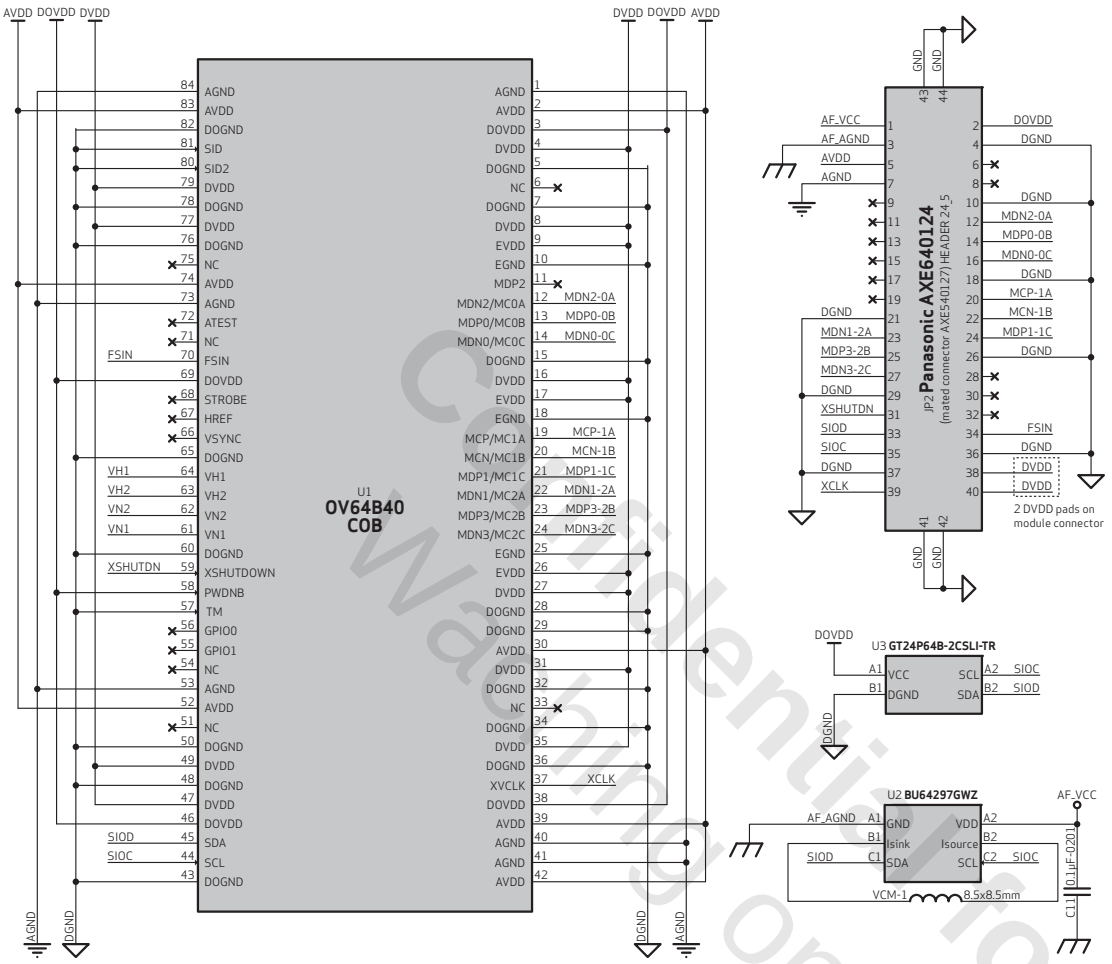


figure 2-2 OV64B40 (C-PHY) reference design schematic



note 1 PWDNB should be pulled high to DOVDD outside of module if unused.

note 2 XSHUTDOWN (XSHUTDN) should be connected to DOVDD outside of module if unused.

note 3 for other pins, such as HREF, FSIN, if unused, can leave floating.

note 4 AVDD is 2.8V (2.7-2.9V) of sensor analog power (clean).

note 5 DOVDD is 1.8 (1.7-1.9V) of sensor digital IO power (clean).

note 6 DVDD is 1.1V (1.05-1.18V) of sensor digital power, needs 2-3 pads on module connector.
DVDD trace width shall be wide enough to avoid big IR drop.

note 7 sensor AGND and DGND should be separated and connected to a single point outside PCB (do not connect inside module).

note 8 capacitors should be close to their related sensor pins.

note 9 EVDD is power supply for MIPI core.
0A&0B&0C, 1A&1B&1C, 2A&2B&2C are MIPI C-PHY trios.
traces of each C-PHY trio should have same or similar length.

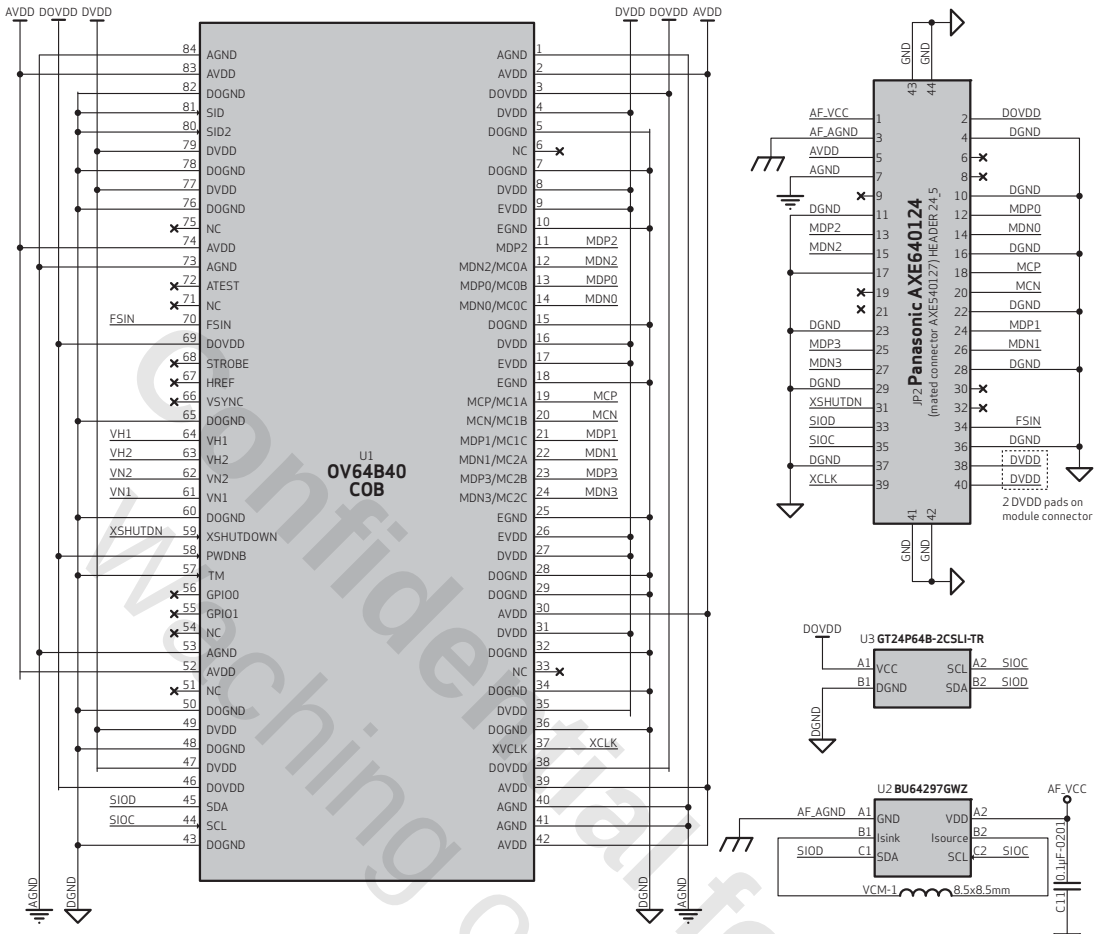
note 10 SID2 and SID are SCCB ID select inputs. SCCB ID is controlled by {SID2, SID} with the following four combinations:
{SID2, SID} = 0/0, SCCB device address = 0x6C
{SID2, SID} = 0/1, SCCB device address = 0x20
{SID2, SID} = 1/0, SCCB device address = 0x44
{SID2, SID} = 1/1, SCCB device address = 0x46

note 11 AF_VCC and AF_AGND is power supply for auto focus related circuitry; although AF_VCC is 2.8-3.3V, it is recommended to use 3.3V for better auto focus performance.

note 12 heat release needs to be considered for module.

note 13 EEPROM slave ID is 0xA4 for write and 0xA5 for read based on current configuration.

figure 2-3 OV64B40 (D-PHY) reference design schematic



note 1 PWDNB should be pulled high to DOVDD outside of module if unused.

note 2 XSHUTDOWN (XSHUTDN) should be connected to DOVDD outside of module if unused.

note 3 for other pins, such as HREF, FSIN, if unused, can leave floating.

note 4 AVDD is 2.8V (2.7-2.9V) of sensor analog power (clean).

note 5 DOVDD is 1.8 (1.7-1.9V) of sensor digital IO power (clean).

note 6 DVDD is 1.1V (1.05-1.18V) of sensor digital power, needs 2-3 pads on module connector.
DVDD trace width shall be wide enough to avoid big IR drop.

note 7 sensor AGND and DGND should be separated and connected to a single point outside PCB (do not connect inside module).

note 8 capacitors should be close to their related sensor pins.

note 9 EVDD is power supply for MIPI core.
MCP and MCN are MIPI clock lane positive and negative outputs.
MDPx and MDNx are MIPI data lane positive and negative outputs.

note 10 traces of MCP, MCN, MDPx, and MDNx should have same or similar length.
differential impedance of clock pair and data pair transmission lines should be controlled at 100 Ohm.

note 11 SID2 and SID are SCCB ID select inputs. SCCB ID is controlled by {SID2, SID} with the following four combinations:
{SID2, SID} = 0/0, SCCB device address = 0x6C
{SID2, SID} = 0/1, SCCB device address = 0x20
{SID2, SID} = 1/0, SCCB device address = 0x44
{SID2, SID} = 1/1, SCCB device address = 0x46

note 12 AF_VCC and AF_AGND is power supply for auto focus related circuitry; although AF_VCC is 2.8-3.3V, it is recommended to use 3.3V for better auto focus performance.

note 13 heat release needs to be considered for module.

note 14 EEPROM slave ID is 0xA4 for write and 0xA5 for read based on current configuration.

2.3 format and frame

The OV64B40 supports RAW RGB and HDR output with one/two/four lane MIPI interface.

table 2-1 format and frame rate

format	resolution	frame rate	methodology	supports PDAF	10-bit MIPI data rate
full (4:3)	9248x6944	15 fps	full 4-cell + remosaic	yes	D-PHY 4-lane x 3 Gbps C-PHY 3-trio x 1.75 Gsps
33 MP (8K 16:9)	7680x4320	30 fps	full 4-cell + remosaic with cropping	yes	D-PHY 4-lane x 3 Gbps C-PHY 3-trio x 1.75 Gsps
16 MP (4:3)	4624x3472	60 fps 30 fps	4C-1 binning 4C-2 binning	no yes	D-PHY 4-lane x 3 Gbps C-PHY 3-trio x 1.75 Gsps
4K2K	3840x2160	120 fps 60 fps	4C-1 binning + cropping 4C-2 binning + cropping	no yes	D-PHY 4-lane x 3 Gbps C-PHY 3-trio x 1.75 Gsps
1080p	1920x1080	240 fps	4C-1 binning + 2x vbin + cropping (RGB)	no	D-PHY 4-lane x 2 Gbps C-PHY 3-trio x 1.2 Gsps
720p	1280x720	480 fps	4C-1 binning + 2x vbin + cropping (RGB)	no	D-PHY 4-lane x 2 Gbps C-PHY 3-trio x 1.2 Gsps

2.4 I/O control

I/O pads on the OV64B40 can be configured as inputs or outputs. The output signals can come either from a data path or registers.

table 2-2 I/O control registers (sheet 1 of 2)

function	register	description
output drive capability control	0x3009	Bit[6:5]: I/O pad drive capability 00: 1x 01: 2x 10: 3x 11: 4x
VSYNC I/O control	0x3002	Bit[7]: Input/output control for VSYNC pad 0: Input 1: Output
VSYNC output select	0x3008	Bit[7]: Output selection for VSYNC pad 0: Normal data path (vertical sync signal) 1: Register control value

table 2-2 I/O control registers (sheet 2 of 2)

function	register	description
VSYNC output value	0x3005	Bit[7]: VSYNC output value
STROBE output select	0x3008	Bit[4]: Output selection for strobe pad 0: Normal data path 1: Register control value
STROBE output value	0x3005	Bit[2]: Strobe output value
HREF I/O control	0x3002	Bit[6]: Input/output control for HREF pad 0: Input 1: Output
HREF output select	0x3008	Bit[6]: Output selection for HREF pad 0: Normal data path (horizontal sync signal) 1: Register control value
HREF output value	0x3005	Bit[6]: HREF output value
FSIN I/O control	0x3002	Bit[3]: Input/output control for FSIN pad 0: Input 1: Output
FSIN output select	0x3008	Bit[3]: Output selection for FSIN pad 0: Normal data path 1: Register control value
FSIN output value	0x3005	Bit[3]: FSIN output value
GPIO0 I/O control	0x3002	Bit[0]: Input/output control for GPIO0 pad 0: Input 1: Output
GPIO0 output select	0x3008	Bit[0]: Output selection for GPIO0 pad 0: Normal data path 1: Register control value (0x3663[6] should also be set to 0)
GPIO0 output value	0x3005	Bit[0]: GPIO0 output value
GPIO1 I/O control	0x3002	Bit[1]: Input/output control for GPIO1 pad 0: Input 1: Output
GPIO1 output select	0x3008	Bit[1]: Output selection for GPIO1 pad 0: Normal data path 1: Register control value
GPIO1 output value	0x3005	Bit[1]: GPIO1 output value

2.5 MIPI interface

The OV64B40 supports one/two/four-lane MIPI transmitter interface and each lane is capable of a data transfer rate of up to 3.0 Gbps.

The OV64B40 supports 2/3 trio C-PHY interface (2.45 Gsps/trio).

2.6 power management

The OV64B40 uses three power supplies: 2.8V AVDD, 1.8V DOVDD, and 1.1V DVDD.

To avoid any glitch from a strong external noise source, OmniVision recommends controlling XSHUTDOWN or PWDNB by GPIO and tying the other pins to DOVDD. OmniVision recommends cutting off all power supplies, including DVDD, when the sensor is not in use.

2.6.1 power up sequence

table 2-3 power up sequences

case	XSHUTDOWN	PWDNB	power up sequence requirement
1	GPIO	DOVDD	Refer to **figure 2-4** XSHUTDOWN rising must occur after AVDD, DOVDD, and DVDD are stable
2	DOVDD	GPIO	Refer to **figure 2-5** PWDNB rising occurs after AVDD, DOVDD, and DVDD are stable

table 2-4 power up sequence timing constraints

constraint	label	min	typ	max	unit
XSHUTDOWN rising – system ready	t0	5			ms
entering streaming mode – first frame start sequence (fixed part)	t1		4096 XVCLK cycles or 150 µs, whichever is larger		
entering streaming mode – first frame start sequence (variable part)	t2		delay is exposure time value		lines
AVDD/DOVDD/DVDD rising, whichever is last – XSHUTDOWN rising	t3	0			ms
external clock to XSHUTDOWN	t4	0			ms
AVDD/DOVDD/DVDD rising, whichever is last – PWDNB rising	t5	0			ms
PWDNB rising – system ready	t6	5			ms
external clock to PWDNB	t7	0			ms

figure 2-4 power up sequence (case 1)

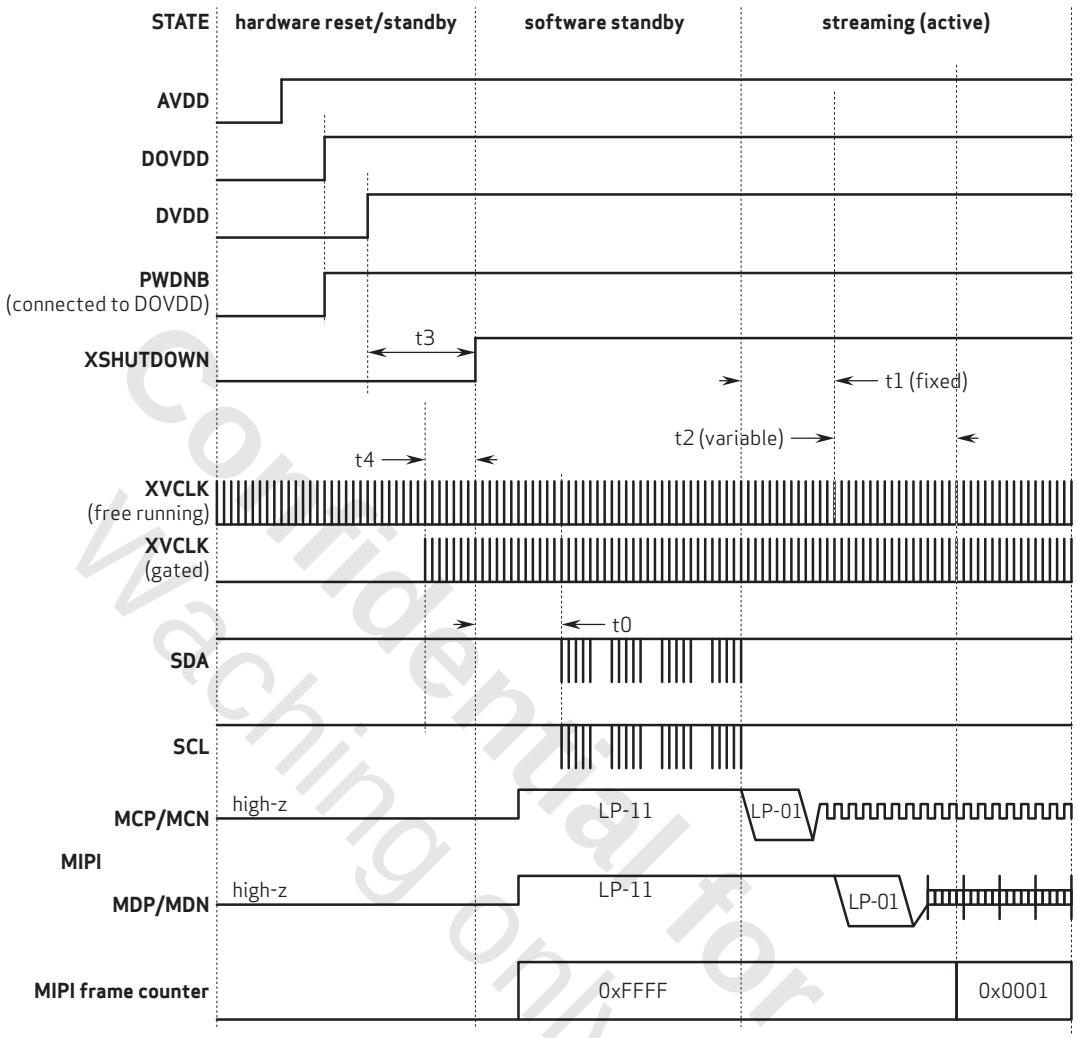
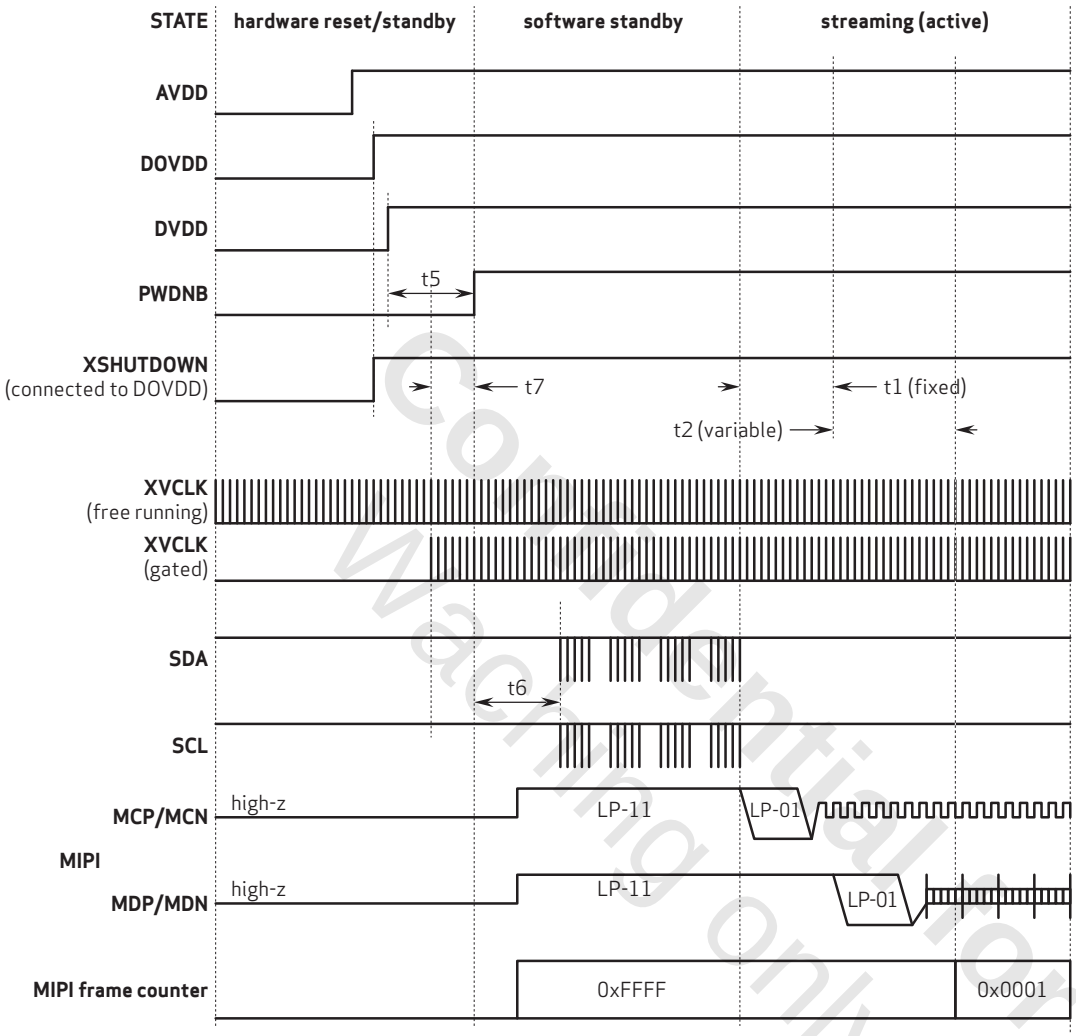


figure 2-5 power up sequence (case 2)



2.6.2 power down sequence

Similar to the power up sequence, the XVCLK input clock may be either gated or continuous. If the SCCB command to exit streaming is received while a frame of MIPI data is being output, then the sensor must wait until the MIPI frame end code before entering software standby mode.

If the SCCB command to exit streaming mode is received during the inter-frame time, then the sensor must enter software standby mode immediately.

Power down cases 1~2 correspond to power up sequences 1~2, respectively.

table 2-5 power down sequences

case	XSHUTDOWN	PWDNB	power up sequence requirement
1	GPIO	DOVDD	Refer to **figure 2-7** 1. Software standby is recommended 2. Pull XSHUTDOWN low for minimum power consumption 3. Cut off DVDD, AVDD, and DOVDD in any order
2	DOVDD	GPIO	Refer to **figure 2-8** 1. Software standby mode is recommended 2. Pull PWDNB low for low power consumption 3. Cut off DVDD, AVDD, and DOVDD in any order

table 2-6 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for MIPI end code before entering software for standby; otherwise, enter software standby mode immediately		
minimum of XVCLK cycles after last SCCB transaction or MIPI frame end	t1	512		XVCLK cycles
last SCCB transaction or MIPI frame end – XSHUTDOWN/PWDNB falling, whichever occurs first	t2	512		XVCLK cycles
XSHUTDOWN falling – AVDD/DOVDD/DVDD falling, whichever is first	t3	0.0		ns
PWDNB falling – AVDD/DOVDD/DVDD falling, whichever is first	t4	0.0		ns

figure 2-6 software standby sequence

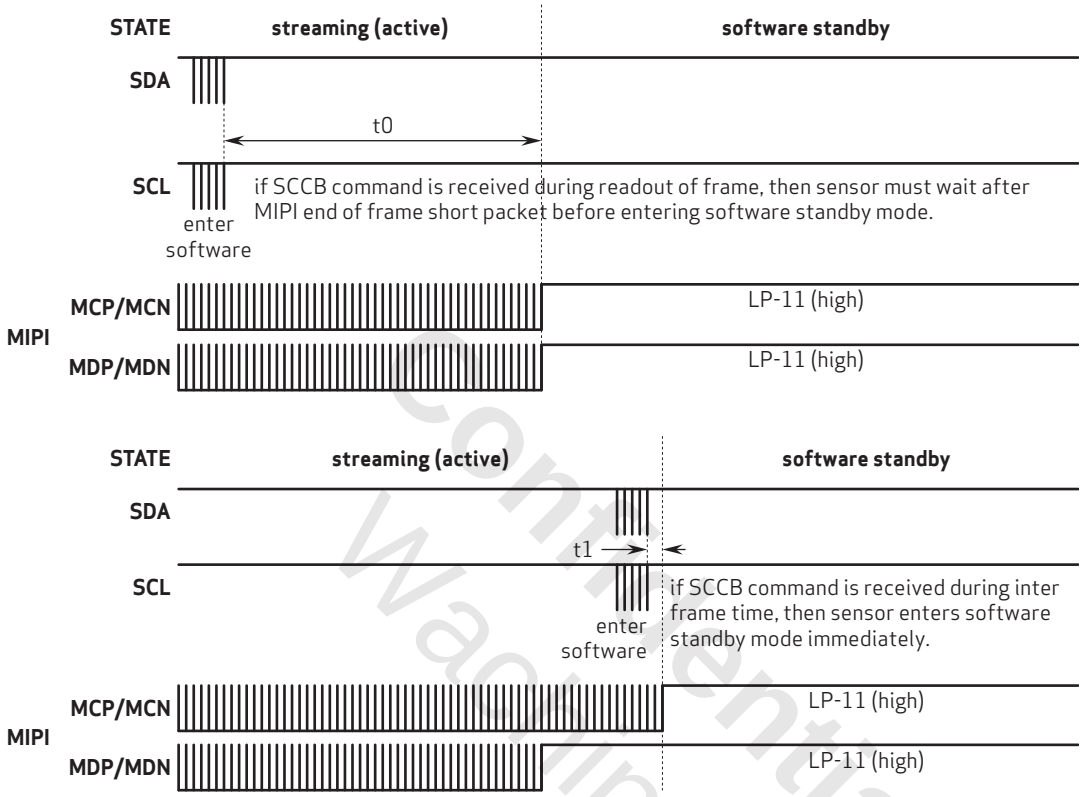


figure 2-7 power down sequence (case 1)

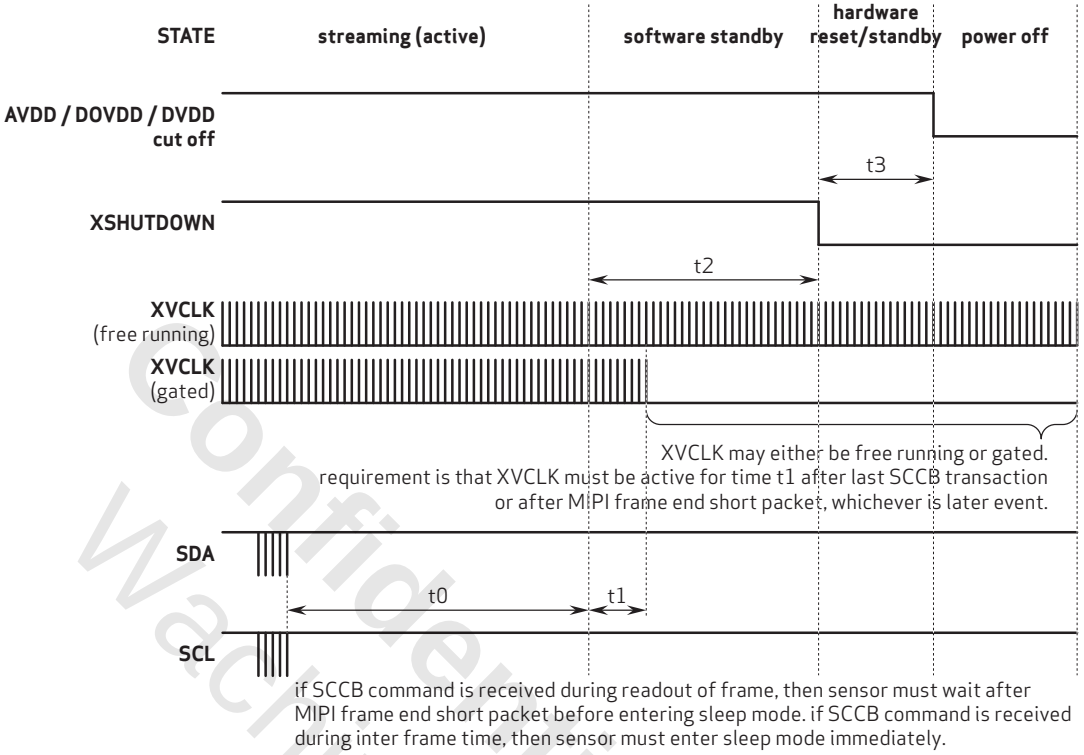
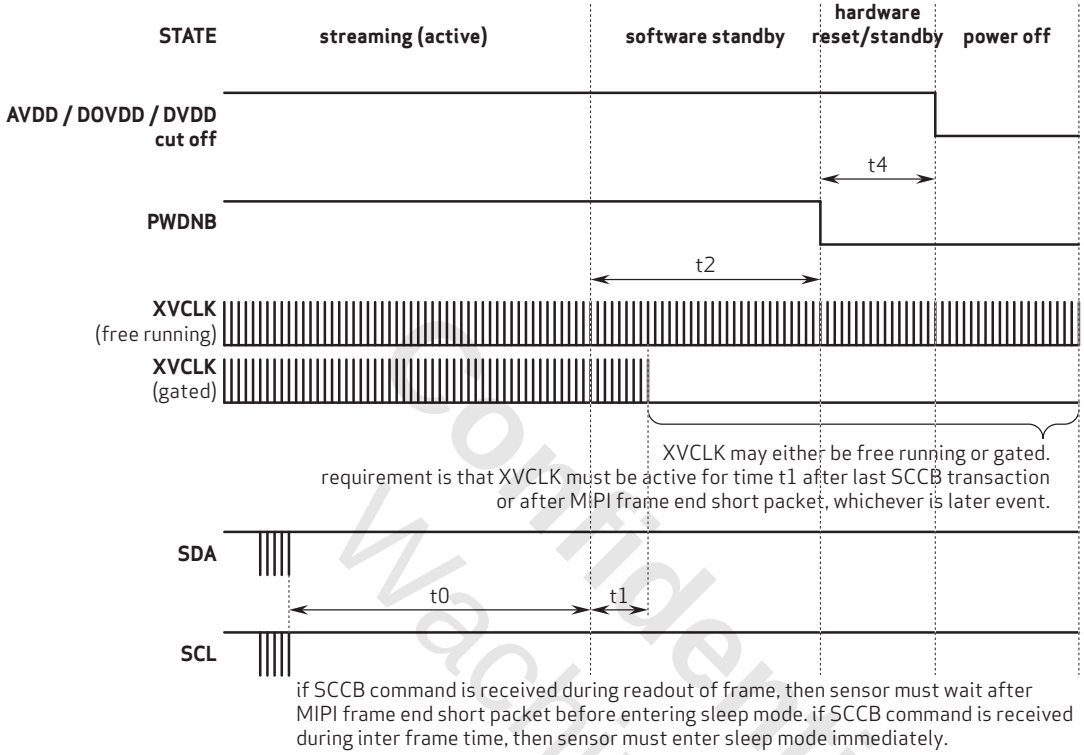


figure 2-8 power down sequence (case 2)



2.7 reset

The whole chip will be reset during power up. Manually applying a hard reset (XSHUTDOWN = 0) upon power up is recommended even though an on-chip power up reset is included. The hard reset is active low with an asynchronous design. The reset pulse width should be greater than or equal to 2 ms.

2.7.1 power on reset generation

The OV64B40 sensor includes an XSHUTDOWN pin that forces a complete hardware reset when it is pulled low (GND). Additionally, in this sensor, a power on reset is generated after the core power becomes stable. The OV64B40 clears all registers and resets them to their default values when a hardware reset occurs.

2.7.2 software reset

A reset can also be initiated through the SCCB interface by setting register 0x0103[0] to high and all registers will be reset to their default values.

2.8 hardware and software standby

Two suspend modes are available for the OV64B40:

- **hardware standby**
- **software standby**

2.8.1 hardware standby

Dropping any power source (AVDD/DOVDD/DVDD) or if XSHUTDOWN is tied to low, will initiate hardware standby mode. In this mode, the total power consumption will be less than 100 µW.

2.8.2 software standby

Executing a software power down (0x0100[0] = 0) through the SCCB interface suspends internal circuit activity, but does not halt the device clock. A 0 to 1 transition on register bit 0x0100[0] can resume the sensor from software standby mode.

table 2-7 hardware and standby descriptions

mode	description
hardware standby	1. Enabled by pulling XSHUTDOWN low 2. Power down all blocks 3. Register values are reset to default values 4. No SCCB communication 5. Minimum power consumption
software standby	1. Default mode after power on reset 2. Power down all blocks except SCCB 3. Register values are maintained 4. SCCB communication is available 5. Low power consumption 6. GPIO can be configured as high/low/tri-state

2.9 system clock control

PLL settings can only be changed during sensor software standby mode (0x0100 = 0).

2.9.1 PLL1

The voltage-controlled oscillator (VCO) range is from 1500 MHz to 3000 MHz. A programmable clock divider is provided to generate different frequencies. PLL1 provides a clock for the MIPI interface and can be tuned per field requirement as long as it is in the range and is fast enough to support the data throughput.

2.9.2 PLL2

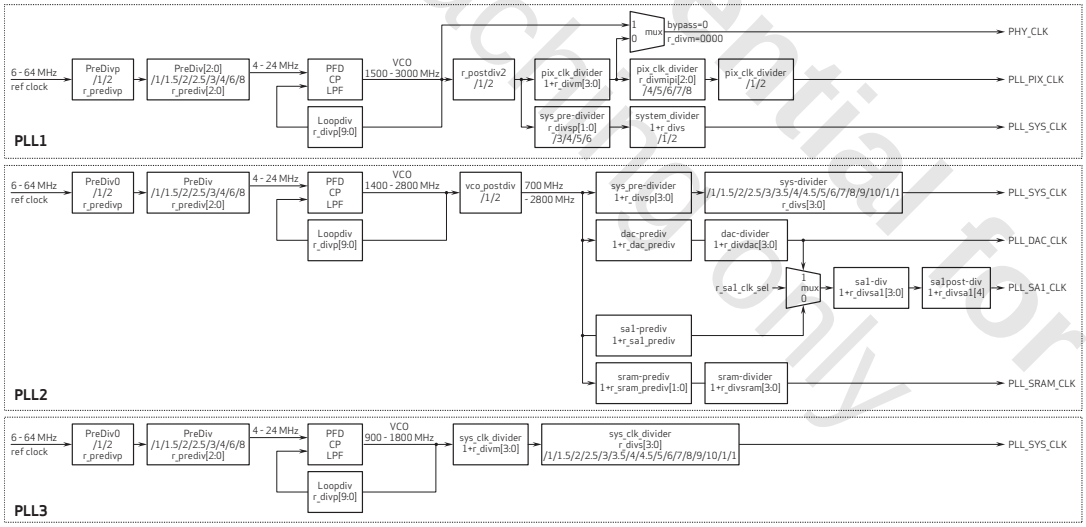
The VCO range is from 1400 MHz to 2800 MHz. A programmable clock divider is provided to generate different frequencies. PLL2 provides clocks for internal circuits and is usually optimized for performance. Tuning PLL2 is not recommended.

2.9.3 PLL3

The VCO range is from 900 MHz to 1800 MHz. A programmable clock divider is provided to generate different frequencies. PLL3 provides a clock for internal data throughput.

2.9.4 PLL clock scheme

figure 2-9 PLL diagram



note Contact your local OmniVision FAE for additional assistance on PLL configuration.

table 2-8 PLL control registers

address	register name	default value	R/W	description
0x0300	PLL_CTRL_0	0x02	RW	Bit[3]: pll1_bp_vco_sync
0x0301	PLL_CTRL_1	0x40	RW	Bit[7]: pll1_divs
0x0302	PLL_CTRL_2	0x33	RW	Bit[5]: pll1_div_rst_sync_en
0x0303	PLL_CTRL_3	0x03	RW	Bit[2:0]: pll1_prediv
0x0304	PLL_CTRL_4	0x01	RW	Bit[1:0]: pll1_divp[9:8]
0x0305	PLL_CTRL_5	0xB5	RW	Bit[7:0]: pll1_divp[7:0]
0x0306	PLL_CTRL_6	0x03	RW	Bit[2:0]: pll1_divmipi
0x0307	PLL_CTRL_7	0x00	RW	Bit[3:0]: pll1_divm
0x0308	PLL_CTRL_8	0x02	RW	Bit[1:0]: pll1_divsp
0x0309	PLL_CTRL_9	0x51	RW	Bit[7:6]: pll1_precision
0x0310	PLL_CTRL_16	0x00	RW	Bit[3:0]: pll1_cntstep[3:0]
0x0311	PLL_CTRL_17	0x00	RW	Bit[2]: pll1_frac_en
0x0312	PLL_CTRL_18	0x07	RW	Bit[2:0]: pll1_cntck
0x0313	PLL_CTRL_19	0x00	RW	Bit[3:0]: pll1_dsm[19:16]
0x0314	PLL_CTRL_20	0x00	RW	Bit[7:0]: pll1_dsm[15:8]
0x0315	PLL_CTRL_21	0x00	RW	Bit[7:0]: pll1_dsm[7:0]
0x0316	PLL_CTRL_22	0x33	RW	Bit[5:3]: pll1_lpf_r
0x0320	PLL_CTRL_32	0x12	RW	Bit[7]: pll2_bp_vco_sync
0x0321	PLL_CTRL_33	0x01	RW	Bit[3:0]: pll2_cp
0x0322	PLL_CTRL_34	0x53	RW	Bit[7:6]: pll2_precision
0x0323	PLL_CTRL_35	0x05	RW	Bit[2:0]: pll2_prediv
0x0324	PLL_CTRL_36	0x01	RW	Bit[1:0]: pll2_divp[9:8]
0x0325	PLL_CTRL_37	0xD0	RW	Bit[7:0]: pll2_divp[7:0]
0x0326	PLL_CTRL_38	0xCB	RW	Bit[7]: pll2_predivp
0x0361	PLL_CTRL_97	0x00	RW	Bit[3]: pll1_lat_sel Bit[2]: pll3_lat_en Bit[1]: pll2_lat_en Bit[0]: pll1_lat_en

2.10 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OV64B40, the SCCB ID is controlled by two SID pins and can be programmable. How to configure the SCCB ID is shown below:

- {SID2, SID} = 0x0: SCCB ID read address is 0x6C, SCCB ID write address is 0x6D, SCCB ID register is 0x3035
- {SID2, SID} = 0x1: SCCB ID read address is 0x20, SCCB ID write address is 0x21, SCCB ID register is 0x3037
- {SID2, SID} = 0x2: SCCB ID read address is 0x44, SCCB ID write address is 0x45, SCCB ID register is 0x3039
- {SID2, SID} = 0x3: SCCB ID read address is 0x46, SCCB ID write address is 0x47, SCCB ID register is 0x303A

There is also an alternative ID in register 0x3036, which has a default value of 0x42.

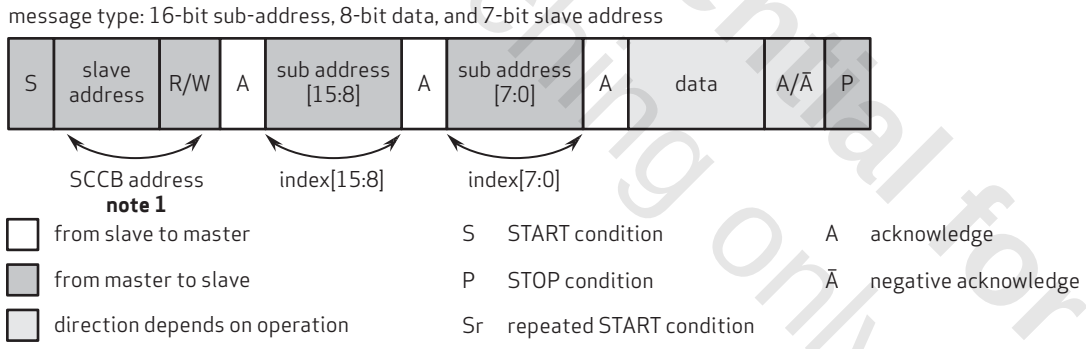
2.10.1 data transfer protocol

Data transfer of the OV64B40 follows the SCCB protocol.

2.10.2 message format

The OV64B40 supports the message format shown in **figure 2-10**. The repeated START (Sr) condition is not shown in **figure 2-10**, but is shown in **figure 2-11** and **figure 2-13**.

figure 2-10 message type



note 1 slave address must be 0x36 for SCCB write address to be 0x6C and for SCCB read address to be 0x6D

2.10.3 read / write operation

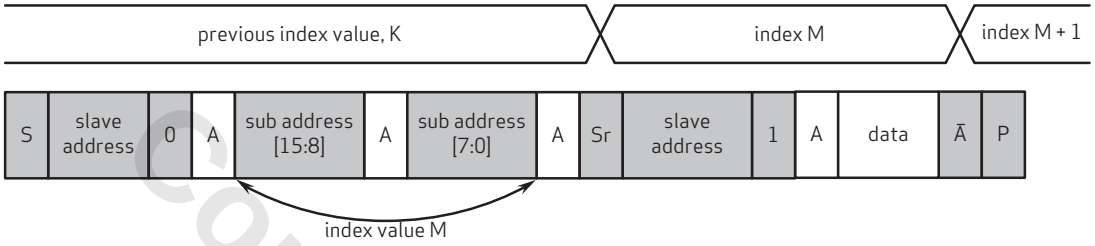
The OV64B40 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

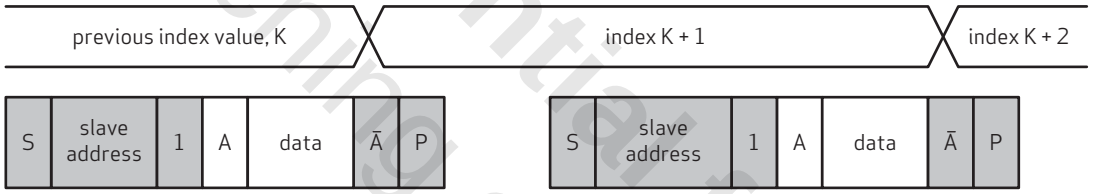
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-11**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-11 SCCB single read from random location



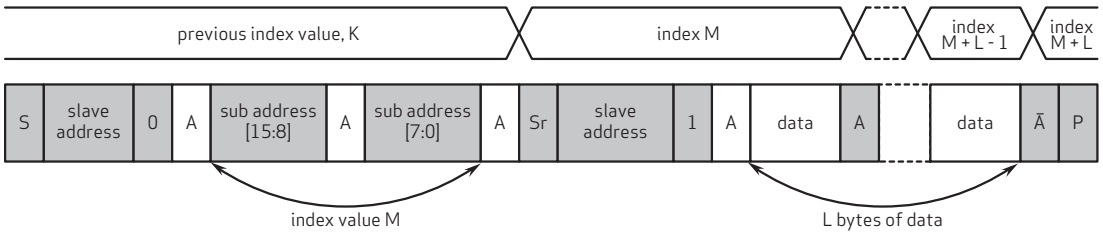
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 2-12**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-12 SCCB single read from current location



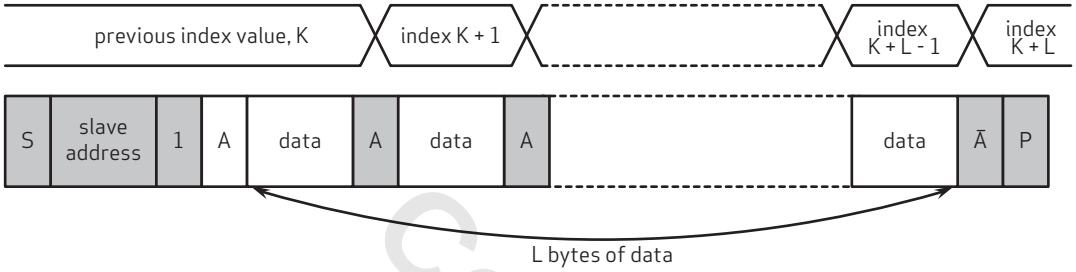
The sequential read from a random location is illustrated in **figure 2-13**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-13 SCCB sequential read from random location



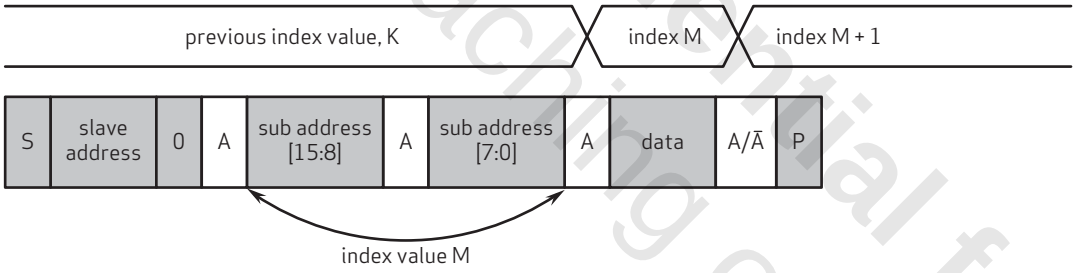
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation as shown in **figure 2-14**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-14 SCCB sequential read from current location



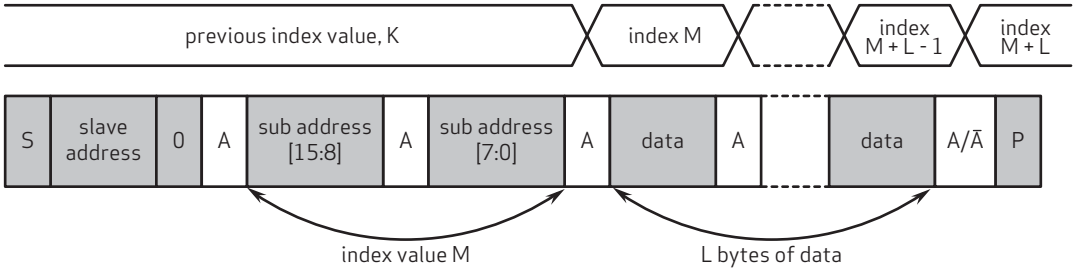
The write operation to a random location is illustrated in **figure 2-15**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-15 SCCB single write to random location



The sequential write is illustrated in **figure 2-16**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-16 SCCB sequential write to random location



2.10.4 SCCB timing

figure 2-17 SCCB interface timing

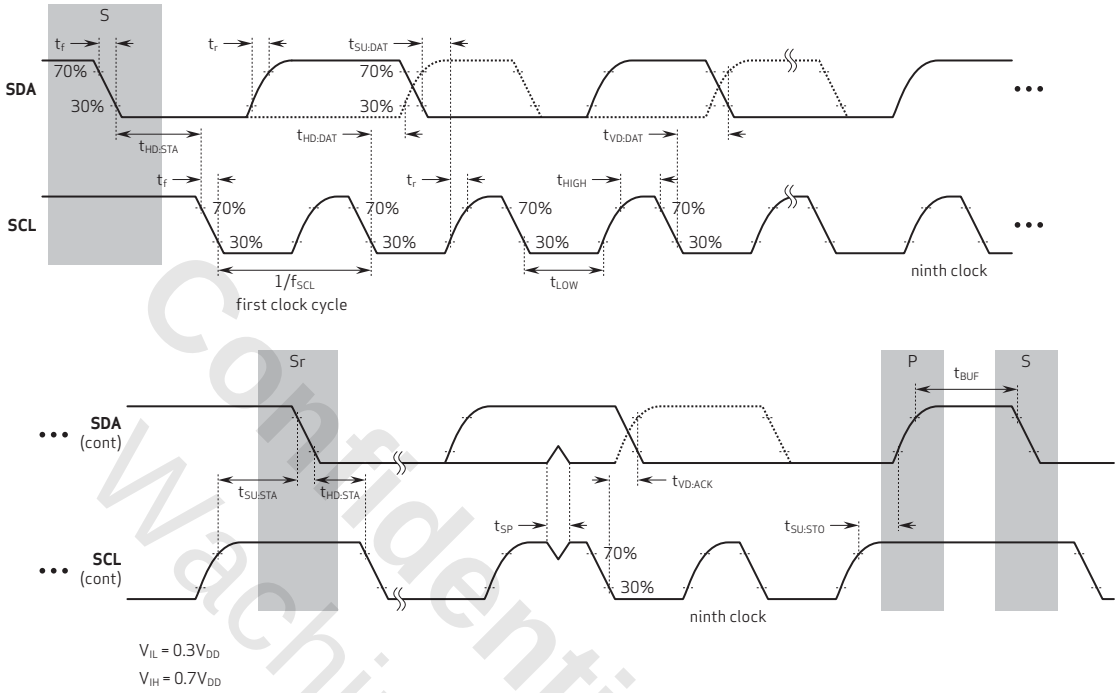


table 2-9 SCCB interface timing specifications[a] (sheet 1 of 2)

symbol	parameter	400 kHz mode		1000 kHz mode		unit
		min	max	min	max	
f_{SCL}	clock frequency		400		1000[b]	kHz
t_{LOW}	clock low period	1.3	–	0.5	–	µs
t_{HIGH}	clock high period	0.6	–	0.26	–	µs
t_{BUF}	bus free time before new start	1.3	–	0.5	–	µs
$t_{HD:STA}$	start condition hold time	0.6	–	0.26	–	µs
$t_{SU:STA}$	start condition setup time	0.6	–	0.26	–	µs
$t_{HD:DAT}$	data hold time	0	–	0	–	µs
$t_{SU:DAT}$	data setup time	100	–	50	–	ns
$t_{VD:DAT}$	data valid time	–	0.9	–	0.45	µs

table 2-9 SCCB interface timing specifications[a] (sheet 2 of 2)

symbol	parameter	400 kHz mode		1000 kHz mode		unit
		min	max	min	max	
$t_{VD:ACK}$	data valid acknowledge time	–	0.9	–	0.45	µs
$t_{SU:STO}$	stop condition setup time	0.6	–	0.26	–	µs
t_r	SCCB rise time	20	300	–	120	ns
t_f	SCCB fall time		300		120	ns
t_{SP}	pulse width of spikes that must be suppressed by input filter	0	50	0	50	ns
C_b	capacitive load for each bus line	–	400	–	550	pF

a. timing measurement shown at beginning of rising edge and/or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge and/or beginning of falling edge signifies 70%

b. input clock range: 12 MHz and 27 MHz; SCCB pull-up resistor: 2K ohm

2.11 group write

Group write is supported in order to update a group of registers in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

The OV64B40 supports up to ten groups (0, 1, 2, 3, 10, 11, 12, 13, 14, and 15) that can be recorded and launched in the same frame. Group 4~9 are reserved. These groups share 3072 bytes of memory and the size of each group is programmable by adjusting the start address.

table 2-10 context switching control (sheet 1 of 3)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Bit[7:0]: group_adr0
0x3201	GROUP ADR1	0x04	RW	Bit[7:0]: group_adr1
0x3202	GROUP ADR2	0x08	RW	Bit[7:0]: group_adr2
0x3203	GROUP ADR3	0x0C	RW	Bit[7:0]: group_adr3
0x3204	GROUP ADR4	0x10	RW	Bit[7:0]: group_adr4
0x3205	GROUP ADR5	0x14	RW	Bit[7:0]: group_adr5
0x3206	FSIN GRP	0x00	RW	Bit[7]: re_launch_disable Bit[4]: fsin_en Bit[1:0]: Start group in FSIN mode
0x3207	COMBINE LAUNCH CTRL	–	W	Bit[7:4]: Launch option select 0110: Launch at HBLK 1010: Launch in frame blanking 1110: Launch directly Bit[3]: cmb_lch_grp3 Combine launch includes group3 Bit[2]: cmb_lch_grp2 Combine launch includes group2 Bit[1]: cmb_lch_grp1 Combine launch includes group1 Bit[0]: cmb_lch_grp0 Combine launch includes group0

table 2-10 context switching control (sheet 2 of 3)

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 0110: Launch at HBLK 1010: Launch in frame blanking 1110: Launch directly Bit[3:0]: group_id 0000: Group bank 0, default start from address 9'h000 0001: Group bank 1, default start from address 9'h040 0010: Group bank 2, default start from address 9'h080 0011: Group bank 3, default start from address 9'h0C0 0100: Group bank 4, default start from address 9'h100 0101: Group bank 5, default start from address 9'h140 0110: Group bank 6, default start from address 9'h180 0111: Group bank 7, default start from address 9'h1A0 1000: Group bank 8, default start from address 9'h1C0 1001: Group bank 9, default start from address 9'h1E0 1010: Group bank 10, default start from address 0x100 1011: Group bank 11, default start from address 9'h120 1100: Group bank 12, default start from address 9'h140 1101: Group bank 13, default start from address 9'h160 1110: Group bank 14, default start from address 9'h180 1111: Group bank 15, default start from address 9'h1A0
0x3209	GRP0 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp0
0x320A	GRP1 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp1
0x320B	GRP2 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp2
0x320C	GRP3 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp3
0x320D	GRP SWCTRL	0x01	RW	Bit[7]: Context switch enable Bit[6:4]: Auto launch loop number Bit[3:0]: Switch back group

table 2-10 context switching control (sheet 3 of 3)

address	register name	default value	R/W	description
0x320E	CONTEXT SW GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0110: Launch at HBLK 1010: Launch in frame blanking 1110: Launch directly Bit[3:0]: group_id 0000: Group bank 0, default start from address 11'h000 0001: Group bank 1, default start from address 11'h100 0010: Group bank 2, default start from address 11'h200 0011: Group bank 3, default start from address 11'h300 1010: Group bank 10, default start from address 11'h500 1011: Group bank 11, default start from address 11'h520 1100: Group bank 12, default start from address 11'h540 1101: Group bank 13, default start from address 11'h560 1110: Group bank 14, default start from address 11'h580 1111: Group bank 15, default start from address 11'h5A0
0x321A	GRP ACT	–	R	Indicates Which Group is Active
0x3239	GRP10 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp10
0x323A	GRP11 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp11
0x323B	GRP12 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp12
0x323C	GRP13 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp13
0x323D	GRP14 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp14
0x323E	GRP15 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp15

2.11.1 hold

After the groups are configured, users can perform a hold operation to store register settings into the SRAM of each group. The hold of each group starts and ends with control register 0x3208. The lower four bits of register 0x3208 control which group to access, and the upper four bits control the start (0x0: hold start) and end (0x1: hold end) of the hold operation.

The example setting below shows the sequence to hold group 0:

```
6C  3208  00    group 0 hold start
6C  3800  11    first register into group 0
6C  3911  22    second register into group 0
6C  3208  10    group 0 hold end
```

2.11.2 launch

After the contents of each group are defined in the hold operation, all registers belonging to each group are stored in SRAM and ready to be written into target registers (i.e., launch of that group).

There are eight launch modes as described in **section 2.11.2.1** to **section 2.11.2.8**.

2.11.2.1 launch mode 1 – quick manual launch

Manual launch is enabled by setting register 0x320D to 0.

Quick manual launch is achieved by writing to control register 0x3208. The value written into this register is 0xEX, the upper 4 bits (0xE) are the quick launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 2, they write the value 0xE2 to register 0x3208, then the contents of group 2 will be written to the target registers immediately after the sensor gets this command through the SCCB. Below is an example of this setting.

```
6C  320D  00    manual launch on
6C  3208  E2    quick manual launch group 2
```

2.11.2.2 launch mode 2 – delay manual launch

Delay manual launch is achieved by writing to register 0x3208. The value written into this register is 0xAX, where the upper four bits (0xA) are the delay launch command and the lower four bits (0xX) are the group number. For example, if users want to launch group 11, they just write the value 0xAB to register 0x3208, then the contents of group 11 will be written to the target registers. The difference with mode 1 is that the writing will wait for some internally defined time spot in vertical blanking, and is thus delayed. Below is an example of this setting.

```
6C  320D  00    manual launch on
6C  3208  AB    delay manual launch group 11
```

2.11.2.3 launch mode 3 – quick auto launch

Quick auto launch works like the mode 1, but the difference is it will return to a specified group automatically. This is controlled by the register 0x320D, where bit[7] is context switch mode enable, bit[6:4] is switch loop number and bit[3:0] controls which group to return. 0x3209, 0x320A, 0x320B, 0x320C, 0x3239, 0x323A, 0x323B, 0x323C, 0x323D, and 0x323E, which are the frame number of group 0, 1, 2, 3, 10, 11, 12, 13, 14, and 15, respectively, controls how many frames to stay before returning.

The operation can be better understood with an example of this setting:

```
6C  320D  9A    Bit[7]: auto switch enable; Bit[6:4]: 1, one loop; Bit[3:0]: a,
                return to group 10
6C  3209  04    stay in group 0 for 4 frames
6C  320A  00    stay in group 1 for 0 frames
6C  320B  00    stay in group 2 for 0 frames
6C  320C  00    stay in group 3 for 0 frames
6C  3239  01    stay in group 10 for 1 frames
6C  323A  00    stay in group 11 for 0 frames
6C  323B  00    stay in group 12 for 0 frames
6C  323C  00    stay in group 13 for 0 frames
6C  323D  00    stay in group 14 for 0 frames
6C  323E  00    stay in group 15 for 0 frames
6C  320E  E0    quick auto launch group 0
```

In this example, the sensor will quick launch group 0, stay at group 0 for 4 frames, and then return to group 10.

2.11.2.4 launch mode 4 – delay auto launch

Delay auto launch works like mode 2 in the delay launch part and like the mode 3 in the return part.

The operation can be better understood with an example of this setting:

```
6C  320D  9A    Bit[7]: auto switch enable; Bit[6:4]: 1, one loop; Bit[3:0]: a,
                return to group 10
6C  3209  04    stay in group 0 for 4 frames
6C  320A  00    skip group 1
6C  320B  00    skip group 2
6C  320C  00    skip group 3
6C  3239  01    stay in group 10 for 1 frames
6C  323A  00    skip group 11
6C  323B  00    skip group 12
6C  323C  00    skip group 13
6C  323D  00    skip group 14
6C  323E  00    skip group 15
6C  320E  A0    delay auto launch group 0
```

In this example, the sensor will delay launch group 0, stay at group 0 for 4 frames, and then return to group 10.

2.11.2.5 launch mode 5 – repeat launch

Repeat launch is also controlled by 0x320D. The only difference between auto launch is that loop number (0x320D[6:4]) should be set to 0. It can support up to ten groups repeating. Registers 0x3209, 0x320A, 0x320B, and 0x320C, which is the frame number of group 0, 1, 2, and 3, respectively, controls how many frames to stay before jumping to the next one. In this mode, the launch is repeated automatically among the group 0, group 1, group 2, and group 3. If any of the group number is set to be 0, that group is skipped.

The operation can be better understood with an example of this setting:

```
6C  320D  80    Bit[7]: context switch enable, Bit[6:4]: 0 loop
6C  3209  02    stay 2 frames in group 0
6C  320A  03    stay 3 frames in group 1
6C  320B  00    skip group 2
6C  320C  00    skip group 3
6C  323A  00    skip group 11
6C  323B  00    skip group 12
6C  323C  08    stay 8 frames in group 13
6C  323D  00    skip group 14
6C  323E  00    skip group 15
6C  320E  A0    delay auto launch group 0
```

In this example, the sensor will delay launch group 0, stay at group 0 for 2 frames, then switch to group 1, staying for 3 frames, then switch to group 13, staying for 8 frames, then switch back to group 0 for 2 frames, group 1 for 3 frames, group 13 for 8 frames and so on.

2.11.2.6 launch mode 6 – auto/repeat launch and manual launch combination

Combine manual launch and auto/repeat launch. During auto/repeat launch, manual launch can be made.

The operation can be better understood with an example of this setting:

```
6C  320D  80    context switch enable, Bit[6:4]: 0 loop
6C  3209  02    stay 2 frames in group 0
6C  320A  03    stay 3 frames in group 1
6C  320B  00    skip group 2
6C  320C  08    stay 8 frames in group 3
6C  3239  00    skip group 10
6C  323A  00    skip group 11
6C  323B  00    skip group 12
6C  323C  00    skip group 13
6C  323D  00    skip group 14
6C  323E  00    skip group 15

6C  320E  A0    delay auto launch group 0
6C  3208  A2    delay manual launch group 12
```

In this example, the sensor receives delay repeat launch command and delay manual launch command consecutively. When launch trigger comes, the sensor will first delay launch group 12 and right after that, delay launch group 0. Then the sensor will keep switching between group 0, group 1, and group 3.

2.11.2.7 launch mode 7 – launch in sleep mode

By default, during sleep mode, delay manual launch command or auto/repeat launch command, will be treated as a quick manual launch command or a quick auto/repeat launch command. To disable this mode, set register bit 0x3680[2] to 1'b1 and the setting will be launched in normal delay mode.

2.11.2.8 launch mode 8 – delay launch multiple groups in one frame

The only difference with mode 2 is that register 0x3208 is written multiple times for multiple groups. In vertical blanking, those groups will be launched one by one.

The operation can be better understood with an example of this setting:

```
6C  320D  00    manual launch on
6C  3208  A0    delay launch group 0
6C  3208  A1    delay launch group 1
6C  3208  A3    delay launch group 3
```

3 block level description

3.1 pixel array structure

The OV64B40 sensor has an image array of 9280 columns by 6976 rows (64,737,280 pixels). **figure 3-1** shows a cross-section of the image sensor array.

In the OV64B40, the color filters are arranged in a 4-cell pattern. The primary color array is arranged in line alternation fashion. Of the 64,737,280 pixels, 64,218,112 (9248x6944) are active pixels and can be output.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

Long exposure time is controlled by registers {0x3500, 0x3501, 0x3502}.

Medium exposure time is controlled by registers {0x3540, 0x3541, 0x3542}.

Short exposure time is controlled by registers {0x3580, 0x3581, 0x3582}.

Maximum exposure time is VTS-24 for full resolution and VTS-12 for downsample mode. Minimum exposure time is 8 rows for full resolution and 4 rows for downsample mode.

note
Maximum exposure = VTS - 24 lines for full resolution (VTS - 12 lines for downsample mode), minimum exposure = 8 rows for full resolution and 4 rows for downsample mode

figure 3-1 sensor output pattern (9248x6944)

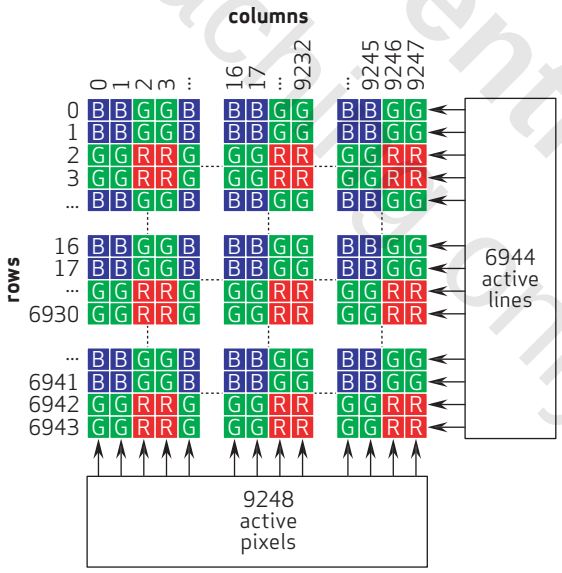


table 3-1 exposure control registers

address	register name	default value	R/W	description
0x3500	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[23:16]
0x3501	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[15:8]
0x3502	EXPO COARSE	0x40	RW	Bit[7:0]: expo_coarse[7:0]
0x3508	GAIN COARSE	0x01	RW	Bit[6:0]: gain_coarse[6:0]
0x3509	CTRL 09	0x00	RW	Bit[7:1]: gain_fine
0x3540	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[23:16]
0x3541	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[15:8]
0x3542	EXPO COARSE	0x40	RW	Bit[7:0]: expo_coarse[7:0]
0x3548	GAIN COARSE	0x01	RW	Bit[6:0]: gain_coarse[6:0]
0x3549	CTRL 09	0x00	RW	Bit[7:1]: gain_fine
0x3580	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[23:16]
0x3581	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[15:8]
0x3582	EXPO COARSE	0x40	RW	Bit[7:0]: expo_coarse[7:0]
0x3588	GAIN COARSE	0x01	RW	Bit[6:0]: gain_coarse[6:0]
0x3589	AEC_PK_9	0x00	RW	Bit[7:1]: gain_fine

3.2 binning

Binning mode is usually used for low resolution. When the binning function is on, the adjacent same-color pixels are averaged or summed (see **figure 3-2**). If the binning function is off, the pixels, which are not output, are skipped. The OV64B40 supports two types of 2x2 binning. One binning type is four adjacent same-color pixels that are summed in array. The other binning type is two adjacent same-color pixels that are summed in array in the vertical direction, then passed to the sensor ISP block to perform sum/average in the horizontal direction.

figure 3-2 example of 2x2 binning

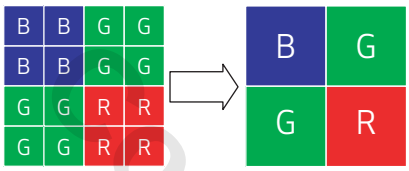


table 3-2 binning-related registers

address	register name	default value	R/W	description
0x3820	TIMING_CTRL_32	0x40	RW	Bit[1]: Array vertical 4-cell bin
0x3821	TIMING_CTRL_33	0x00	RW	Bit[4]: 4-cell horizontal bin mode
0x5001	ISP_TOP_1	0x1F	RW	Bit[7]: raw_bin_en
0x5180	RAW_BIN_1315_D2V2_TOP_0	0xC5	RW	Bit[1]: m_bVBinningEnable Enable vertical binning Bit[0]: m_bHBinningEnable Enable horizontal binning

3.3 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

3.4 10-bit A/D converters

The balanced signal is then digitized by the on-chip 10-bit ADC.

3.5 PDAF control

The OV64B40 supports PDAF data output through MIPI by programmable data type mode or virtual channel mode. All PDAF data or partial PDAF data are selected for output. In mirror mode, PDAF data can also be mirrored.

3.5.1 PDAF data output: option 1 (programmable data type)

Option 1 uses programmable data type for PDAF raw data. Set register bits 0x3684[0] to 1, 0x3684[1] to 1, 0x3684[2] to 0, and 0x3684[3] to 1 to enable PD output timing under MIPI data type mode. Register bits 0x3699[5:0] is the data type of PD data. PDAF data is output during image data horizontal blanking. Maximum PDAF pixel number in one package is configured by registers {0x4640, 0x4641}*8.

3.5.2 PDAF data output: option 2 (MIPI virtual channel)

Option 2 is the MIPI virtual channel for PDAF raw data. Set registers bits 0x3684[0] to 1, 0x3684[1] to 1, 0x3684[2] to 1, and 0x3684[3] to 0 to enable PDAF output timing, and set register bit 0x480E[2] to 1 to enable MIPI virtual channel mode. A normal image outputs through MIPI virtual channel 0. PDAF data outputs through MIPI virtual channel 1. PDAF data is output during image data horizontal blanking. Maximum PDAF pixel number in one package is configured by registers {0x4640, 0x4641}*8.

figure 3-3 PDAF data output diagram

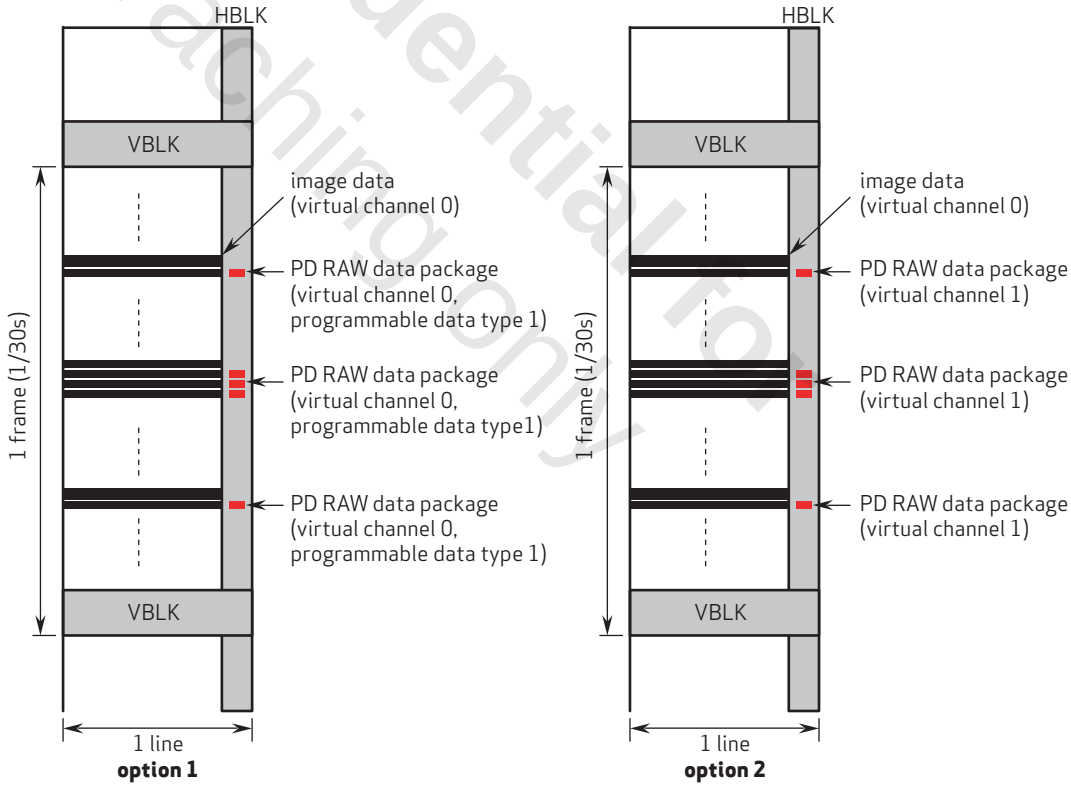


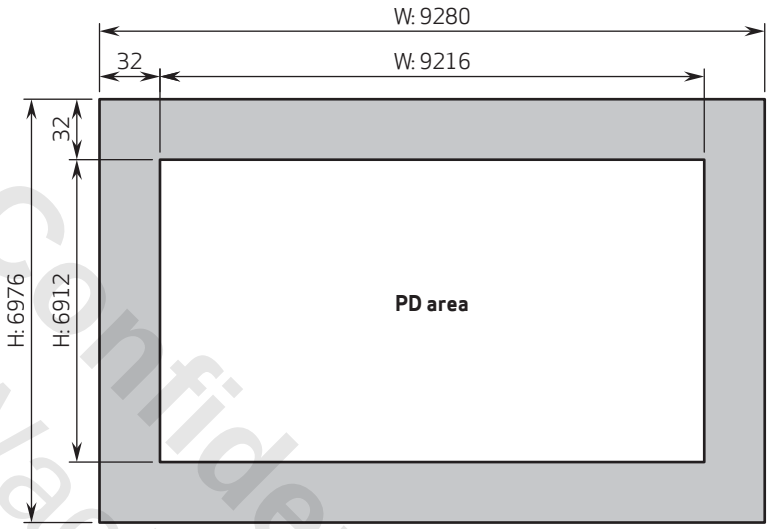
table 3-3 PDAF control registers

address	register name	default value	R/W	description
0x3684	CORE_4	0x17	RW	Bit[6]: r_pd_swap_up_dn Option to swap PD data upper/lower row Bit[5]: r_pd_rev_en Option to swap PD data left/right pixel Bit[4]: r_pd_low8 Option to output low 8 bits PD data Bit[3]: r_pd_dt_mode PD DT mode enable Bit[2]: r_pd_vc_mode PD VC mode enable Bit[1]: r_pd_data_en PD data output enable Bit[0]: r_pdaf_mipi_align_en MIPI align enable
0x3699	CORE_25	0x13	RW	Bit[5:0]: PD data DT
0x4640	VFIFO_40_0	0x00	RW	Bit[7:0]: start_size[15:8]
0x4641	VFIFO_40_1	0x30	RW	Bit[7:0]: start_size[7:0]
0x484B	MIPI_CORE_75	0x07	RW	Bit[6]: Line start select 0: Line start short packet from VFIFO non-empty 1: Line start short packet from VFIFO ready

3.6 PD pixel arrangement

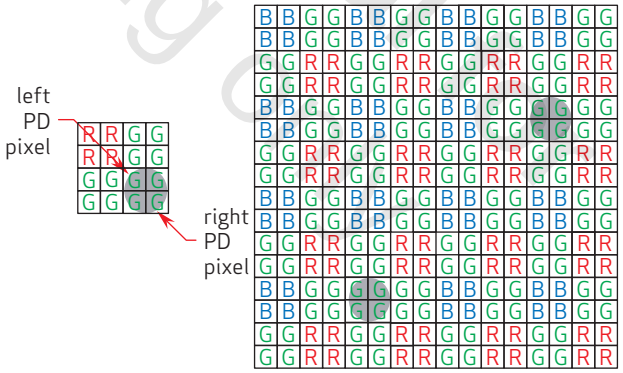
PD pixels are evenly arranged in the PD area.

figure 3-4 PD pixel arrangement



For 4C ML PD, the full size PD pattern is an area of 16x16, evenly placed in the PD area as shown in **figure 3-5**.

figure 3-5 4C ML PD pattern



note 1 first 16x16 pattern location is (32, 32) for 9248x6944

note 2 PD pixel are all green pixels

note 3 PD pattern is on final output image and sensor orientation is in correct orientation for correct image with normal (non-mirror/non-flip) sensor setting (see **section 9** for correct orientation)

4 image sensor core digital functions

4.1 mirror and flip

The OV64B40 provides mirror and flip readout modes, which respectively, reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	TIMING_CTRL_32	0x40	RW	Bit[2]: Vertical flip
0x3821	TIMING_CTRL_33	0x00	RW	Bit[2]: Mirror

4.2 image cropping/windowing

An image windowing area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. Windowing is achieved by masking off the pixels outside of the window; thus, the original timing is not affected.

To crop a specific size, the user must configure H/V output size (registers 0x3808~0x380B), H/V start address (registers 0x3800~0x3803), H/V end address (registers 0x3804~0x3807) and H/V offset (registers 0x3810~0x3813).

figure 4-2 image cropping/windowing

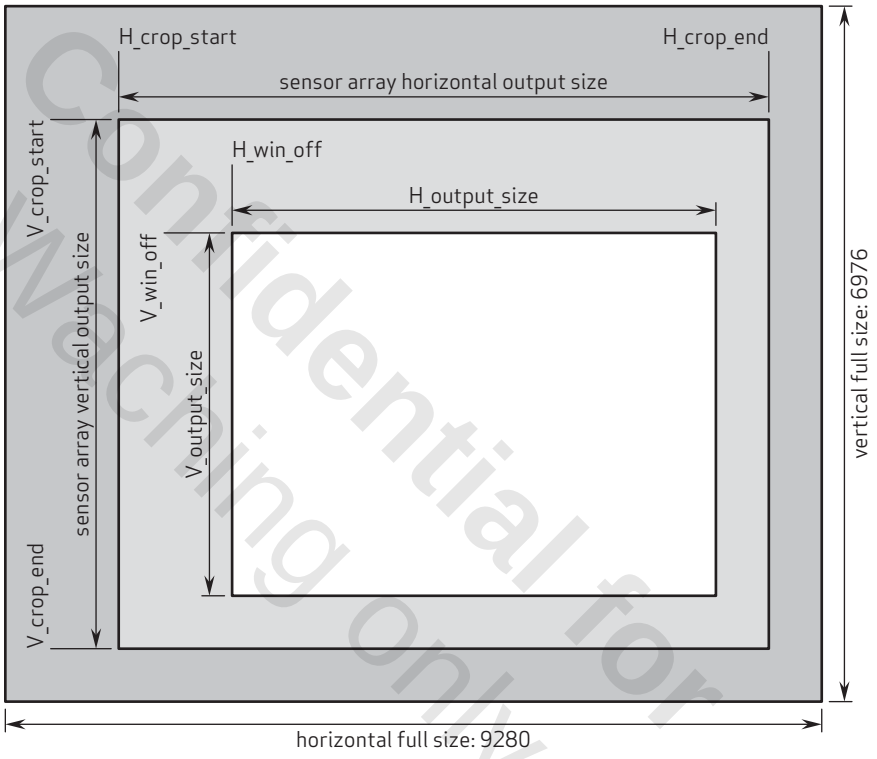


table 4-2 image cropping/windowing control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	TIMING_CTRL_0	0x00	RW	Bit[7:0]: Array horizontal start point[15:8]
0x3801	TIMING_CTRL_1	0x00	RW	Bit[7:0]: Array horizontal start point[7:0]
0x3802	TIMING_CTRL_2	0x00	RW	Bit[7:0]: Array vertical start point[15:8]
0x3803	TIMING_CTRL_3	0x00	RW	Bit[7:0]: Array vertical start point[7:0]

table 4-2 image cropping/windowing control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3804	TIMING_CTRL_4	0x24	RW	Bit[7:0]: Array horizontal end point[15:8]
0x3805	TIMING_CTRL_5	0x3F	RW	Bit[7:0]: Array horizontal end point[7:0]
0x3806	TIMING_CTRL_6	0x1B	RW	Bit[7:0]: Array vertical end point[15:8]
0x3807	TIMING_CTRL_7	0x3F	RW	Bit[7:0]: Array vertical end point[7:0]
0x3808	TIMING_CTRL_8	0x24	RW	Bit[7:0]: ISP horizontal output width[15:8]
0x3809	TIMING_CTRL_9	0x20	RW	Bit[7:0]: ISP horizontal output width[7:0]
0x380A	TIMING_CTRL_10	0x1B	RW	Bit[7:0]: ISP vertical output height[15:8]
0x380B	TIMING_CTRL_11	0x20	RW	Bit[7:0]: ISP vertical output height[7:0]
0x380C	TIMING_CTRL_12	0x02	RW	Bit[7:0]: Total horizontal timing size[15:8]
0x380D	TIMING_CTRL_13	0x94	RW	Bit[7:0]: Total horizontal timing size[7:0]
0x380E	TIMING_CTRL_14	0x1D	RW	Bit[7:0]: Total vertical timing size[15:8]
0x380F	TIMING_CTRL_15	0x98	RW	Bit[7:0]: Total vertical timing size[7:0]
0x3810	TIMING_CTRL_16	0x00	RW	Bit[7:0]: ISP horizontal windowing offset[15:8]
0x3811	TIMING_CTRL_17	0x10	RW	Bit[7:0]: ISP horizontal windowing offset[7:0]
0x3812	TIMING_CTRL_18	0x00	RW	Bit[7:0]: ISP vertical windowing offset[15:8]
0x3813	TIMING_CTRL_19	0x10	RW	Bit[7:0]: ISP vertical windowing offset[7:0]
0x3814	TIMING_CTRL_20	0x11	RW	Bit[7:4]: X odd increase number Bit[3:0]: X even increase number
0x3815	TIMING_CTRL_21	0x11	RW	Bit[7:4]: Y odd increase number Bit[3:0]: Y even increase number
0x383B	TIMING_CTRL_59	0x00	RW	Bit[7]: threshold_vts_sub 0: For shift down 1: For shift up Bit[6:0]: Vertical offset shift

4.3 test pattern

For testing purposes, the OV64B40 offers test pattern: color bar. The OV64B40 also offers two digital effects: transparent effect and rolling bar effect. The output type of digital test pattern is controlled by the test_pattern_type register (0x50C1[5:4]). The digital test pattern function is controlled by register 0x50C1[0]. For medium and short exposure, color bar is controlled by 0x53C1 and 0x56C1, respectively.

4.3.1 color bar

There are four types of color bars which are switched by bar-style in register 0x50C1[5:4] (see **figure 4-3**).

figure 4-3 color bar types

4.3.2 transparent effect

The transparent effect is enabled by transparent_en register (0x50C1[3]). If this register is set, the transparent test pattern will be displayed. **figure 4-4** is an example showing a transparent color bar image.

figure 4-4 transparent effect

4.3.3 rolling bar effect

The rolling bar is set by rolling_bar_en register (0x50C1[2]). If it is set, an inverted-color rolling bar will roll from up to down. **figure 4-5** is an example showing a rolling bar on color bar image.

figure 4-5 rolling bar effect

table 4-3 test pattern registers

address	register name	default value	R/W	description
0x50C1	PRE_ISP_2325_D2V2_TOP_1	0x00	RW	Bit[7]: Flip option Range is [0:1] Bit[6]: Mirror option Range is [0:1] Bit[5:4]: Color bar option Range is [0:3] Bit[3]: Transparent mode enable Range is [0:1] Bit[2]: Rolling mode enable Range is [0:1] Bit[1]: Clear last four bits enable Range is [0:1] Bit[0]: Test pattern enable Range is [0:1]
0x53C1	PRE_ISP_2325_D2V2_TOP_1	0x00	RW	Bit[7]: Flip option Range is [0:1] Bit[6]: Mirror option Range is [0:1] Bit[5:4]: Color bar option Range is [0:3] Bit[3]: Transparent mode enable Range is [0:1] Bit[2]: Rolling mode enable Range is [0:1] Bit[1]: Clear last four bits enable Range is [0:1] Bit[0]: Test pattern enable Range is [0:1]
0x56C1	PRE_ISP_2325_D2V2_TOP_1	0x00	RW	Bit[7]: Flip option Range is [0:1] Bit[6]: Mirror option Range is [0:1] Bit[5:4]: Color bar option Range is [0:3] Bit[3]: Transparent mode enable Range is [0:1] Bit[2]: Rolling mode enable Range is [0:1] Bit[1]: Clear last four bits enable Range is [0:1] Bit[0]: Test pattern enable Range is [0:1]

4.4 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration.

There are two main functions of the BLC:

- applying all normal pixel values based on the values of the black levels
- applying multiplication to all the pixel values based on digital gain

table 4-4 BLC_L control registers

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0xF8	RW	Bit[7]: offset_trig_en Bit[6]: exp_trig_en Bit[5]: gain_trig_en Bit[4]: fmt_trig_en Bit[3]: rst_trig_en Bit[2]: man_trig_en Bit[1]: blc_freeze Bit[0]: blc_always_update
0x4001	BLC CTRL01	0x07	RW	Bit[7]: r_gain_chg_mf_mode Bit[6]: r_fmt_chg_mf_mode Bit[5]: r_off_chg_mf_mode Bit[4]: r_rst_mf_mode Bit[3]: r_man_avg_en Bit[2]: r_gain_chg_mf_en Bit[1]: r_fmt_chg_mf_en Bit[0]: r_off_chg_mf_en
0x4010	BLC CTRL10	0xE8	RW	Bit[7]: zero_ln_out_en Bit[6]: blk_ln_out_en Bit[5]: dither_en Bit[4]: realgain_cmp_en Bit[3]: median_filter_en Bit[2]: disable_target_adjust Bit[1]: manually_set_hsize Bit[0]: manually_set_ln_num
0x4019	BLK LVL TARGET	0x00	RW	Bit[1:0]: blk_lvl_target[9:8]
0x401A	BLK LVL TARGET	0x40	RW	Bit[7:0]: blk_lvl_target[7:0]

table 4-5 BLC_M control registers

address	register name	default value	R/W	description
0x4900	BLC CTRL00	0xF8	RW	Bit[7]: offset_trig_en Bit[6]: exp_trig_en Bit[5]: gain_trig_en Bit[4]: fmt_trig_en Bit[3]: rst_trig_en Bit[2]: man_trig_en Bit[1]: blc_freeze Bit[0]: blc_always_update
0x4901	BLC CTRL01	0x07	RW	Bit[7]: r_gain_chg_mf_mode Bit[6]: r_fmt_chg_mf_mode Bit[5]: r_off_chg_mf_mode Bit[4]: r_rst_mf_mode Bit[3]: r_man_avg_en Bit[2]: r_gain_chg_mf_en Bit[1]: r_fmt_chg_mf_en Bit[0]: r_off_chg_mf_en
0x4910	BLC CTRL10	0xE8	RW	Bit[7]: zero_ln_out_en Bit[6]: blk_ln_out_en Bit[5]: dither_en Bit[4]: realgain_cmp_en Bit[3]: median_filter_en Bit[2]: disable_target_adjust Bit[1]: manualy_set_hsize Bit[0]: manualy_set_ln_num
0x4919	BLK LVL TARGET	0x00	RW	Bit[1:0]: blk_lvl_target[9:8]
0x491A	BLK LVL TARGET	0x40	RW	Bit[7:0]: blk_lvl_target[7:0]

table 4-6 BLC_S control registers

address	register name	default value	R/W	description
0x4A00	BLC CTRL00	0xF8	RW	Bit[7]: offset_trig_en Bit[6]: exp_trig_en Bit[5]: gain_trig_en Bit[4]: fmt_trig_en Bit[3]: rst_trig_en Bit[2]: man_trig_en Bit[1]: blc_freeze Bit[0]: blc_always_update
0x4A01	BLC CTRL01	0x07	RW	Bit[7]: r_gain_chg_mf_mode Bit[6]: r_fmt_chg_mf_mode Bit[5]: r_off_chg_mf_mode Bit[4]: r_rst_mf_mode Bit[3]: r_man_avg_en Bit[2]: r_gain_chg_mf_en Bit[1]: r_fmt_chg_mf_en Bit[0]: r_off_chg_mf_en
0x4A10	BLC CTRL10	0xE8	RW	Bit[7]: zero_ln_out_en Bit[6]: blk_ln_out_en Bit[5]: dither_en Bit[4]: realgain_cmp_en Bit[3]: median_filter_en Bit[2]: disable_target_adjust Bit[1]: manualy_set_hsize Bit[0]: manualy_set_ln_num
0x4A19	BLK LVL TARGET	0x00	RW	Bit[1:0]: blk_lvl_target[9:8]
0x4A1A	BLK LVL TARGET	0x40	RW	Bit[7:0]: blk_lvl_target[7:0]

4.5 one-time programmable (OTP) memory

The OV64B40 supports a maximum of 2048 bytes of one-time programmable (OTP) memory to store chip identification and manufacturing information, which can be used to update the sensor's default setting, and can be controlled through the SCCB (see **table 4-7**).

OTP loading data can be triggered when powering up or when writing 0x01 to register 0x3D81. Power up loading data is enabled by register bit 0x3D85[3], which by default is on. Auto mode and manual mode can be chosen by setting register bit 0x3D84[6] to 0 and 1, respectively, and by default, it is in auto mode. In auto mode, all data in the OTP will be loaded to the OTP buffer. While in manual mode, part of the data, which is defined by start address ({0x3D88, 0x3D89}) and end address ({0x3D8A, 0x3D8B}).

The OV64B40 supports two consecutive sections of OTP_DPC clusters programmed in OTP memory. If OTP memory is in that case, the sorting function should be enabled by register bit 0x3D85[7], which by default is off. The first section of the OTP_DPC cluster start address {0x3DAA, 0x3DAB}, second section of the OTP_DPC cluster start address {0x3DAC, 0x3DAD}, and also the OTP_DPC cluster end address {0x3DAE, 0x3DAF} should be configured.

OTP data can be loaded from 0x7000 to 0x77FF through the SCCB interface.

The OTP memory access conditions are based on typical conditions: sensor wakeup, 2.7~2.9V AVDD, 1.1V DVDD, and 212 MHz system clock.

Set register bit 0x5000[2] to 0 before any OTP access to avoid timing conflict, which may cause OTP read/write failure. After OTP access is complete, set register bit 0x5000[2] back to 1.

OTP write in partial mode example:

```
6C 0103 01
6C 3D84 40; [6]partial mode enable
6C 3D85 1B
6C 0100 01
6C 3D88 70 ;; partial mode OTP write start address high byte
6C 3D89 00 ;; partial mode OTP write start address low byte
6C 3D8A 71 ;; partial mode OTP write end address high byte
6C 3D8B FF ;; partial mode OTP write end address low byte
           ;; It is 71FF in this example
6C 7000 xx ;; Data[0]
6C 7001 xx ;; Data[1]
6C 7002 xx ;; Data[2]
6C 7003 xx ;; Data[3]
6C 7004 xx ;; Data[4]
…
6C 71FF xx ;; Data[511]
6C 3D80 01 ;[0] program enable
```

OTP read example:

```
6C 0103 01
6C 3D84 00 ;[6] partial mode enable
6C 3D85 1B
           ;[3] power up load data enable
           ;[1] power up load setting enable
           ;[0] write reg load setting enable
6C 0100 01 ;resume from sleep
           ;read 7000 - 77FF
```

To use OTP memory under different operating conditions, please contact your local OmniVision FAE.

table 4-7 OTP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3D80	R PGM CTR	–	R	Bit[7]: otp_pgenb_n
0x3D81	R LOAD CTR	–	R	Bit[7]: otp_load Bit[6]: Not used Bit[5]: otp_bist_err Bit[4]: otp_bist_done Bit[0]: otp_rd
0x3D82	R PGM PULSE	0x7D	RW	Bit[7:0]: contrl_prgram_strbe_pulse by 16*Tsclk
0x3D83	R LOAD PULSE	0x10	RW	Bit[4:0]: contrl_load_strbe_pulse by 2*Tsclk
0x3D84	R MODE CTRL	0x1C	RW	Bit[7]: pgm_dis Bit[6]: manu_mode_en Bit[4]: Update load setting 1: Update dpc1_st_adr by load setting Bit[3]: 14-bit hsize for DPC sort feature Bit[2]: Select SMIC or TSMC 0: SMIC 1: TSMC Bit[1]: Clock switch select 1: otp_sram clock will switch to reg_bus clock Bit[0]: bank_sram_switch
0x3D85	R REG85	0x0B	RW	Bit[7]: dpc_sort_en Bit[6]: otp_bist_comp_val Bit[5]: Compare select 0: Compare with SRAM 1: Compare with 0/1 Bit[4]: otp_bist_en Bit[3]: pwup_load_en Bit[2]: wkup_load_en Bit[1]: hw_ld_setting_en Bit[0]: sw_ld_setting_en

table 4-7 OTP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3D86	SRAM TEST SIGNALS	0x11	RW	Bit[7:0]: RAMS[15:8]
0x3D87	R PS2CS	0x30	RW	Bit[7:0]: RAMS[7:0]
0x3D88	R STT PT H	0x00	RW	Bit[7:0]: start_addr_for_manu_mode[15:8]
0x3D89	R STT PT L	0x00	RW	Bit[7:0]: start_addr_for_manu_mode[7:0]
0x3D8A	R END PT H	0x03	RW	Bit[7:0]: end_addr_for_manu_mode[15:8]
0x3D8B	R END PT L	0xFF	RW	Bit[7:0]: end_addr_for_manu_mode[7:0]
0x3D8C	R SETTING ADR STT PT H	0x00	RW	Bit[7:0]: start_addr_for_load_setting[15:8]
0x3D8D	R SETTING ADR STT PT L	0x10	RW	Bit[7:0]: start_addr_for_load_setting[7:0]
0x3D8E	OTP BIST ERR ADR H	–	R	Bit[7:0]: otp_bist_err_adr[15:8]
0x3D8F	OTP BIST ERR ADR L	–	R	Bit[7:0]: otp_bist_err_adr[7:0]
0x3D90	R BASE ADR H	0x00	RW	Bit[7:0]: efuse_base_address[15:8]
0x3D91	R BASE ADR L	0x00	RW	Bit[7:0]: efuse_base_address[7:0]
0x3D92	PGENB TIMING	0x1F	RW	Bit[7:4]: t_pgenb_end Bit[3:0]: t_pgenb_start
0x3D93	VDDQ TIMING	0x46	RW	Bit[7:4]: t_vddq_end Bit[3:0]: t_vddq_start
0x3D94	OTP STRBE GAP PGM	0x04	RW	Bit[7:0]: Gap between strobe pulse when programming
0x3D95	OTP STRBE GAP LOAD	0x05	RW	Bit[3:0]: Gap between strobe pulse when loading
0x3D96	SRAM RM	0x0F	RW	Bit[3:0]: ps_to_csb_time_control by 16*Tsclk
0x3D97	AEN SETUP HOLD TIME	0x0F	RW	Bit[4:0]: AEN to RDEN/PGMEN setup and hold time by 2*Tsclk
0x3D98	A HOLD TIME	0x62	RW	Bit[7:4]: A to AEN hold when programming by 2*Tsclk Bit[3:0]: A to AEN hold when loading by 2*Tsclk
0x3DA4	SLOPE REG	0x24	RW	Bit[7:2]: slope_end Bit[1:0]: slope_sreg
0x3DAA	R DPC 1ST STT ADR H	0x00	RW	Bit[7:0]: first_dpc_start_adr[15:8]

table 4-7 OTP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3DAB	R DPC 1ST STT ADR L	0x00	RW	Bit[7:0]: first_dpc_start_adr[7:0]
0x3DAC	R DPC 2ND STT ADR H	0x00	RW	Bit[7:0]: second_dpc_start_adr[15:8]
0x3DAD	R DPC 2ND STT ADR L	0x00	RW	Bit[7:0]: second_dpc_start_adr[7:0]
0x3DAE	R DPC END ADR H	0x00	RW	Bit[7:0]: dpc_end_adr[15:8]
0x3DAF	R DPC END ADR L	0x00	RW	Bit[7:0]: dpc_end_adr[7:0]

4.6 temperature sensor

The OV64B40 supports an on-chip temperature sensor that covers -64°C to +192°C with an error up to 5°C. It can be controlled through the SCCB interface (see **table 4-8**).

When the readout data is lower than 0xC0, the temperature is a positive value. If the readout data is higher than 0xC0, the temperature is lower than 0°C and the readout data is two's complement code. Before reading the temperature, the temperature sensor should be triggered by a 0 to 1 transition of register bit 0x4D12[0].

table 4-8 temperature sensor functions

address	register name	default value	R/W	description
0x4D12	TPM_CTRL_12	–	W	Writing register bit 0x4D12[0] to '1' will trigger temperature calculation, then registers 0x4D12 and 0x4D13 will be latched temperature value
0x4D13	TPM_CTRL_13	–	R	Latched Temperature Value, Integer Part

4.7 strobe flash

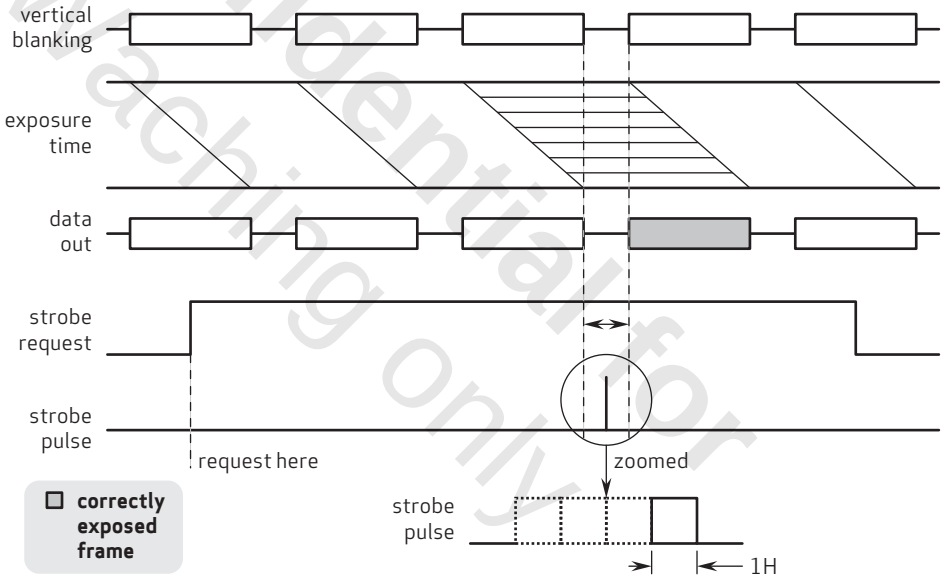
4.7.1 strobe flash control

The strobe signal is programmable using register bits 0x3C80[2:0]. It supports both LED and xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. The OV64B40 supports the following flashing modes: xenon flash control, LED mode 1, LED mode 2, LED mode 3, and LED mode 4. Strobe trigger point can be controlled by register bits 0x3C84[5:4]. If register bits 0x3C84[5:4] is 2'b00, the trigger point is the end of stream. If register bits 0x3C84[5:4] is 2'b10, the trigger point is the end of pre-charge.

4.7.1.1 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 4-6**). The third frame will be correctly exposed. The pulse width can be changed in xenon mode between 1H and 4H, and controlled by register bits 0x3C80[5:4], where H is one row period.

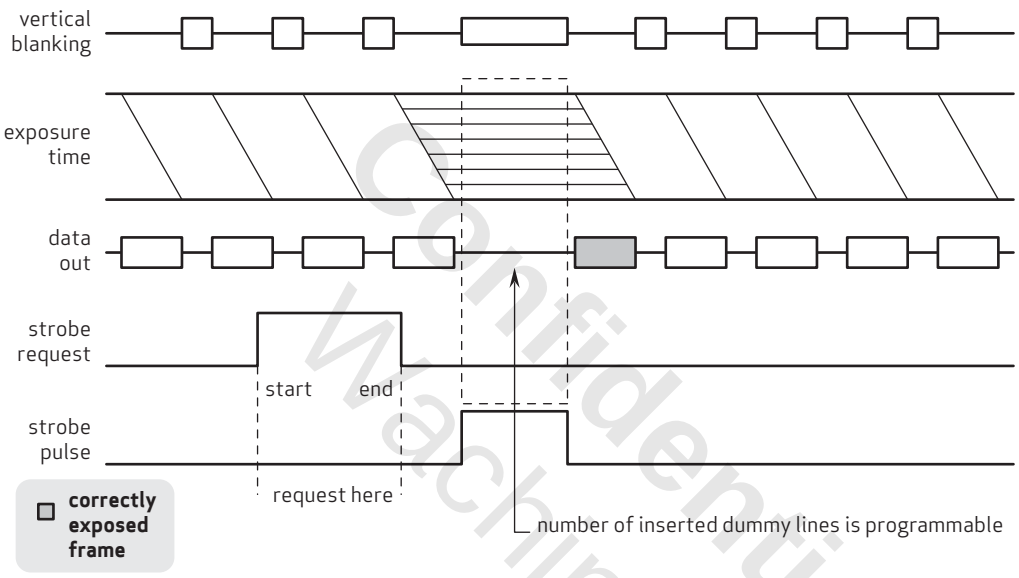
figure 4-6 xenon flash mode



4.7.1.2 LED 1 & 2 mode

In LED 1 & 2 modes, the strobe pulse is active two frames after the strobe request is submitted and the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set as shown in **figure 4-7**. If end request has not been sent, the strobe signal is activated intermittently until the strobe end request is set (see **figure 4-8**). The strobe width is programmable.

figure 4-7 LED 1 and 2 mode - one pulse output

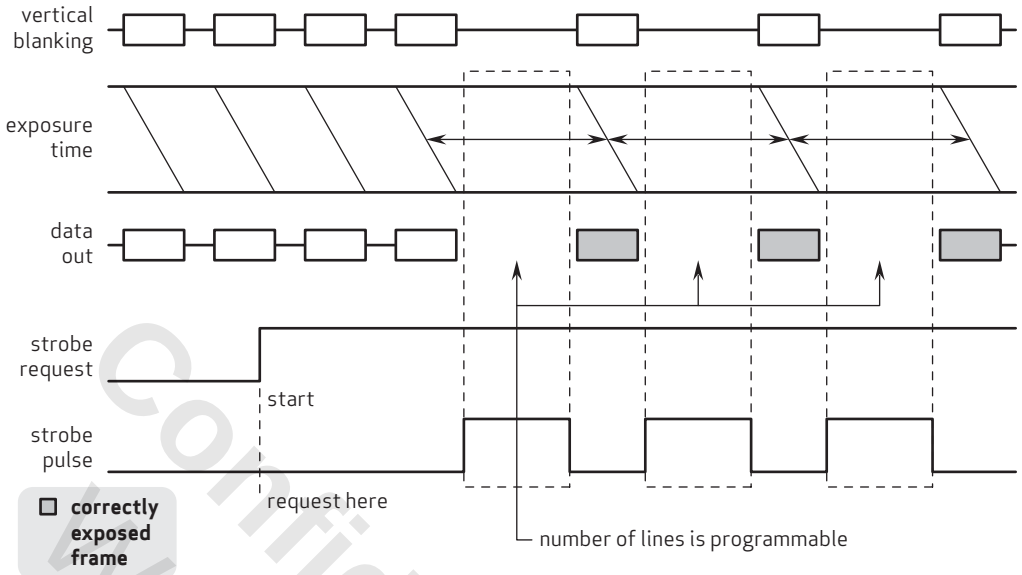


The strobe width is controlled by registers 0x3C82 and 0x3C83. The inserted dummy lines are used for the additional exposure lines added to 0x3501~0x3502. The maximum line of 0x3C82 and 0x3C83 is calculated by 0xFFFF0 - (0x3501, 0x3502).

Example of LED 1 & 2 mode:

```
6C 3C80 01 ;Select LED 1 mode
6C 3C82 00 ;Set strobe width
6C 3C83 3F ;Set strobe width
6C 3002 80 ;Set VSYNC output enable
6C 3C80 81 ;Request on
;delay 100 ;if using LED 2 mode
6C 3C80 00 ;Request off
```

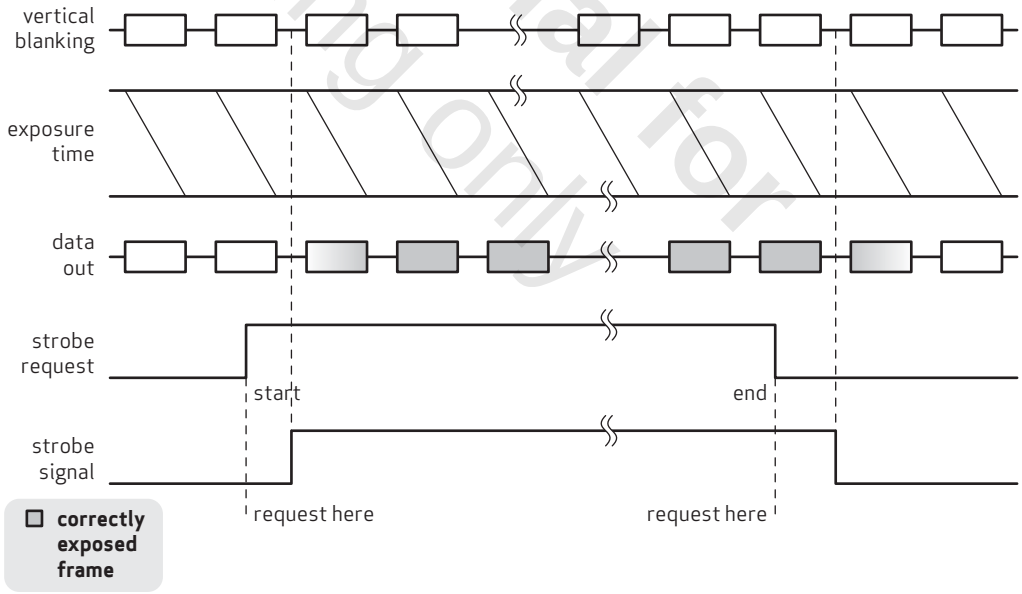
figure 4-8 LED 1 and 2 mode - multiple pulse output



4.7.1.3 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see **figure 4-9**).

figure 4-9 LED 3 mode



4.7.1.4 LED 4 mode

In LED 4 mode, the strobe signal width is controlled by register 0x3C85 (see **figure 4-10**). Strobe width = 128 × (2^0x3C85[1:0]) × (0x3C85[7:2] + 1) × sclk_period. The maximum value of 0x3C85[7:2] is 6'b111110.

figure 4-10 LED 4 mode

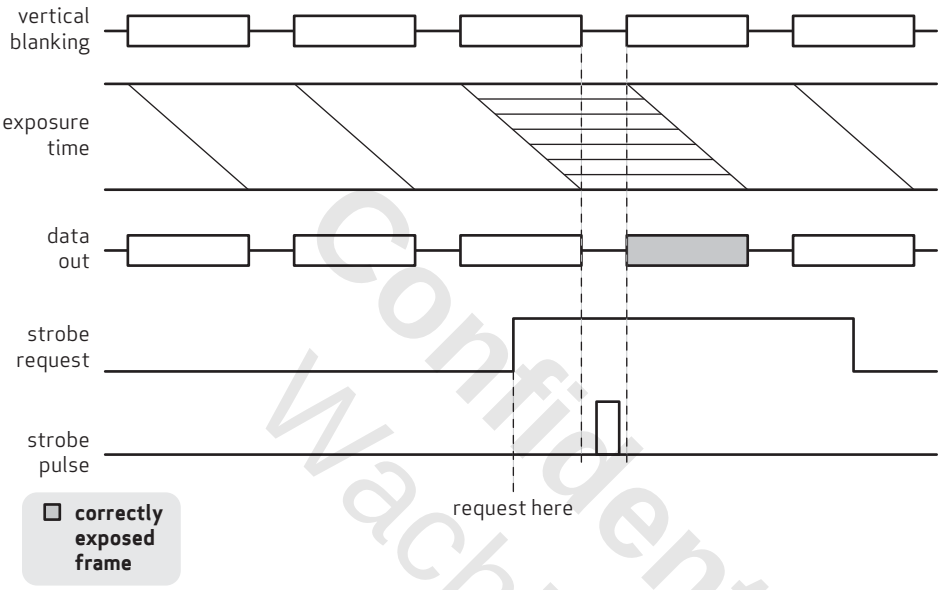


table 4-9 flash strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3C80	RSTRB	0x00	RW	Bit[7]: Strobe on/off Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: width_in_xenon Bit[2:0]: Strobe mode 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3C82	STROBE ADD DUMMY	0x00	RW	Bit[7:0]: Dummy line number added at strobe[15:8]
0x3C83	STROBE ADD DUMMY	0x00	RW	Bit[7:0]: Dummy line number added at strobe[7:0]

table 4-9 flash strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3C84	STROBE CTRL1	0x00	RW	Bit[5:4]: start_point_sel 00: SOF 01: end_of_sample 10: end_of_precharge Bit[3]: strobe_md4_repeat Bit[2]: strobe_repeat_enable Bit[1:0]: strobe_lantency 00: Strobe generated at next frame 01: Delay one frame, strobe generated 2 frames later 10: Delay one frame, strobe generated 3 frames later 11: Delay one frame, strobe generated 4 frames later
0x3C85	STROBE WIDTH	0x00	RW	Bit[7:2]: strobe_pulse_width_step Bit[1:0]: strobe_pulse_width_gain strobe_pulse_width = 128 × (2^gain) × (step+1) × sclk_period

4.8 embedded line

In the OV64B40, the user can configure the registers being output in embedded line. The embedded data contains the values of a programmable list of registers to describe the current state of the sensor (e.g., frame counter, exposure time and gain, etc.). One row of embedded data can be output at the beginning or end of image frame. In total, embedded line can support up to 2048 bytes of data. **table 4-11** and **table 4-12** show the structure of the outputted image when embedded (both front and end) data is enabled for non-staggered or staggered HDR mode.

figure 4-11 image output, non-staggered HDR

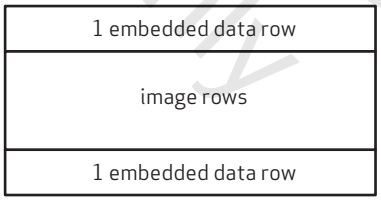
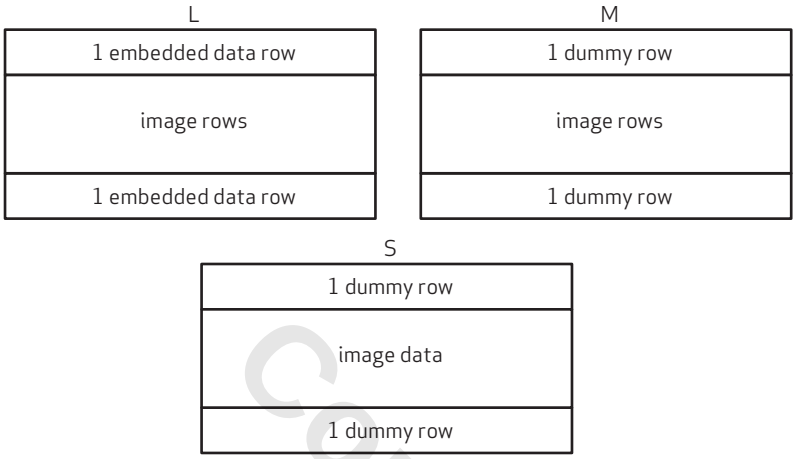


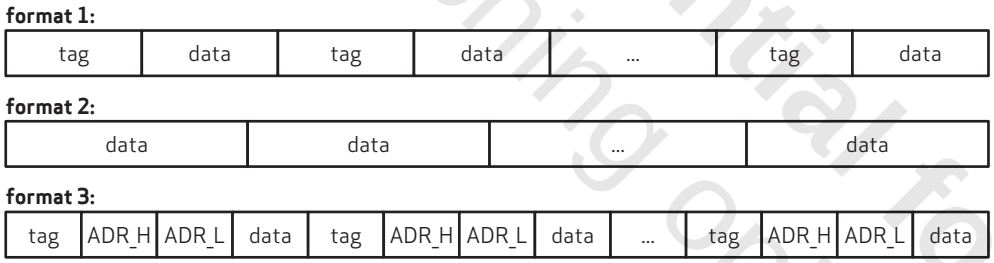
figure 4-12 image output, 2 or 3-staggered HDR



4.8.1 embedded data format at output

The valid data is from the embedded row in the long exposure image. Dummy data is inserted in the embedded row in medium and short exposure images. This mode has three data formats as shown in **figure 4-13**.

figure 4-13 three data formats



tag: 8-bit, set by register 0x3219[7:0], default is 8'h55

data: effective embedded data

ADR_H: high byte of the address of the following embedded data

ADR_L: low byte of the address of the following embedded data

The first two modes are selected by register bit 0x369F[1], 1'b0 for format 2 and 1'b1 for format 1. Mode 3 is enabled by register bit 0x369F[0] = 1.

4.8.2 embedded line setup

This setup outputs embedded line data in front of or at the end of frame.

```
6C 3685 EB ;
6C 369F 03 ; [2]: 0, no mirror; [1]: 1, tag+data; [0]: 1, output emb_adr
6C 3216 01
6C 3218 27 ;[5] embline_adr_en; [2] emb_sof_en; [1] emb_eof_en; [0] emb_tag_en
6C 368A C0 ;[7] emb_front_en; [6] emb_end_en
6C 3208 04 ;embedded line record
6C 387E 03 ;frame cnt registers
6C 5000 04
6C 4800 02
6C 3208 14
6C 3208 05
6C 387E 03
6C 5000 04
6C 4800 02
6C 3208 15 ;embedded line end
```

4.8.3 embedded line output

Embedded line is output in front of or at the end of the image line. Valid embedded line content width is programmable. Invalid embedded line content is fixed and filled with dummy data from one programmable byte controlled by register 0x3217. Embedded line supports tag and no tags. Tag value is programmable, and controlled by register 0x3219.

table 4-10 embedded line registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3685	CORE_5	0x12	RW	Bit[7]: Embedded line enable Bit[6]: Embedded line LSB enable Bit[5:0]: Embedded line data byte
0x368A	CORE_10	0xEE	RW	Bit[5]: r_eof_opt Select EOF from window Bit[4]: r_pd_eof_img Select PD EOF from image EOF Bit[3]: r_sof_from_win Select SOF from window Bit[2]: r_sof_en Ripple SOF enable Bit[1]: r_eof_en Ripple EOF enable Bit[0]: r_eof_sel Option to select L/M/S EOF from pipeline delayed EOF
0x3216	EMB LINE NUM	0x01	RW	Bit[3:0]: emb_line_num

table 4-10 embedded line registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3217	PADDING DATA	0x00	RW	Bit[7:0]: padding_data
0x3218	R16	0x00	RW	Bit[7:6]: emb_line_blk_ctrl 00: 32 SCLK 01: 64 SCLK 10: 128 SCLK 11: Wait for external trigger signal Bit[5]: embline_addr_en Bit[4]: r_padding_md2 0: No dummy data mixing with valid data 1: Dummy data output with valid data every cycle Bit[3]: frame_trig_sel 0: tc_grp_wr 1: EOF Bit[2]: embline_eof_en Bit[1]: embline_sof_en Bit[0]: embline_tag_en
0x3219	TAG DATA	0x55	RW	Bit[7:0]: emb_tag

5 image sensor processor digital functions

5.1 DSP general description

The OV64B40 ISP has the following work modes:

- 4-cell full mode
- 4-cell binning mode
- 4-cell binning + stagger HDR 2-exposure mode
- 4-cell binning + stagger HDR 3-exposure mode

The ISP receives image data from the sensor array, which includes modules for RAW image processing. The video stream arrives as 10-bit parallel data separated into long exposure (L), medium exposure (M), and very short (VS) exposure channels. After processing the data from the ISP, it is configured to the correct output format in the output interface.

One of the first processing steps in the ISP (whether or not any of the available digital test patterns are enabled) is digital gain. Digital gain is applied to make an image white balanced (WB gain). Defect pixel and clusters (DPC) are corrected on-the-fly for each capture. At the end, image windowing is performed, if enabled.

figure 5-1 4C full mode block diagram

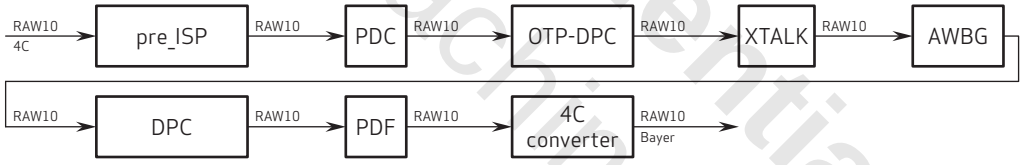


figure 5-2 4C bin mode block diagram

5.2 PD and ISP features

5.2.1 PD features

- supports 2x2 MLPD
- PD compensation (PDC)
- PD correction (PDF) and PD write back

5.2.2 image process features

- test pattern
- manual WB gain (MWB)
- XTALK
- OTP_DPC
- DPC
- RAW binning (RAW_BIN)
- FourCell2Bayer converter

5.3 pre_ISP

Pre_ISP provides the following functions:

- test pattern (color bar) for ISP data path

For testing mode (register bit 0x50C1[0] = 1'b1 for long, 0x53C1[0] = 1 for medium, 0x56C1[0] = 1 for short), the pre_ISP offers four color bar patterns controlled by register bits 0x50C1[5:4] for long, 0x53C1[5:4] for medium, and 0x56C1[5:4] for short. It also offers a color bar test pattern with transparent effect and rolling bar effect controlled by register bits 0x50C1[3:2] for long, 0x53C1[3:2] for medium, and 0x56C1[3:2] for short.

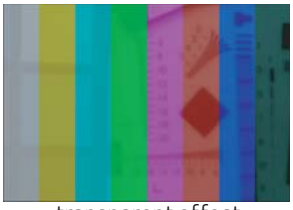
figure 5-3 pre_ISP test patterns

Rolling bar effect is enabled by setting register bit 0x50C1[2] high for long, register bit 0x53C1[2] high for medium, and register bit 0x56C1[2] high for short.

Transparent effect is enabled by setting register bit 0x50C1[3] high for long, register bit 0x53C1[3] high for medium, and register bit 0x56C1[3] for short.

figure 5-4 rolling bar and transparent effects

rolling effect
(0x50C1[2]=1'b1)



transparent effect
(0x50C1[3]=1'b1)

5.4 PD compensation

PD compensation compensates for the PD pixels, which is enabled by register bit 0x5000[1]. The fading list for compensation is stored in SRAM, mapping to 0x5F80~0x651F. It needs to be initialized after power on before use. Please note, to avoid timing conflict, PD fading list can be accessed either in sleep mode or PDC disable condition only.

5.5 WB gain

White balance (referred to as WB) is the process of removing unrealistic color casts, so that objects, which appear white in person, are rendered white in the photo.

This manual white balance (referred to as MWB) algorithm is designed to compensate the effects of changing spectra of the scene illumination on the quality of the color rendition. Manual white balance is enabled by register bit 0x5000[4]. Manual mode configuration is in registers 0x5100~0x5107 for L, 0x5400~0x5407 for M, and 0x5700~0x5707 for S.

table 5-1 gain register descriptions (sheet 1 of 2)

pixel	exposure	gain registers
B	long	nManualAWBGain_0 {0x5100, 0x5101}
Gb	long	nManualAWBGain_1 {0x5102, 0x5103}
Gr	long	nManualAWBGain_2 {0x5104, 0x5105}
R	long	nManualAWBGain_3 {0x5106, 0x5107}
B	medium	nManualAWBGain_0 {0x5400, 0x5401}
Gb	medium	nManualAWBGain_1 {0x5402, 0x5403}
Gr	medium	nManualAWBGain_2 {0x5404, 0x5405}
R	medium	nManualAWBGain_3 {0x5406, 0x5407}

table 5-1 gain register descriptions (sheet 2 of 2)

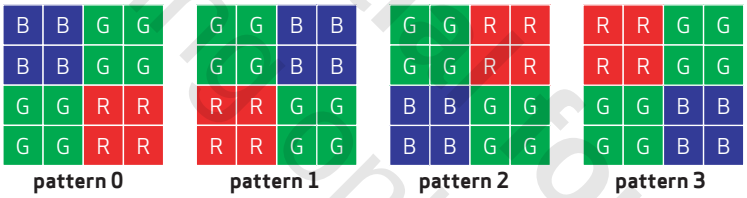
pixel	exposure	gain registers
B	short	nManualAWBGain_0 {0x5700, 0x5701}
Gb	short	nManualAWBGain_1 {0x5702, 0x5703}
Gr	short	nManualAWBGain_2 {0x5704, 0x5705}
R	short	nManualAWBGain_3 {0x5706, 0x5707}

The RAW R, G, B values vary with the light source spectrum and the pixel QE spectrum response. Light source spectrum is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, the light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is about 2850K, while the color temperature of an overcast day is surprisingly high.

To make sure the gray image is gray in the image regardless of the light spectrum, the sensor needs to adjust the gain for each channel with color temperature. This process is called white balance (WB).In the WB module, different WB gains are applied to B/Gb/Gr/R channels of the long (L), medium (M), and short (S) exposure RAW images. In the WB module, different WB gains are applied to B/Gb/Gr/R channels of the long (L), medium (M), and short (S) exposure RAW images.

There are four patterns for the RAW format image. The R, G, B pixel array is different in each pattern. Four gain channels should be adjusted to fit for the fixed pattern.

figure 5-5 pixel pattern



5.6 PD correction

PD correction is used to correct the PD pixels in the image. It is enabled by register bit 0x5001[0] and register bit 0x51D0[6] for long, register bit 0x54D0[6] for medium, and register bit 0x57D0[6] for short.

5.7 DPC

Defect pixels are defined as the pixels with high possibility to be brighter or darker than its neighboring pixels, which includes both dead pixels and wounded pixels. When sensor gain exposure time or temperature increases, there are more defect pixels.

Defect pixel cancellation (DPC) is an online defect pixel detection and correction algorithm.

DPC is enabled by setting DPCEnable (register bit 0x5000[6]). The defect black pixel cancellation and defect white pixel cancellation are controlled by BlackPixel (register bit 0x5152[1] for long, 0x5452[1] for medium, 0x5752[1] for short) and WhitePixel (register bit 0x5152[0] for long, 0x5452[0] for medium, 0x5752[0] for short).

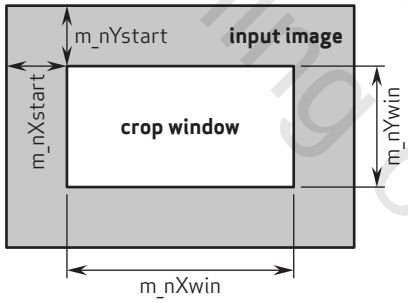
5.8 window

The window module can crop an output image by any size. These control signals can be both automatically generated and manually set by registers.

In manual mode (register bit 0x4288[3] = 1'b1), Xstart (registers {0x4280, 0x4281}) is used to define horizontal start point, Ystart (registers {0x4282, 0x4283}) is used to define vertical start point. Note that horizontal start and vertical start points can be any number.

Xwin (registers {0x4284, 0x4285}) and Ywin (registers {0x4286, 0x4287}) are used to define width and height of the output image.

figure 5-6 crop window definitions



6 register tables

The following tables provide descriptions of the device control registers contained in the OV64B40. For all register enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read when {SID2, SID} = 0x00 (when {SID2, SID} = 0x01, 0x20 for write and 0x21 for read; when {SID2, SID} = 0x02, 0x44 for write and 0x45 for read; when {SID2, SID} = 0x03, 0x46 for write and 0x47 for read).

6.1 module name and address range

table 6-1 module name and address range (sheet 1 of 3)

module name	address range
PLL_CTRL	0x0300~0x0361
SC_CMMN_REG	0x3000~0x3048
SCCB	0x3100~0x3108
GROUP_HOLD	0x3200~0x3245
PSV_CTRL	0x3400~0x3429
AEC_PK_L	0x3500~0x353D
AEC_PK_M	0x3540~0x3578
AEC_PK_S	0x3580~0x35BF
ANALOG_REG	0x3600~0x365B
CORE_REG	0x3680~0x36C1
SENSOR_REG	0x3700~0x37FF
TIMING_CTRL	0x3800~0x38F2
SENSOR_REG1	0x3900~0x3A7D
STROBE	0x3C80~0x3C85
OTP_SC	0x3D80~0x3DAF
SENSOR_FREX	0x3F85~0x3F9F
BLC_L	0x4000~0x40EF
BLC_M	0x4900~0x49EF
BLC_S	0x4A00~0x4AEF
FC	0x4200~0x4203
ISP_FC	0x4220~0x4223
WINDOW	0x4280~0x429B
TEST_MODE	0x4300~0x4314

table 6-1 module name and address range (sheet 2 of 3)

module name	address range
DATA_SYNC	0x4500~0x4547
LR_PIPE_STITCH	0x4580~0x458B
LR_PD_STITCH	0x45C0~0x45CB
VFIFO	0x4600~0x460D
PD_FIFO	0x4640~0x464F
MIPI_CORE	0x4800~0x487A, 0x48C0~0x48C5
MIPI_PHY	0x4880~0x488A
TPM	0x4D00~0x4D23
ISP_TOP	0x5000~0x50B7
PRE_ISP_L	0x50C0~0x50E7
AWBG_L	0x50F0~0x5107
OTP_L	0x5110~0x5141
DPC_L	0x5150~0x5177
RAW_BIN_L	0x5180~0x518D
BINC_L	0x51B0~0x51C7
PDF_L	0x51D0~0x521B
PDC_L	0x5250~0x534C
RAW_DNS_L	0x5350~0x535F
PRE_ISP_M	0x53C0~0x53E7
AWBG_M	0x53F0~0x5407
OTP_M	0x5410~0x5441
DPC_M	0x5450~0x5477
RAW_BIN_M	0x5480~0x548D
BINC_M	0x54B0~0x54C7
PDF_M	0x54D0~0x551B
PDC_M	0x5550~0x564C
RAW_DNS_M	0x5650~0x565F
PRE_ISP_S	0x56C0~0x56E7
AWBG_S	0x56F0~0x5707
OTP_S	0x5710~0x5741

table 6-1 module name and address range (sheet 3 of 3)

module name	address range
DPC_S	0x5750~0x5777
RAW_BIN_S	0x5780~0x578C
BINC_S	0x57B0~0x57C7
PDF_S	0x57D0~0x581B
PDC_S	0x5850~0x594C
RAW_DNS_S	0x5950~0x595F
4CC	0x5980~0x59DB
XTC	0x5A00~0x5A17
XTC_1C	0x5A40~0x5B5F
XTC_3C	0x5B80~0x5EDF
PDF_33	0x5F00~0x5F43
PDC_FD_LIST	0x5F80~0x651F
DPD	0x6520~0x652F

6.2 PLL_CTRL [0x0300 - 0x0361]

table 6-2 PLL_CTRL registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x0300	PLL_CTRL_0	0x02	RW	Bit[7:4]: Not used Bit[3]: pll1_bp_vco_sync Bit[2]: pll1_rst Bit[1]: pll1_dither_en Bit[0]: pll1_bypass
0x0301	PLL_CTRL_1	0x40	RW	Bit[7]: pll1_divs Bit[6]: pll1_predivp Bit[5:4]: Not used Bit[3]: pll1_divpix Bit[2:0]: Not used
0x0302	PLL_CTRL_2	0x33	RW	Bit[7:6]: Not used Bit[5]: pll1_div_rst_sync_en Bit[4]: pll1_bias_ext Bit[3:0]: pll1_cp

table 6-2 PLL_CTRL registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x0303	PLL_CTRL_3	0x03	RW	Bit[7:5]: Not used Bit[4]: pll1_vco_postdiv Bit[3]: Not used Bit[2:0]: pll1_prediv
0x0304	PLL_CTRL_4	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pll1_divp[9:8]
0x0305	PLL_CTRL_5	0xB5	RW	Bit[7:0]: pll1_divp[7:0]
0x0306	PLL_CTRL_6	0x03	RW	Bit[7:3]: Not used Bit[2:0]: pll1_divmipi
0x0307	PLL_CTRL_7	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pll1_divm
0x0308	PLL_CTRL_8	0x02	RW	Bit[7:2]: Not used Bit[1:0]: pll1_divsp
0x0309	PLL_CTRL_9	0x51	RW	Bit[7:6]: pll1_precision Bit[5:4]: pll1_cnt_ref Bit[3:2]: Reserved Bit[1]: pll1_lock_det_en Bit[0]: pll1_en_extl
0x030A~ 0x030F	NOT USED	–	–	Not Used
0x0310	PLL_CTRL_16	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pll1_cntstep[3:0]
0x0311	PLL_CTRL_17	0x00	RW	Bit[7:3]: Not used Bit[2]: pll1_frac_en Bit[1]: pll1_cntstep_3x Bit[0]: pll1_sscg_en
0x0312	PLL_CTRL_18	0x07	RW	Bit[7:3]: Not used Bit[2:0]: pll1_cntck
0x0313	PLL_CTRL_19	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pll1_dsm[19:16]
0x0314	PLL_CTRL_20	0x00	RW	Bit[7:0]: pll1_dsm[15:8]
0x0315	PLL_CTRL_21	0x00	RW	Bit[7:0]: pll1_dsm[7:0]
0x0316	PLL_CTRL_22	0x33	RW	Bit[7]: Not used Bit[6]: pll1_bias_sel_mipi Bit[5:3]: pll1_lpf_r Bit[2]: Band selection Bit[1]: pll1_exti_cp Bit[0]: PLL1 speed up enable
0x0317~ 0x031F	NOT USED	–	–	Not Used

table 6-2 PLL_CTRL registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x0320	PLL_CTRL_32	0x12	RW	Bit[7]: pll2_bp_vco_sync Bit[6]: pll2_sel_bak_divs Bit[5]: pll2_sel_bak_sa1 Bit[4]: pll2_en_extl Bit[3]: Reserved Bit[2]: pll2_rst Bit[1]: pll2_div_rst_sync_en Bit[0]: pll2_bypass
0x0321	PLL_CTRL_33	0x01	RW	Bit[7:4]: Not used Bit[3:0]: pll2_cp
0x0322	PLL_CTRL_34	0x53	RW	Bit[7:6]: pll2_precision Bit[5:4]: pll2_cnt_ref Bit[3:2]: Not used Bit[1]: pll2_lock_det_en Bit[0]: Not used
0x0323	PLL_CTRL_35	0x05	RW	Bit[7:3]: Not used Bit[2:0]: pll2_prediv
0x0324	PLL_CTRL_36	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pll2_divp[9:8]
0x0325	PLL_CTRL_37	0xD0	RW	Bit[7:0]: pll2_divp[7:0]
0x0326	PLL_CTRL_38	0xCB	RW	Bit[7]: pll2_predivp Bit[6]: pll2_bias_ext Bit[5]: pll2_sa1_clk_sel Bit[4]: sa1_post_div 0: 1+r_div_sa1[3:0] 1: 2*(1+r_div_sa1[3:0]) Bit[3:0]: 1+r_div_sa1[3:0]
0x0327	PLL_CTRL_39	0x05	RW	Bit[7:4]: Not used Bit[3:0]: 1+r_divsam
0x0328	NOT USED	–	–	Not Used
0x0329	PLL_CTRL_41	0x01	RW	Bit[7:4]: Not used Bit[3:0]: 1+r_divdac
0x032A	PLL_CTRL_42	0x05	RW	Bit[7:4]: Not used Bit[3:0]: 1+r_div_sys_pre

table 6-2 PLL_CTRL registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x032B	PLL_CTRL_43	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pll2_sys_div 0000: /1 0001: /1.5 0010: /2 0011: /2.5 0100: /3 0101: /3.5 0110: /4 0111: /4.5 1000: /5 1001: /6 1010: /7 1011: /8 1100: /9 1101: /10 111x: /1
0x032C	PLL_CTRL_44	0x00	RW	Bit[7:2]: Not used Bit[1:0]: 1+r_sram_prediv
0x032D	PLL_CTRL_45	0x00	RW	Bit[7:1]: Not used Bit[0]: 1+r_sa1_prediv
0x032E	PLL_CTRL_46	0x00	RW	Bit[7:3]: Not used Bit[2]: plll2_bias_sel_mipi Bit[1]: pll_py2 Bit[0]: 1+r_dac_prediv
0x032F	PLL_CTRL_47	0x10	RW	Bit[7:5]: pll2_lpf_r Bit[4]: pll2_en_exti_cp Bit[3]: dacclk_test_en Bit[2]: Band selection Bit[1]: Half ICP enable Bit[0]: Speed up enable
0x0330~ 0x033F	RSVD	–	–	Reserved
0x0340	PLL_CTRL_64	0x02	RW	Bit[7]: pll3_bp_vco_sync Bit[6]: pll3_sel_bak_divs Bit[5]: pll3_sel_bak_sa1 Bit[4]: pll3_en_extl Bit[3]: Reserved Bit[2]: pll3_rst Bit[1]: pll3_div_rst_sync_en Bit[0]: pll3_bypass
0x0341	PLL_CTRL_65	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll3_cp

table 6-2 PLL_CTRL registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x0342	PLL_CTRL_66	0x53	RW	Bit[7:6]: pll3_precision Bit[5:4]: pll3_cnt_ref Bit[3:2]: Not used Bit[1]: pll3_lock_det_en Bit[0]: Not used
0x0343	PLL_CTRL_67	0x03	RW	Bit[7:3]: Not used Bit[2:0]: pll3_prediv
0x0344	PLL_CTRL_68	0x01	RW	Bit[7:2]: Not used Bit[1:0]: pll3_divp[9:8]
0x0345	PLL_CTRL_69	0x09	RW	Bit[7:0]: pll3_divp[7:0]
0x0346	PLL_CTRL_70	0xCB	RW	Bit[7]: pll3_predivp Bit[6]: pll3_bias_ext Bit[5]: pll3_sa1_clk_sel Bit[4]: sa1_post_div 0: 1+r_div_sa1[3:0] 1: 2*(1+r_div_sa1[3:0]) Bit[3:0]: 1+r_div_sa1[3:0]
0x0347	PLL_CTRL_71	0x07	RW	Bit[7:4]: Not used Bit[3:0]: 1+r_divsam
0x0348	NOT USED	–	–	Not Used
0x0349	PLL_CTRL_73	0x01	RW	Bit[7:4]: Not used Bit[3:0]: 1+r_divdac
0x034A	PLL_CTRL_74	0x05	RW	Bit[7:4]: Not used Bit[3:0]: 1+r_div_sys_pre
0x034B	PLL_CTRL_75	0x00	RW	Bit[7:4]: Not used Bit[3:0]: pll3_sys_div 0000: /1 0001: /1.5 0010: /2 0011: /2.5 0100: /3 0101: /3.5 0110: /4 0111: /4.5 1000: /5 1001: /6 1010: /7 1011: /8 1100: /9 1101: /10 111x: /1
0x034C	PLL_CTRL_76	0x00	RW	Bit[7:2]: Not used Bit[1:0]: 1+r_sram_prediv

table 6-2 PLL_CTRL registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x034D	PLL_CTRL_77	0x00	RW	Bit[7:1]: Not used Bit[0]: 1+r_sa1_prediv
0x034E	PLL_CTRL_78	0x00	RW	Bit[7:1]: Not used Bit[0]: 1+r_dac_prediv
0x034F	PLL_CTRL_79	0xB0	RW	Bit[7:1]: Not used Bit[0]: PLL3 speed up enable
0x0350	PLL_CTRL_80	0x02	RW	Bit[7:6]: Reserved Bit[5:3]: srclk_sel Bit[2]: SRCLK option Bit[1]: Pixel clock divide by 2 enable Bit[0]: System clock divide by 2 enable
0x0351~ 0x035F	RSVD	–	–	Reserved
0x0360	PLL_CTRL_96	0x09	RW	Bit[7]: Reserved Bit[6]: lvds_bit_sel_man_en Bit[5:4]: lvds_bit_sel_man Bit[3]: Reserved Bit[2:0]: mipi_bit_sel
0x0361	PLL_CTRL_97	0x00	RW	Bit[7:4]: Not used Bit[3]: pll1_lat_sel Bit[2]: pll3_lat_en Bit[1]: pll2_lat_en Bit[0]: pll1_lat_en

6.3 SC_CMMN_REG [0x3000 - 0x3048]

table 6-3 SC_CMMN_REG registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x3000	RSVD	–	–	Reserved
0x3001	SC_CMMN_1	0x00	RW	Bit[7:2]: Reserved Bit[1]: r_io_pad_oen[9] GPIO3 oen Bit[0]: r_io_pad_oen[8] GPIO2 oen
0x3002	SC_CMMN_2	0x00	RW	Bit[7]: r_io_pad_oen[7] VSYNC oen Bit[6]: r_io_pad_oen[6] HREF oen Bit[5]: Reserved Bit[4]: r_io_pad_oen[4] FREX oen Bit[3]: r_io_pad_oen[3] FSIN oen Bit[2]: Reserved Bit[1]: r_io_pad_oen[1] GPIO1 oen Bit[0]: r_io_pad_oen[0] GPIO0 oen
0x3003	RSVD	–	–	Reserved
0x3004	SC_CMMN_4	0x04	RW	Bit[7:2]: Reserved Bit[1]: r_io_pad_out[9] GPIO3 out Bit[0]: r_io_pad_out[8] GPIO2 out
0x3005	SC_CMMN_5	0x00	RW	Bit[7]: r_io_pad_out[7] VSYNC out control Bit[6]: r_io_pad_out[6] HREF out control Bit[5]: Reserved Bit[4]: r_io_pad_out[4] FREX out control Bit[3]: r_io_pad_out[3] FSIN out control Bit[2]: r_io_pad_out[2] STROBE out control Bit[1]: r_io_pad_out[1] GPIO1 out control Bit[0]: r_io_pad_out[0] GPIO0 out control
0x3006	RSVD	–	–	Reserved

table 6-3 SC_CMMN_REG registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x3007	SC_CMMN_7	0x08	RW	Bit[7:2]: Reserved Bit[1]: r_io_pad_sel[9] GPIO3 select output control value Bit[0]: r_io_pad_sel[8] GPIO2 select output control value
0x3008	SC_CMMN_8	0x00	RW	Bit[7]: r_io_pad_sel[7] VSYNC select output control value Bit[6]: r_io_pad_sel[6] HREF select output control value Bit[5]: Reserved Bit[4]: r_io_pad_sel[4] STROBE select output control value Bit[3]: r_io_pad_sel[3] FSIN select output control value Bit[2]: r_io_pad_sel[2] ILL_PWM select output control value Bit[1]: r_io_pad_sel[1] GPIO1 select output control value Bit[0]: r_io_pad_sel[0] GPIO0 select output control value
0x3009	SC_CMMN_9	0x04	RW	Bit[7:0]: r_pad_pk[7:0]
0x300A	SC_CMMN_10	0x56	R	Bit[7:0]: r_snr_id[23:16]
0x300B	SC_CMMN_11	0x64	R	Bit[7:0]: r_snr_id[15:8]
0x300C	SC_CMMN_12	0x42	R	Bit[7:0]: r_snr_id[7:0]
0x300D	SC_CMMN_13	0x22	RW	Bit[7]: Reserved Bit[6:4]: p_pump2_div Bit[3:0]: p_pump_div
0x300E	SC_CMMN_14	0x22	RW	Bit[7]: Reserved Bit[6:4]: n_pump2_div Bit[3:0]: n_pump_div
0x300F~ 0x3011	NOT USED	–	–	Not Used
0x3012	SC_CMMN_18	0x41	RW	r_mipi_sc Bit[7:4]: r_mipi_lane_num Bit[3]: Not used Bit[2]: r_mipi_pd_man Bit[1:0]: Reserved
0x3013	RSVD	–	–	Reserved

table 6-3 SC_CMMN_REG registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x3014	SC_CMMN_20	0xD2	RW	r_clk_rst_ctrl_0 Bit[7]: clk_en_lr_pd Bit[6]: clk_en_sync_fifo Bit[5]: Reserved Bit[4]: clk_en_lr Bit[3]: rst_lr_pd Bit[2]: rst_sync_fifo Bit[1]: Reserved Bit[0]: rst_lr
0x3015	SC_CMMN_21	0x00	RW	r_clk_rst_ctrl_1 Bit[7]: clk_en_psram Bit[6]: clk_en_bist Bit[5]: clk_en_band Bit[4]: Reserved Bit[3]: rst_psrm Bit[2]: rst_mbist Bit[1]: rst_band Bit[0]: Reserved
0x3016	SC_CMMN_22	0xB0	RW	r_clk_rst_ctrl_2 Bit[7]: clk_en_sensor_top Bit[6]: clk_en_strobe Bit[5]: clk_en_pdfifo Bit[4]: clk_en_tc Bit[3]: rst_sensor_top Bit[2]: rst_strobe Bit[1]: rst_pdfifo Bit[0]: rst_tc
0x3017	SC_CMMN_23	0xF0	RW	r_clk_rst_ctrl_3 Bit[7]: clk_en_tpm Bit[6]: clk_en_isp Bit[5]: Reserved Bit[4]: clk_en_vfifo Bit[3]: rst_tpm Bit[2]: rst_isp Bit[1]: rst_arb Bit[0]: rst_vfifo
0x3018	SC_CMMN_24	0xF0	RW	r_clk_rst_ctrl_4 Bit[7]: clk_en_pdfifo Bit[6]: clk_en_mipi Bit[5]: clk_en_win Bit[4]: clk_en_efuse Bit[3]: Reserved Bit[2]: rst_mipi Bit[1]: rst_win Bit[0]: rst_efuse

table 6-3 SC_CMMN_REG registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x3019	SC_CMMN_25	0xD2	RW	r_clk_rst_ctrl_5 Bit[7]: clk_en_blc Bit[6]: clk_en_spfc Bit[5]: clk_en_testmode Bit[4]: sclk_fc_en Bit[3]: rst_blc_en Bit[2]: rst_ispfc Bit[1]: rst_testmode Bit[0]: rst_fc
0x301A	SC_CMMN_26	0xF0	RW	r_clk_rst_ctrl_6 Bit[7]: clk_en_grp Bit[6]: clk_en_asram Bit[5]: clk_en_vfifo Bit[4]: clk_en_mipi Bit[3]: rst_grp Bit[2]: rst_mipi_sc Bit[1]: rst_illum Bit[0]: rst_psv
0x301B	SC_CMMN_27	0x34	RW	r_clk_rst_ctrl_7 Bit[7:5]: Reserved Bit[4]: clk_en_emb Bit[3:1]: Reserved Bit[0]: rst_emb
0x301C	SC_CMMN_28	0x81	RW	r_frex_rst_mask_ctrl_0 Bit[7]: frex_mask_sensor_top Bit[6]: frex_mask_illum Bit[5]: frex_mask_snr_sync Bit[4]: Reserved Bit[3]: frex_mask_ispfc Bit[2]: frex_mask_blc Bit[1]: frex_mask_psram/band/stg/tc Bit[0]: frex_mask_stb
0x301D	SC_CMMN_29	0x02	RW	r_frex_rst_mask_ctrl_1 Bit[7]: Reserved Bit[6]: frex_mask_tpm Bit[5]: frex_mask_isp/win/lr Bit[4]: Reserved Bit[3]: frex_mask_mipi Bit[2]: frex_mask_testmode Bit[1]: frex_mask_arb Bit[0]: frex_mask_mipi_phy
0x301E	SC_CMMN_30	0x98	RW	r_frex_rst_mask_ctrl_2 Bit[7:6]: Reserved Bit[5]: frex_mask_psv Bit[4]: frex_mask_emb/grp Bit[3:0]: Reserved

table 6-3 SC_CMMN_REG registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x301F	NOT USED	–	–	Not Used
0x3020	SC_CMMN_32	0x01	RW	Bit[7:1]: Reserved Bit[0]: cen_global
0x3021	RSVD	–	–	Reserved
0x3022	SC_CMMN_34	0xF0	RW	r_clk_rst_ctrl_9 Bit[7]: isp_srf_clk_en Bit[6]: arb_clk_en Bit[5:4]: Reserved Bit[3]: isp_srf_clk from sclk Do not switch to padclk in sleep Bit[2]: arb_clk from sclk Do not switch to padclk in sleep Bit[1]: Reserved Bit[0]: clk_grp from sclk Do not switch to padclk in sleep
0x3023	RSVD	–	–	Reserved
0x3024	SC_CMMN_36	0xF0	RW	r_frex_rst_mask_ctrl_3 Bit[7:5]: Reserved Bit[4]: frex_mask_fc Bit[3:0]: Reserved
0x3025	RSVD	–	–	Reserved
0x3026	SC_CMMN_38	0x98	RW	PSV Mode Clock Gating Disable Bit[7:5]: Reserved Bit[4]: mask_mipi_clk_gating Bit[3]: mask_vfifo_clk_gating Bit[2]: mask_pdfifo_clk_gating Bit[1]: Reserved Bit[0]: mask_psram_clk_gating
0x3027	SC_CMMN_39	0x0C	RW	PSV Mode Clock Gating Disable Bit[7]: mask_testmode_clk_gating Bit[6]: mask_ispfc_clk_gating Bit[5]: Mask clock gating for sync_fifo, BLC, band_eav Bit[4]: Reserved Bit[3]: mask_clk_gating_mipi_sclk Bit[2]: mask_clk_gating_vfifo_sclk Bit[1]: Mask clock gating for ISP, lr_pipe, lr_pd Bit[0]: Mask clock gating for pdfifo_sclk
0x3028~ 0x3029	RSVD	–	–	Reserved
0x302A	SC_CMMN_42	–	R	Bit[7:0]: version_id[7:0]

table 6-3 SC_CMMN_REG registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x302B	SC_CMMN_43	–	R	Bit[7:0]: split_id[7:0]
0x302C	SC_CMMN_44	0x01	RW	Bit[7:0]: r_sc_lp_ctrl[39:32]
0x302D	SC_CMMN_45	0x00	RW	Bit[7:0]: r_sc_lp_ctrl[31:24]
0x302E	SC_CMMN_46	0x00	RW	Bit[7:0]: r_sc_lp_ctrl[23:16]
0x302F	SC_CMMN_47	0x00	RW	Bit[7:0]: r_sc_lp_ctrl[15:8]
0x3030	SC_CMMN_48	0x03	RW	Bit[7:0]: r_sc_lp_ctrl[7:0]
0x3031~ 0x3034	RSVD	–	–	Reserved
0x3035	SC_CMMN_53	0x6C	RW	Bit[7:0]: r_sccb_id_0[7:0] for SID = 0
0x3036	SC_CMMN_54	0x42	RW	Bit[7:0]: r_sccb_id_1[7:0] for SID = 0
0x3037	SC_CMMN_55	0x20	RW	Bit[7:0]: r_sccb_id_2[7:0] for SID = 1
0x3038	SC_CMMN_56	0x00	RW	Bit[7:1]: Reserved Bit[0]: sccb_id2_nack
0x3039	SC_CMMN_57	0x44	RW	Bit[7:0]: r_sccb_id_3[7:0] for SID = 2
0x303A	SC_CMMN_58	0x46	RW	Bit[7:0]: r_sccb_id_4[7:0] for SID = 3
0x300B~ 0x300C	RSVD	–	–	Reserved
0x303D	SC_CMMN_61	–	R	Bit[7:0]: r_io_pad[23:16]
0x303E	SC_CMMN_62	–	R	Bit[7:0]: r_io_pad[15:8]
0x303F	SC_CMMN_63	–	R	Bit[7:0]: r_io_pad[7:0]
0x3040~ 0x3043	RSVD	–	–	Reserved
0x3044	SC_CMMN_68	0xC2	RW	Bit[7:0]: r_esd_watchdog_ctrl[15:8]
0x3045	SC_CMMN_69	0x08	RW	Bit[7:0]: r_esd_watchdog_ctrl[7:0]
0x3046	RSVD	–	–	Reserved
0x3047	SC_CMMN_71	0x07	RW	Bit[7:3]: Not used Bit[2:0]: sclk_sw_ctrl[10:8]
0x3048	SC_CMMN_72	0x67	RW	Bit[7:0]: sclk_sw_ctrl[7:0]

6.4 SCCB [0x3100 - 0x3108]

table 6-4 SCCB registers

address	register name	default value	R/W	description
0x3100	SCCB CTRL	0x00	RW	Bit[7:4]: Reserved Bit[3]: r_sda_dly_en Bit[2:0]: r_sda_dly
0x3101	SCCB OPT	0x12	RW	Bit[7:5]: Reserved Bit[4]: en_ss_addr_inc Bit[3]: r_sda_byp_sync 0: Two clock stage sync for sda_i 1: No sync for sda_i Bit[2]: r_scl_byp_sync 0: Two clock stage sync for scl_i 1: No sync for scl_i Bit[1]: r_msk_glitch Bit[0]: r_msk_stop
0x3102	SCCB SCL CHK	0x05	RW	Bit[7:4]: Not used Bit[3]: r_scl_chk_en Bit[2:0]: r_scl_pulse_num_min
0x3103	PLL CLK SEL	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pll_clk_sel
0x3104~ 0x3106	RSVD	–	–	Reserved
0x3107	CTRL07	0x86	RW	Bit[7]: r_srb_clk_syn_en Bit[6:0]: sccb_sysreg
0x3108	NOT USED	–	–	Not Used

6.5 GROUP_HOLD [0x3200 - 0x3245]

table 6-5 GROUP_HOLD registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Bit[7:0]: group_adr0
0x3201	GROUP ADR1	0x04	RW	Bit[7:0]: group_adr1
0x3202	GROUP ADR2	0x08	RW	Bit[7:0]: group_adr2
0x3203	GROUP ADR3	0x0C	RW	Bit[7:0]: group_adr3

table 6-5 GROUP_HOLD registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x3204	GROUP ADR4	0x10	RW	Bit[7:0]: group_adr4
0x3205	GROUP ADR5	0x14	RW	Bit[7:0]: group_adr5
0x3206	FSIN GRP	0x00	RW	Bit[7]: re_launch_disable Bit[6:5]: Not used Bit[4]: fsin_en Bit[3:0]: Start group in FSIN mode
0x3207	COMBINE LAUNCH CTRL	–	W	Bit[7:4]: Launch option select 0110: Launch at HBLK 1010: Launch in frame blanking 1110: Launch directly Others: Reserved Bit[3]: cmb_lch_grp3 Combine launch include group3 Bit[2]: cmb_lch_grp2 Combine launch include group2 Bit[1]: cmb_lch_grp1 Combine launch include group1 Bit[0]: cmb_lch_grp0 Combine launch include group0

table 6-5 GROUP_HOLD registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 0110: Launch at HBLK 1010: Launch in frame blanking 1110: Launch directly Others: Reserved Bit[3:0]: group_id 0000: Group bank 0, default start from address 9'h000 0001: Group bank 1, default start from address 9'h040 0010: Group bank 2, default start from address 9'h080 0011: Group bank 3, default start from address 9'h0C0 0100: Group bank 4, default start from address 9'h100 0101: Group bank 5, default start from address 9'h140 0110: Group bank 6, default start from address 9'h180 0111: Group bank 7, default start from address 9'h1A0 1000: Group bank 8, default start from address 9'h1C0 1001: Group bank 9, default start from address 9'h1E0 1010: Group bank 10, default start from address 0x100 1011: Group bank 11, default start from address 9'h120 1100: Group bank 12, default start from address 9'h140 1101: Group bank 13, default start from address 9'h160 1110: Group bank 14, default start from address 9'h180 1111: Group bank 15, default start from address 9'h1A0
0x3209	GRP0 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp0
0x320A	GRP1 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp1
0x320B	GRP2 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp2
0x320C	GRP3 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp3
0x320D	GRP SWCTRL	0x01	RW	Bit[7]: Context switch enable Bit[6:4]: Auto launch loop number Bit[3:0]: Switch back group

table 6-5 GROUP_HOLD registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x320E	CONTEXT SW GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0110: Launch at HBLK 1010: Launch in frame blanking 1110: Launch directly Others: Reserved Bit[3:0]: group_id 0000: Group bank 0, default start from address 11'h000 0001: Group bank 1, default start from address 11'h100 0010: Group bank 2, default start from address 11'h200 0011: Group bank 3, default start from address 11'h300 1010: Group bank 10, default start from address 11'h500 1011: Group bank 11, default start from address 11'h520 1100: Group bank 12, default start from address 11'h540 1101: Group bank 13, default start from address 11'h560 1110: Group bank 14, default start from address 11'h580 1111: Group bank 15, default start from address 11'h5A0 Others: Reserved
0x320F	RSVD	–	–	Reserved
0x3210	GROUP LEN0	–	W	group_len0
0x3211	GROUP LEN1	–	W	group_len1
0x3212	GROUP LEN2	–	W	group_len2
0x3213	GROUP LEN3	–	W	group_len3
0x3214	GROUP LEN4	–	W	group_len4
0x3215	GROUP LEN5	–	W	group_len5
0x3216	EMB LINE NUM	0x01	RW	Bit[7:4]: Not used Bit[3:0]: emb_line_num
0x3217	PADDING DATA	0x00	RW	Bit[7:0]: padding_data

table 6-5 GROUP_HOLD registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x3218	R16	0x00	RW	Bit[7:6]: emb_line_blk_ctrl 00: 32 SCLK 01: 64 SCLK 10: 128 SCLK 11: Wait for external trigger signal Bit[5]: embline_addr_en Bit[4]: r_padding_md2 0: No dummy data mixing with valid data 1: Dummy data output with valid data every cycle Bit[3]: frame_trig_sel 0: tc_grp_wr 1: EOF Bit[2]: embline_eof_en Bit[1]: embline_sof_en Bit[0]: embline_tag_en
0x3219	TAG DATA	0x55	RW	Bit[7:0]: emb_tag
0x321A	GRP ACT	–	R	Indicates Which Group is Active
0x321B	NOT USED	–	–	Not Used
0x321C	FRAME CNT GRP0	–	R	frame_cnt_grp0
0x321D	FRAME CNT GRP1	–	R	frame_cnt_grp1
0x321E	FRAME CNT GRP2	–	R	frame_cnt_grp2
0x321F	FRAME CNT GRP3	–	R	frame_cnt_grp3
0x3220	SRAM TEST	0x11	RW	Bit[7:6]: Reserved Bit[5:0]: SRAM test
0x3221	SRAM TEST	0x30	RW	Bit[7]: Not used Bit[6:3]: sram_rm Bit[2]: sram_rme Bit[1]: sram_test1 Bit[0]: sram_ls
0x3222	GAIN LAUNCH CTRL	0x02	RW	Bit[7:2]: Not used Bit[1]: default_launch_en Bit[0]: gain_launch_en
0x3223	GROUP ADR6	0x18	RW	Bit[7:0]: group_adr6
0x3224	GROUP ADR7	0x1A	RW	Bit[7:0]: group_adr7
0x3225	GROUP ADR8	0x1C	RW	Bit[7:0]: group_adr8
0x3226	GROUP ADR9	0x1E	RW	Bit[7:0]: group_adr9
0x3227	GROUP LEN6	–	W	group_len6

table 6-5 GROUP_HOLD registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x3228	GROUP LEN7	–	W	group_len7
0x3229	GROUP LEN8	–	W	group_len8
0x322A	GROUP LEN9	–	W	group_len9
0x322B~ 0x322E	NOT USED	–	–	Not Used
0x322F	TC GRP WR CTRL	0x00	RW	Bit[7]: r_grp_wr_opt Bit[6:0]: mask_grp_wr_frame_num
0x3230	GROUP ADR10	0x10	RW	Bit[7:0]: group_adr10
0x3231	GROUP ADR11	0x12	RW	Bit[7:0]: group_adr11
0x3232	GROUP ADR12	0x14	RW	Bit[7:0]: group_adr12
0x3233	GROUP ADR13	0x16	RW	Bit[7:0]: group_adr13
0x3234	GROUP ADR14	0x18	RW	Bit[7:0]: group_adr14
0x3235	GROUP ADR15	0x1A	RW	Bit[7:0]: group_adr15
0x3236~ 0x3238	NOT USED	–	–	Not Used
0x3239	GRP10 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp10
0x323A	GRP11 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp11
0x323B	GRP12 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp12
0x323C	GRP13 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp13
0x323D	GRP14 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp14
0x323E	GRP15 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp15
0x323F	NOT USED	–	–	Not Used
0x3240	GROUP LEN10	–	W	group_len10
0x3241	GROUP LEN11	–	W	group_len11
0x3242	GROUP LEN12	–	W	group_len12
0x3243	GROUP LEN13	–	W	group_len13
0x3244	GROUP LEN14	–	W	group_len14
0x3245	GROUP LEN15	–	W	group_len15

6.6 PSV_CTRL [0x3400 - 0x3429]

table 6-6 PSV_CTRL registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3400	PSV_CTRL_13_0	0x08	RW	Bit[7:4]: Reserved Bit[3]: psv_auto_dis PSV auto mode disable Bit[2]: r_psv_mode_en PSV manual mode enable Bit[1]: r_dis_m Disable vblanking for M channel (debug) Bit[0]: r_dis_s Disable vblanking for S channel (debug)
0x3401	PSV_CTRL_13_1	0x00	RW	Bit[7:5]: Reserved Bit[4]: stream_clk_allon Clock is always on (disable clock gating) Bit[3:0]: Reserved
0x3402~ 0x3405	NOT USED	–	–	Not Used
0x3406	PSV_CTRL_13_6	0x08	RW	Bit[7:0]: r_stream_st_offs Streaming start line number before frame end, number = r_stream_st_offs × 4
0x3407	PSV_CTRL_13_7	0x08	RW	Bit[7:0]: r_pchg_st_offs Pre-charge start line number before frame end, number = r_pchg_st_offs × 4
0x3408	PSV_CTRL_13_8	0x05	RW	Bit[7:4]: Reserved Bit[3:0]: r_clk_winp_offs Clock enable start line number before frame end, number = r_clk_winp_offs × 4
0x3409	PSV_CTRL_13_9	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: r_clk_winp_offs Clock disable delay line number after internal streaming ends, number = r_clk_winp_offs × 4
0x340A	PSV_CTRL_13_10	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: r_pchg_rear_offs Pre-charge delay line number after internal pre-charge ends, number = r_clk_winp_offs × 4
0x340B	RSVD	–	–	Reserved
0x340C	PSV_CTRL_13_12	0x10	RW	Bit[7:0]: psv_auto_on_thresh[15:8] PSV auto mode VTS threshold, enter PSV mode if VTS < psv_auto_on_thresh

table 6-6 PSV_CTRL registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x340D	PSV_CTRL_13_13	0x00	RW	Bit[7:0]: psv_auto_on_thresh[7:0] PSV auto mode VTS threshold, enter PSV mode if VTS < psv_auto_on_thresh
0x340E	PSV_CTRL_13_14	0x30	RW	Bit[7:0]: r_vblank_thresh[7:0] PSV mode auto disable vblanking threshold, if vblanking < r_vblank_thresh, will not enter PSV mode even when PSV is on
0x340F~ 0x341F	RSVD	–	–	Reserved
0x3420	PSV_CTRL_13_32	0x00	RW	Bit[7:4]: Reserved Bit[3:2]: r_mipi_pll_pd_sel Control MIPI PD signal 00: No power down 01: Power down in vertical blanking 10: Always power down 11: Power down in streaming clock off period Bit[1:0]: r_mipi_phy_rst_sel Control MIPI PHY reset signal 00: No power down 01: Power down in vertical blanking 10: Always power down 11: Power down in streaming clock off period
0x3421	PSV_CTRL_13_33	0x15	RW	r_asp_pd Bit[7]: Control VDAC PD Bit[6]: Control VREF PD Bit[5]: Control V2I PD Bit[4]: Control XDEC PD Bit[3]: Control CBAR PD Bit[2]: Control VLN PD Bit[1]: Control DCPM PD Bit[0]: Control SRAM PD
0x3422	PSV_CTRL_13_34	0x40	RW	r_asp_pd Bit[7]: Reserved Bit[6]: Control FDC PD Bit[5]: Control pump clock PD Bit[4:3]: Reserved Bit[2]: Control ramp buffer PD Bit[1]: Reserved Bit[0]: Control pump PD
0x3423	RSVD	–	–	Reserved

table 6-6 PSV_CTRL registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x3424	PSV_CTRL_13_36	0x00	RW	r_asp_pd_sel_0 Bit[7:6]: asp_pd_sig3_timing_option for CBAR 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming Bit[5:4]: asp_pd_sig2_timing_option for VLN 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming Bit[3:2]: asp_pd_sig1_timing_option for DCOMP 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming Bit[1:0]: asp_pd_sig0_timing_option for ASRAM 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming

table 6-6 PSV_CTRL registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x3425	PSV_CTRL_13_37	0x00	RW	r_asp_pd_sel_1 Bit[7:6]: asp_pd_sig7_timing_option for DAC 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming Bit[5:4]: asp_pd_sig6_timing_option for VREF 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming Bit[3:2]: asp_pd_sig5_timing_option for V2I 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming Bit[1:0]: asp_pd_sig4_timing_option for XDEC 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming
0x3426	PSV_CTRL_13_38	0x00	RW	r_asp_pd_sel_2 Bit[7:6]: Reserved Bit[5:4]: asp_pd_sig10_timing_option for RAMPBUF 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming Bit[3:2]: Reserved Bit[1:0]: asp_pd_sig8_timing_option for PUMP 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming

table 6-6 PSV_CTRL registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x3427	PSV_CTRL_13_39	0x00	RW	r_asp_pd_sel_3 Bit[7:6]: Reserved Bit[5:4]: asp_pd_sig14_timing_option for FDC 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming Bit[3:2]: asp_pd_sig13_timing_option for PUMP_CLK 00: Controlled by register 01: Power down in vertical blanking 10: Power down in pre-change vertical blanking 11: Power down in common vertical blanking of pre-change and streaming Bit[1:0]: Reserved
0x3428~ 0x3429	RSVD	–	–	Reserved

6.7 AEC_PK_L [0x3500 - 0x353D]

table 6-7 AEC_PK_L registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3500	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[23:16]
0x3501	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[15:8]
0x3502	EXPO COARSE	0x40	RW	Bit[7:0]: expo_coarse[7:0]

table 6-7 AEC_PK_L registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3503	AEC_CFG_3	0xA8	RW	Bit[7]: agc_manual_en 0: real_gain_auto 1: real_gain manual Bit[6]: digi_gain_delay_1frame 0: 2 frame delay 1: 1 frame delay Bit[5]: format_change_update_en Bit[4]: gain_delay_option 0: 2 frame delay 1: 1 frame delay Bit[3]: aec_manual_en 0: Auto AEC enable 1: Manual AEC enable Bit[2]: expo_fine_delay_option 0: 2 frame delay 1: 1 frame delay Bit[1]: expo_coarse_delay_option 0: 2 frame delay 1: 1 frame delay Bit[0]: expo_change_delay_option 0: 2 frame delay 1: 1 frame delay
0x3504	AEC_CFG_4	0x08	RW	Bit[7]: real_gain_as_snr_gain Bit[6]: isp_real_gain_blc Bit[5]: digi_gain_by_mwb Bit[4]: gain_delay_by_expo_change Bit[3]: initial_update_en Bit[2]: Use B channel digital gain apply to all channels Bit[1]: vdl_sync_en Bit[0]: Not used
0x3505	MANUAL UPDATE EN	–	RW	Bit[7:1]: Not used Bit[0]: manual_update_en[0]
0x3506	AEC_PK_FINE_ EXP_6	0x00	RW	Bit[7:0]: expo_fine[15:8]
0x3507	AEC_PK_FINE_ EXP_7	0x00	RW	Bit[7:0]: expo_fine[7:0]
0x3508	GAIN COARSE	0x01	RW	Bit[7]: Not used Bit[6:0]: gain_coarse[6:0]
0x3509	CTRL 09	0x00	RW	Bit[7:1]: gain_fine Bit[0]: Not used
0x350A	AEC_CFG_10	0x01	RW	Bit[7:4]: Not used Bit[3:0]: dig_gain_coarse_b[3:0]
0x350B	AEC_CFG_11	0x00	RW	Bit[7:0]: For global digital gain or digital gain for B channel[9:2]

table 6-7 AEC_PK_L registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x350C	AEC_CFG_12	0x00	RW	Bit[7:6]: For global digital gain or digital gain for B channel[1:0] Bit[5:0]: Not used

0x350D	AEC_CFG_13	0x00	RW	Bit[7:2]: Not used
				Bit[1:0]: snr_gain_map
				00: Default
				cmp_gain[2:0] = snr_gain_coarse[2:0];
				dac_gain[1:0] = snr_gain_coarse[4:3]
				01: Opt1
				cmp_gain[2:0] = {snr_gain_coarse[3:2], snr_gain_coarse[0]};
				dac_gain[1:0] = {snr_gain_coarse[4], snr_gain_coarse[1]}
				10: Opt2
				cmp_gain[2:0] = {snr_gain_coarse[3], snr_gain_coarse[1:0]};
				dac_gain[1:0] = {snr_gain_coarse[4], snr_gain_coarse[2]}
				11: Opt3
				cmp_gain[2:0] = snr_gain_coarse[3:1];
				dac_gain[1:0] = {snr_gain_coarse[4], snr_gain_coarse[0]}

0x350E	CTRL0E	0x00	RW	Bit[7]: r_otp_gain_en Bit[6]: r_otp_gain_auto_en Bit[5]: r_gain_shift Bit[4:0]: Not used
0x350F	R OTP GAIN MAN COARSE	0x01	RW	Bit[7:0]: r_otp_gain_man_coarse
0x3510	AEC_PK_DIG_GAIN_16	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain for Gb channel[3:0]
0x3511	AEC_PK_DIG_GAIN_17	0x00	RW	Bit[7:0]: Digital gain for Gb channel[9:2]
0x3512	AEC_PK_DIG_GAIN_18	0x00	RW	Bit[7:6]: Digital gain for Gb channel[1:0] Bit[5:0]: Not used
0x3513	AEC_PK_DIG_GAIN_19	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain for Gr channel[3:0]
0x3514	AEC_PK_DIG_GAIN_20	0x00	RW	Bit[7:0]: Digital gain for Gr channel[9:2]

table 6-7 AEC_PK_L registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x3515	AEC_PK_DIG_GAIN_21	0x00	RW	Bit[7:6]: Digital gain for Gr channel[1:0] Bit[5:0]: Not used
0x3516	AEC_PK_DIG_GAIN_22	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain for R channel[3:0]
0x3517	AEC_PK_DIG_GAIN_23	0x00	RW	Bit[7:0]: Digital gain for R channel[9:2]
0x3518	AEC_PK_DIG_GAIN_24	0x00	RW	Bit[7:6]: Digital gain for R channel[1:0] Bit[5:0]: Not used
0x3519	R OTP GAIN MAN FINE	0x00	RW	Bit[7:0]: r_otp_gain_man_fine[15:8]
0x351A	R OTP GAIN MAN FINE	0x00	RW	Bit[7:0]: r_otp_gain_man_fine[7:0]
0x351B	AEC_CFG_27	–	R	Bit[7:0]: expo_coarse_cur[23:16]
0x351C	AEC_CFG_28	–	R	Bit[7:0]: expo_coarse_cur[15:8]
0x351D	AEC_CFG_29	–	R	Bit[7:0]: expo_coarse_cur[7:0]
0x351E	AEC_CFG_30	–	R	Bit[7]: Not used Bit[6:0]: gain_coarse_cur_use[6:0]
0x351F	AEC_CFG_31	–	R	Bit[7:1]: gain_fine_cur_use[6:0] Bit[0]: Not used
0x3520	AEC_CFG_32	–	R	Bit[7]: Not used Bit[6:0]: gain_coarse_cur_org[6:0]
0x3521	AEC_CFG_33	–	R	Bit[7:1]: gain_fine_cur_org[6:0] Bit[0]: Not used
0x3522	AEC_CFG_34	–	R	Bit[7]: Not used Bit[6:0]: snr_gain_coarse_cur[6:0]
0x3523	AEC_CFG_35	–	R	Bit[7:1]: snr_gain_fine_cur[6:0] Bit[0]: Not used
0x3524	AEC_CFG_36	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_b[3:0]
0x3525	AEC_CFG_37	–	R	Bit[7:0]: cur_dig_gain_fine_b[9:2]
0x3526	AEC_CFG_38	–	R	Bit[7:6]: cur_dig_gain_fine_b[1:0] Bit[5:0]: Not used
0x3527	AEC_CFG_39	–	R	Bit[7]: Not used Bit[6:0]: real_gain_blc_coarse[6:0]
0x3528	AEC_CFG_40	–	R	Bit[7:4]: real_gain_blc_fine[3:0] Bit[3:0]: Not used
0x3529	AEC_CFG_41	–	R	Bit[7:3]: Not used Bit[2:0]: real_gain_isp_coarse[10:8]

table 6-7 AEC_PK_L registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x352A	AEC_CFG_42	–	R	Bit[7:0]: real_gain_isp_coarse[7:0]
0x352B	AEC_CFG_43	–	R	Bit[7:4]: real_gain_isp_fine[3:0] Bit[3:0]: Not used
0x352C	AEC_PK_FINE_EXP_44	–	R	Bit[7:0]: expo_fine_cur[15:8]
0x352D	R OTP GAIN AUTO COARSE	0x01	RW	Bit[7:0]: r_otp_gain_auto_coarse
0x352E	R OTP GAIN AUTO FINE	0x00	RW	Bit[7:0]: r_otp_gain_auto_fine[15:8]
0x352F	R OTP GAIN AUTO FINE	0x00	RW	Bit[7:0]: r_otp_gain_auto_fine[7:0]
0x3530	AEC_PK_DIG_GAIN_48	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_gb[3:0]
0x3531	AEC_PK_DIG_GAIN_49	–	R	Bit[7:0]: cur_dig_gain_fine_gb[9:2]
0x3532	AEC_PK_DIG_GAIN_50	–	R	Bit[7:6]: cur_dig_gain_fine_gb[1:0] Bit[5:0]: Not used
0x3533	AEC_PK_DIG_GAIN_51	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_gr[3:0]
0x3534	AEC_PK_DIG_GAIN_52	–	R	Bit[7:0]: cur_dig_gain_fine_gr[9:2]
0x3535	AEC_PK_DIG_GAIN_53	–	R	Bit[7:6]: cur_dig_gain_fine_gr[1:0] Bit[5:0]: Not used
0x3536	AEC_PK_DIG_GAIN_54	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_r[3:0]
0x3537	AEC_PK_DIG_GAIN_55	–	R	Bit[7:0]: cur_dig_gain_fine_r[9:2]
0x3538	AEC_PK_DIG_GAIN_56	–	R	Bit[7:6]: cur_dig_gain_fine_r[1:0] Bit[5:0]: Not used
0x3539	REAL GAIN ISP COMPLETE	–	R	Bit[7:0]: real_gain_isp_complete[39:32]
0x353A	REAL GAIN ISP COMPLETE	–	R	Bit[7:0]: real_gain_isp_complete[31:24]
0x353B	REAL GAIN ISP COMPLETE	–	R	Bit[7:0]: real_gain_isp_complete[23:16]
0x353C	REAL GAIN ISP COMPLETE	–	R	Bit[7:0]: real_gain_isp_complete[15:8]
0x353D	REAL GAIN ISP COMPLETE	–	R	Bit[7:0]: real_gain_isp_complete[7:0]

6.8 AEC_PK_M [0x3540 - 0x3578]

table 6-8 AEC_PK_M registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x3540	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[23:16]
0x3541	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[15:8]
0x3542	EXPO COARSE	0x40	RW	Bit[7:0]: expo_coarse[7:0]
0x3543	AEC_CFG_3	0xA8	RW	Bit[7]: agc_manual_en 0: real_gain_auto 1: real_gain manual Bit[6]: digi_gain_delay_1frame 0: 2 frame delay 1: 1 frame delay Bit[5]: format_change_update_en Bit[4]: gain_delay_option 0: 2 frame delay 1: 1 frame delay Bit[3]: aec_manual_en 0: Auto AEC enable 1: Manual AEC enable Bit[2]: expo_fine_delay_option 0: 2 frame delay 1: 1 frame delay Bit[1]: expo_coarse_delay_option 0: 2 frame delay 1: 1 frame delay Bit[0]: expo_change_delay_option 0: 2 frame delay 1: 1 frame delay
0x3544	AEC_CFG_4	0x08	RW	Bit[7]: real_gain_as_snr_gain Bit[6]: isp_real_gain_blc Bit[5]: digi_gain_by_mwb Bit[4]: gain_delay_by_expo_change Bit[3]: initial_update_en Bit[2]: Use B channel digital gain apply to all channels Bit[1]: vdl_sync_en Bit[0]: Not used
0x3545	NOT USED	–	–	Not Used
0x3546	AEC_PK_FINE_ EXP_6	0x00	RW	Bit[7:0]: expo_fine[15:8]
0x3547	AEC_PK_FINE_ EXP_7	0x00	RW	Bit[7:0]: expo_fine[7:0]
0x3548	GAIN COARSE	0x01	RW	Bit[7]: Not used Bit[6:0]: gain_coarse[6:0]

table 6-8 AEC_PK_M registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x3549	CTRL 09	0x00	RW	Bit[7:1]: gain_fine Bit[0]: Not used
0x354A	AEC_CFG_10	0x01	RW	Bit[7:4]: Not used Bit[3:0]: dig_gain_coarse_b[3:0]
0x354B	AEC_CFG_11	0x00	RW	Bit[7:0]: For global digital gain or digital gain for B channel[9:2]
0x354C	AEC_CFG_12	0x00	RW	Bit[7:6]: For global digital gain or digital gain for B channel[1:0] Bit[5:0]: Not used

0x354D	AEC_CFG_13	0x00	RW	Bit[7:2]: Not used
				Bit[1:0]: snr_gain_map
				00: Default
				cmp_gain[2:0] = snr_gain_coarse[2:0];
				dac_gain[1:0] = snr_gain_coarse[4:3]
				01: Opt1
				cmp_gain[2:0] = {snr_gain_coarse[3:2], snr_gain_coarse[0]};
				dac_gain[1:0] = {snr_gain_coarse[4], snr_gain_coarse[1]}
				10: Opt2
				cmp_gain[2:0] = {snr_gain_coarse[3], snr_gain_coarse[1:0]};
				dac_gain[1:0] = {snr_gain_coarse[4], snr_gain_coarse[2]}
				11: Opt3
				cmp_gain[2:0] = snr_gain_coarse[3:1];
				dac_gain[1:0] = {snr_gain_coarse[4], snr_gain_coarse[0]}

0x354E~ 0x354F	NOT USED	–	–	Not Used
0x3550	AEC_PK_DIG_GAIN_16	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain for Gb channel[3:0]
0x3551	AEC_PK_DIG_GAIN_17	0x00	RW	Bit[7:0]: Digital gain for Gb channel[9:2]
0x3552	AEC_PK_DIG_GAIN_18	0x00	RW	Bit[7:6]: Digital gain for Gb channel[1:0] Bit[5:0]: Not used

table 6-8 AEC_PK_M registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x3553	AEC_PK_DIG_GAIN_19	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain for Gr channel[3:0]
0x3554	AEC_PK_DIG_GAIN_20	0x00	RW	Bit[7:0]: Digital gain for Gr channel[9:2]
0x3555	AEC_PK_DIG_GAIN_21	0x00	RW	Bit[7:6]: Digital gain for Gr channel[1:0] Bit[5:0]: Not used
0x3556	AEC_PK_DIG_GAIN_22	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Digital gain for R channel[3:0]
0x3557	AEC_PK_DIG_GAIN_23	0x00	RW	Bit[7:0]: Digital gain for R channel[9:2]
0x3558	AEC_PK_DIG_GAIN_24	0x00	RW	Bit[7:6]: Digital gain for R channel[1:0] Bit[5:0]: Not used
0x3559~ 0x355A	NOT USED	–	–	Not Used
0x355B	AEC_CFG_27	–	R	Bit[7:0]: expo_coarse_cur[23:16]
0x355C	AEC_CFG_28	–	R	Bit[7:0]: expo_coarse_cur[15:8]
0x355D	AEC_CFG_29	–	R	Bit[7:0]: expo_coarse_cur[7:0]
0x355E	AEC_CFG_30	–	R	Bit[7]: Not used Bit[6:0]: gain_coarse_cur_use[6:0]
0x355F	AEC_CFG_31	–	R	Bit[7:1]: gain_fine_cur_use[6:0] Bit[0]: Not used
0x3560	AEC_CFG_32	–	R	Bit[7]: Not used Bit[6:0]: gain_coarse_cur_org[6:0]
0x3561	AEC_CFG_33	–	R	Bit[7:1]: gain_fine_cur_org[6:0] Bit[0]: Not used
0x3562	AEC_CFG_34	–	R	Bit[7]: Not used Bit[6:0]: snr_gain_coarse_cur[6:0]
0x3563	AEC_CFG_35	–	R	Bit[7:1]: snr_gain_fine_cur[6:0] Bit[0]: Not used
0x3564	AEC_CFG_36	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_b[3:0]
0x3565	AEC_CFG_37	–	R	Bit[7:0]: cur_dig_gain_fine_b[9:2]
0x3566	AEC_CFG_38	–	R	Bit[7:6]: cur_dig_gain_fine_b[1:0] Bit[5:0]: Not used
0x3567	AEC_CFG_39	–	R	Bit[7]: Not used Bit[6:0]: real_gain_blc_coarse[6:0]
0x3568	AEC_CFG_40	–	R	Bit[7:4]: real_gain_blc_fine[3:0] Bit[3:0]: Not used

table 6-8 AEC_PK_M registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x3569	AEC_CFG_41	–	R	Bit[7:3]: Not used Bit[2:0]: real_gain_isp_coarse[10:8]
0x356A	AEC_CFG_42	–	R	Bit[7:0]: real_gain_isp_coarse[7:0]
0x356B	AEC_CFG_43	–	R	Bit[7:4]: real_gain_isp_fine[3:0] Bit[3:0]: Not used
0x356C	AEC_PK_FINE_EXP_44	–	R	Bit[7:0]: expo_fine_cur[15:8]
0x356D	AEC_PK_FINE_EXP_45	–	R	Bit[7:0]: expo_fine_cur[7:0]
0x356E~ 0x356F	NOT USED	–	–	Not Used
0x3570	AEC_PK_DIG_GAIN_48	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_gb[3:0]
0x3571	AEC_PK_DIG_GAIN_49	–	R	Bit[7:0]: cur_dig_gain_fine_gb[9:2]
0x3572	AEC_PK_DIG_GAIN_50	–	R	Bit[7:6]: cur_dig_gain_fine_gb[1:0] Bit[5:0]: Not used
0x3573	AEC_PK_DIG_GAIN_51	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_gr[3:0]
0x3574	AEC_PK_DIG_GAIN_52	–	R	Bit[7:0]: cur_dig_gain_fine_gr[9:2]
0x3575	AEC_PK_DIG_GAIN_53	–	R	Bit[7:6]: cur_dig_gain_fine_gr[1:0] Bit[5:0]: Not used
0x3576	AEC_PK_DIG_GAIN_54	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_r[3:0]
0x3577	AEC_PK_DIG_GAIN_55	–	R	Bit[7:0]: cur_dig_gain_fine_r[9:2]
0x3578	AEC_PK_DIG_GAIN_56	–	R	Bit[7:6]: cur_dig_gain_fine_r[1:0] Bit[5:0]: Not used

6.9 AEC_PK_S [0x3580 - 0x35BF]

table 6-9 AEC_PK_S registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x3580	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[23:16]
0x3581	EXPO COARSE	0x00	RW	Bit[7:0]: expo_coarse[15:8]
0x3582	EXPO COARSE	0x40	RW	Bit[7:0]: expo_coarse[7:0]

table 6-9 AEC_PK_S registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x3583	AEC_PK_3	0xA8	RW	Bit[7]: agc_manual_en 0: real_gain_auto 1: real_gain manual Bit[6]: digi_gain_delay_1frame 0: 2 frame delay 1: 1 frame delay Bit[5]: format_change_update_en Bit[4]: gain_delay_option 0: 2 frame delay 1: 1 frame delay Bit[3]: aec_manual_en 0: Auto AEC enable 1: Manual AEC enable Bit[2]: expo_fine_delay_option 0: 2 frame delay 1: 1 frame delay Bit[1]: expo_coarse_delay_option 0: 2 frame delay 1: 1 frame delay Bit[0]: expo_change_delay_option 0: 2 frame delay 1: 1 frame delay
0x3584	AEC_PK_4	0x08	RW	Bit[7]: real_gain_as_snr_gain Bit[6]: isp_real_gain_blc Bit[5]: digi_gain_by_mwb Bit[4]: gain_delay_by_expo_change Bit[3]: initial_update_en Bit[2]: Use B channel digital gain apply to all channels Bit[1]: vdl_sync_en Bit[0]: Not used
0x3585	MANUAL UPDATE EN	–	RW	Bit[7:1]: Not used Bit[0]: manual_update_en[0]
0x3586	AEC_PK_6	0x00	RW	Bit[7:0]: expo_fine[15:8]
0x3587	AEC_PK_7	0x00	RW	Bit[7:0]: expo_fine[7:0]
0x3588	GAIN COARSE	0x01	RW	Bit[7]: Not used Bit[6:0]: gain_coarse[6:0]
0x3589	AEC_PK_9	0x00	RW	Bit[7:1]: gain_fine Bit[0]: Not used
0x358A	AEC_PK_A	0x01	RW	Bit[7:4]: Not used Bit[3:0]: dig_gain_coarse_b[3:0]
0x358B	AEC_PK_B	0x00	RW	Bit[7:0]: dig_gain_fine_b[9:2]
0x358C	AEC_PK_C	0x00	RW	Bit[7:6]: dig_gain_fine_b[1:0] Bit[5:0]: Not used

table 6-9 AEC_PK_S registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x358D	AEC_PK_D	0x00	RW	Bit[7:2]: Not used Bit[1:0]: snr_gain_map
0x358E	AEC_PK_E	0x00	RW	Bit[7]: r_otp_gain_en Bit[6]: r_otp_gain_auto_en Bit[5]: r_gain_shift Bit[4:0]: Not used
0x358F	AEC_PK_F	0x01	RW	Bit[7:0]: r_otp_gain_man_coarse
0x3590	AEC_PK_10	0x01	RW	Bit[7:4]: Not used Bit[3:0]: dig_gain_coarse_gb[3:0]
0x3591	AEC_PK_11	0x00	RW	Bit[7:0]: dig_gain_fine_gb[9:2]
0x3592	AEC_PK_12	0x00	RW	Bit[7:6]: dig_gain_fine_gb[1:0] Bit[5:0]: Not used
0x3593	AEC_PK_13	0x01	RW	Bit[7:4]: Not used Bit[3:0]: dig_gain_coarse_gr[3:0]
0x3594	AEC_PK_14	0x00	RW	Bit[7:0]: dig_gain_fine_gr[9:2]
0x3595	AEC_PK_15	0x00	RW	Bit[7:6]: dig_gain_fine_gr[1:0] Bit[5:0]: Not used
0x3596	AEC_PK_16	0x01	RW	Bit[7:4]: Not used Bit[3:0]: dig_gain_coarse_r[3:0]
0x3597	AEC_PK_17	0x00	RW	Bit[7:0]: dig_gain_fine_r[9:2]
0x3598	AEC_PK_18	0x00	RW	Bit[7:6]: dig_gain_fine_r[1:0] Bit[5:0]: Not used
0x3599	AEC_PK_19	0x00	RW	Bit[7:0]: r_otp_gain_man_fine[15:8]
0x359A	AEC_PK_1A	0x00	RW	Bit[7:0]: r_otp_gain_man_fine[7:0]
0x359B	AEC_PK_1B	–	R	Bit[7:0]: expo_coarse_cur[23:16]
0x359C	AEC_PK_1C	–	R	Bit[7:0]: expo_coarse_cur[15:8]
0x359D	AEC_PK_1D	–	R	Bit[7:0]: expo_coarse_cur[7:0]
0x359E	AEC_PK_1E	–	R	Bit[7]: Not used Bit[6:0]: gain_coarse_cur_use[6:0]
0x359F	AEC_PK_1F	–	R	Bit[7:1]: gain_fine_cur_use[6:0] Bit[0]: Not used
0x35A0	AEC_PK_20	–	R	Bit[7]: Not used Bit[6:0]: gain_coarse_cur_org[6:0]
0x35A1	AEC_PK_21	–	R	Bit[7:1]: gain_fine_cur_org[6:0] Bit[0]: Not used

table 6-9 AEC_PK_S registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x35A2	AEC_PK_22	–	R	Bit[7]: Not used Bit[6:0]: snr_gain_coarse_cur[6:0]
0x35A3	AEC_PK_23	–	R	Bit[7:1]: snr_gain_fine_cur[6:0] Bit[0]: Not used
0x35A4	AEC_PK_24	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_b[3:0]
0x35A5	AEC_PK_25	–	R	Bit[7:0]: cur_dig_gain_fine_b[9:2]
0x35A6	AEC_PK_26	–	R	Bit[7:6]: cur_dig_gain_fine_b[1:0] Bit[5:0]: Not used
0x35A7	AEC_PK_27	–	R	Bit[7]: Not used Bit[6:0]: real_gain_blc_coarse[6:0]
0x35A8	AEC_PK_28	–	R	Bit[7:4]: real_gain_blc_fine[3:0] Bit[3:0]: Not used
0x35A9	AEC_PK_29	–	R	Bit[7:3]: Not used Bit[2:0]: real_gain_isp_coarse[10:8]
0x35AA	AEC_PK_2A	–	R	Bit[7:0]: real_gain_isp_coarse[7:0]
0x35AB	AEC_PK_2B	–	R	Bit[7:4]: real_gain_isp_fine[3:0] Bit[3:0]: Not used
0x35AC	AEC_PK_2C	–	R	Bit[7:0]: expo_fine_cur[15:8]
0x35AD	AEC_PK_2D	–	R	Bit[7:1]: Not used Bit[0]: r_otp_gain_man_coarse
0x35AE	AEC_PK_2E	0x00	RW	Bit[7:0]: r_otp_gain_auto_fine[9:2]
0x35AF	AEC_PK_2F	0x00	RW	Bit[7:6]: r_otp_gain_auto_fine[1:0] Bit[5:0]: Not used
0x35B0	AEC_PK_30	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_gb[3:0]
0x35B1	AEC_PK_31	–	R	Bit[7:0]: cur_dig_gain_fine_gb[9:2]
0x35B2	AEC_PK_32	–	R	Bit[7:6]: cur_dig_gain_fine_gb[1:0] Bit[5:0]: Not used
0x35B3	AEC_PK_33	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_gr[3:0]
0x35B4	AEC_PK_34	–	R	Bit[7:0]: cur_dig_gain_fine_gr[9:2]
0x35B5	AEC_PK_35	–	R	Bit[7:6]: cur_dig_gain_fine_gr[1:0] Bit[5:0]: Not used
0x35B6	AEC_PK_36	–	R	Bit[7:4]: Not used Bit[3:0]: cur_dig_gain_coarse_r[3:0]

table 6-9 AEC_PK_S registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x35B7	AEC_PK_37	–	R	Bit[7:0]: cur_dig_gain_fine_r[9:2]
0x35B8	AEC_PK_38	–	R	Bit[7:6]: cur_dig_gain_fine_r[1:0] Bit[5:0]: Not used
0x35B9	AEC_PK_39	–	R	Bit[7:0]: real_gain_isp_complete[39:32]
0x35BA	AEC_PK_3A	–	R	Bit[7:0]: real_gain_isp_complete[31:24]
0x35BB	AEC_PK_3B	–	R	Bit[7:0]: real_gain_isp_complete[23:16]
0x35BC	AEC_PK_3C	–	R	Bit[7:0]: real_gain_isp_complete[15:8]
0x35BD	AEC_PK_3D	–	R	Bit[7:0]: real_gain_isp_complete[7:0]
0x35BE	AEC_PK_3E	0x10	RW	Bit[7:5]: Not used Bit[4]: sig_gain_en Bit[3]: sig_gain_man_en Bit[2:0]: sig_gain_man
0x35BF	AEC_PK_3F	0x80	RW	Bit[7:0]: ideal_low_sig_gain

6.10 ANALOG_REG [0x3600 - 0x365B]

table 6-10 ANALOG_REG registers

address	register name	default value	R/W	description
0x3600~ 0x365B	ANA_0~ANA_91	–	–	Analog Registers

6.11 CORE_REG [0x3680 - 0x36C1]

table 6-11 CORE_REG registers

address	register name	default value	R/W	description
0x3680~ 0x36C1	CORE_0~CORE_65	–	–	Core Registers

6.12 SENSOR_REG [0x3700 - 0x37FF]

table 6-12 SENSOR_REG registers

address	register name	default value	R/W	description
0x3700~ 0x37FF	REG00~REGFF	–	–	Sensor Registers

6.13 TIMING_CTRL [0x3800 - 0x38F2]

table 6-13 TIMING_CTRL registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x3800	TIMING_CTRL_0	0x00	RW	Bit[7:0]: Array horizontal start point[15:8]
0x3801	TIMING_CTRL_1	0x00	RW	Bit[7:0]: Array horizontal start point[7:0]
0x3802	TIMING_CTRL_2	0x00	RW	Bit[7:0]: Array vertical start point[15:8]
0x3803	TIMING_CTRL_3	0x00	RW	Bit[7:0]: Array vertical start point[7:0]
0x3804	TIMING_CTRL_4	0x24	RW	Bit[7:0]: Array horizontal end point[15:8]
0x3805	TIMING_CTRL_5	0x3F	RW	Bit[7:0]: Array horizontal end point[7:0]
0x3806	TIMING_CTRL_6	0x1B	RW	Bit[7:0]: Array vertical end point[15:8]
0x3807	TIMING_CTRL_7	0x3F	RW	Bit[7:0]: Array vertical end point[7:0]
0x3808	TIMING_CTRL_8	0x24	RW	Bit[7:0]: ISP horizontal output width[15:8]
0x3809	TIMING_CTRL_9	0x20	RW	Bit[7:0]: ISP horizontal output width[7:0]
0x380A	TIMING_CTRL_10	0x1B	RW	Bit[7:0]: ISP vertical output height[15:8]
0x380B	TIMING_CTRL_11	0x20	RW	Bit[7:0]: ISP vertical output height[7:0]
0x380C	TIMING_CTRL_12	0x02	RW	Bit[7:0]: Total horizontal timing size[15:8]
0x380D	TIMING_CTRL_13	0x94	RW	Bit[7:0]: Total horizontal timing size[7:0]
0x380E	TIMING_CTRL_14	0x1D	RW	Bit[7:0]: Total vertical timing size[15:8]
0x380F	TIMING_CTRL_15	0x98	RW	Bit[7:0]: Total vertical timing size[7:0]
0x3810	TIMING_CTRL_16	0x00	RW	Bit[7:0]: ISP horizontal windowing offset[15:8]
0x3811	TIMING_CTRL_17	0x10	RW	Bit[7:0]: ISP horizontal windowing offset[7:0]
0x3812	TIMING_CTRL_18	0x00	RW	Bit[7:0]: ISP vertical windowing offset[15:8]

table 6-13 TIMING_CTRL registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x3813	TIMING_CTRL_19	0x10	RW	Bit[7:0]: ISP vertical windowing offset[7:0]
0x3814	TIMING_CTRL_20	0x11	RW	Bit[7:4]: X odd increase number Bit[3:0]: X even increase number
0x3815	TIMING_CTRL_21	0x11	RW	Bit[7:4]: Y odd increase number Bit[3:0]: Y even increase number
0x3816	TIMING_CTRL_22	0x00	RW	Bit[7:0]: HSYNC start point[15:8]
0x3817	TIMING_CTRL_23	0x00	RW	Bit[7:0]: HSYNC start point[7:0]
0x3818	TIMING_CTRL_24	0x00	RW	Bit[7:0]: HSYNC end point[15:8]
0x3819	TIMING_CTRL_25	0x20	RW	Bit[7:0]: HSYNC end point[7:0]
0x381A	TIMING_CTRL_26	0x00	RW	Bit[7:0]: VSYNC start row[15:8]
0x381B	TIMING_CTRL_27	0x00	RW	Bit[7:0]: VSYNC start row[7:0]
0x381C	TIMING_CTRL_28	0x00	RW	Bit[7:0]: VSYNC start column[15:8]
0x381D	TIMING_CTRL_29	0x00	RW	Bit[7:0]: VSYNC start column[7:0]
0x381E	TIMING_CTRL_30	0x00	RW	Bit[7:0]: VSYNC width[15:8]
0x381F	TIMING_CTRL_31	0x00	RW	Bit[7:0]: VSYNC width[7:0]
0x3820	TIMING_CTRL_32	0x40	RW	Bit[7]: Black row high sub ratio mode Bit[6]: Row address jump8 mode Bit[5]: Digital vertical 4x bin Bit[4]: Digital vertical 4x sub Bit[3]: 3 exposure mode enable Bit[2]: Vertical flip Bit[1]: Array vertical 4-cell bin Bit[0]: Array vertical fast bin
0x3821	TIMING_CTRL_33	0x00	RW	Bit[7:6]: Digital horizontal 4x bin mode Bit[5]: 2-exposure HDR mode Bit[4]: 4-cell horizontal bin mode Bit[3]: Analog hbin2 mode Bit[2]: Mirror Bit[1]: Half speed read out mode Bit[0]: Double speed read out mode

table 6-13 TIMING_CTRL registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x3822	TIMING_CTRL_34	0x00	RW	Bit[7]: 4x vertical scale control for ISP RAW bin Bit[6]: 2x vertical scale control for ISP RAW bin Bit[5]: 4x horizontal scale control for ISP RAW bin Bit[4]: 2x horizontal scale control for ISP RAW bin Bit[3]: Pre-charge 4x skipped row enable Bit[2]: Pre-charge skipped TX Bit[1]: Pre-charge skipped row enable for second format Bit[0]: Pre-charge skipped row enable
0x3823	TIMING_CTRL_35	0x04	RW	Bit[7]: Stagger HDR enable Bit[6]: Stagger-HDR number 0: 2-expo 1: 3-expo Bit[5]: Medium/short exposure clipped by BLC row number enable Bit[4]: Stagger HDR BLC number manual enable Bit[3]: Stagger HDR reset point manual enable for medium exposure Bit[2]: Four cell mode enable Bit[1:0]: Stagger HDR reset point manual enable for short exposure
0x3824	TIMING_CTRL_36	0x00	RW	Bit[7:0]: CS reset value at vs_ext[15:8]
0x3825	TIMING_CTRL_37	0x00	RW	Bit[7:0]: CS reset value at vs_ext[7:0]
0x3826	TIMING_CTRL_38	0x00	RW	Bit[7:0]: R reset value at vs_ext[15:8]
0x3827	TIMING_CTRL_39	0x40	RW	Bit[7:0]: R reset value at vs_ext[7:0]
0x3828	TIMING_CTRL_40	0x07	RW	Bit[7:0]: Frame exposure VTS adjust option
0x3829	TIMING_CTRL_41	0x04	RW	Bit[7:0]: Group write launch ahead row number reference to frame end
0x382A	TIMING_CTRL_42	0x82	RW	Bit[7]: Generate internal first frame flag (frame after wakeup) Bit[6]: VTS take effect in 2 frames after written enable Bit[5:4]: Threshold for line difference in VTS auto adjust mode Bit[3]: VTS auto adjust mode enable for frame sync Bit[2]: VTS manual adjust enable Bit[1]: VTS auto extension enable Bit[0]: Move group write forward to pipeline end point

table 6-13 TIMING_CTRL registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x382B	TIMING_CTRL_43	0x10	RW	Bit[7:0]: Group write trigger point after entering vblanking
0x382C	TIMING_CTRL_44	0x00	RW	Bit[7:0]: Fractional adjust mode[15:8]
0x382D	TIMING_CTRL_45	0x00	RW	Bit[7:0]: Fractional adjust mode[7:0]
0x382E	TIMING_CTRL_46	0x71	RW	Bit[7:6]: Disable FSIN adjustment Bit[5:4]: Exposure select for VSYNC output in staggered HDR mode Bit[3]: Staggered HDR group write point option Bit[2]: Manual long/medium/short distance enable Bit[1]: No mask for sleep in stagger HDR mode Bit[0]: No mask for group hold in stagger HDR mode
0x382F	TIMING_CTRL_47	0x01	RW	Bit[7:0]: Staggered HDR BLC manual row number
0x3830	TIMING_CTRL_48	0x07	RW	Bit[7:0]: Staggered HDR medium/short exposure adjust number
0x3831	NOT USED	–	–	Not Used
0x3832	TIMING_CTRL_50	0x00	RW	Bit[7:0]: Manual VTS adjust line number[15:8]
0x3833	TIMING_CTRL_51	0x00	RW	Bit[7:0]: Manual VTS adjust line number[7:0]
0x3834	TIMING_CTRL_52	0x80	RW	Bit[7:0]: Adjust threshold for entering double VTS in VTS auto adjust mode
0x3835	TIMING_CTRL_53	0x00	RW	Bit[7:0]: Auto VTS adjust mode sync row number[15:8]
0x3836	TIMING_CTRL_54	0x00	RW	Bit[7:0]: Auto VTS adjust mode sync row number[7:0]
0x3837	TIMING_CTRL_55	0x07	RW	Bit[7:0]: VTS auto extension additional rows
0x3838	TIMING_CTRL_56	0x00	RW	Bit[7]: threshold_vts_sub 0: For shift right 1: For shift left Bit[6:0]: Horizontal start shift pixel number
0x3839	TIMING_CTRL_57	0x00	RW	Bit[7]: threshold_vts_sub 0: For shift down 1: For shift up Bit[6:0]: Vertical start shift pixel number

table 6-13 TIMING_CTRL registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x383A	TIMING_CTRL_58	0x00	RW	Bit[7]: threshold_vts_sub 0: For shift right 1: For shift left Bit[6:0]: Horizontal offset shift
0x383B	TIMING_CTRL_59	0x00	RW	Bit[7]: threshold_vts_sub 0: For shift down 1: For shift up Bit[6:0]: Vertical offset shift
0x383C~ 0x383D	NOT USED	–	–	Not Used
0x383E	TIMING_CTRL_62	0x00	RW	Bit[7:4]: Staggered HDR fine exposure reset point Bit[3:0]: Staggered HDR normal exposure reset point
0x383F	TIMING_CTRL_63	0x00	RW	Bit[7:4]: Reserved Bit[3]: SOF from rend enable Bit[2]: DPD mode Bit[1]: HDR_expo_remap Bit[0]: HDR 3-expo 121 mode enable
0x3840	TIMING_CTRL_64	0x00	RW	Bit[7:0]: Total vertical timing size[23:16]
0x3841	TIMING_CTRL_65	0x00	RW	Bit[7:0]: VSYNC start row[23:16]
0x3842	TIMING_CTRL_66	0x00	RW	Bit[7:0]: R reset value at vs_ext[23:16]
0x3843	TIMING_CTRL_67	0x00	RW	Bit[7:0]: Auto VTS adjust mode sync row number[23:16]
0x3844	TIMING_CTRL_68	0x00	RW	Bit[7:0]: Frame sync output row start[23:16]
0x3845	TIMING_CTRL_69	0x00	RW	Bit[7:0]: Staggered HDR medium exposure reset point[23:16]
0x3846	TIMING_CTRL_70	0x00	RW	Bit[7:0]: Staggered HDR medium exposure reset point[15:8]
0x3847	TIMING_CTRL_71	0x00	RW	Bit[7:0]: Staggered HDR medium exposure reset point[7:0]
0x3848	TIMING_CTRL_72	0x00	RW	Bit[7:0]: Staggered HDR short exposure reset point[23:16]
0x3849	TIMING_CTRL_73	0x00	RW	Bit[7:0]: Staggered HDR short exposure reset point[15:8]
0x384A	TIMING_CTRL_74	0x00	RW	Bit[7:0]: Staggered HDR short exposure reset point[7:0]
0x384B	NOT USED	–	–	Not Used

table 6-13 TIMING_CTRL registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x384C	TIMING_CTRL_76	0x02	RW	Bit[7:0]: Second format total horizontal timing size[15:8]
0x384D	TIMING_CTRL_77	0x94	RW	Bit[7:0]: Second format total horizontal timing size[7:0]
0x384E	TIMING_CTRL_78	0x03	RW	Bit[7:2]: Reserved Bit[1:0]: Context switch sync frame selection group 8~9[9:8]
0x384F	TIMING_CTRL_79	0xFF	RW	Bit[7:0]: Context switch sync frame selection group 0~7[7:0]
0x3850	TIMING_CTRL_80	0x00	RW	Bit[7:0]: Manual long to medium distance[23:16]
0x3851	TIMING_CTRL_81	0x00	RW	Bit[7:0]: Manual long to medium distance[15:8]
0x3852	TIMING_CTRL_82	0x00	RW	Bit[7:0]: Manual long to medium distance[7:0]
0x3853	TIMING_CTRL_83	0x00	RW	Bit[7:0]: Manual medium to short distance[23:16]
0x3854	TIMING_CTRL_84	0x00	RW	Bit[7:0]: Manual medium to short distance[15:8]
0x3855	TIMING_CTRL_85	0x00	RW	Bit[7:0]: Manual medium to short distance[7:0]
0x3856	TIMING_CTRL_86	0x00	RW	Bit[7:0]: PD window horizontal additional offset
0x3857	TIMING_CTRL_87	0x00	RW	Bit[7:0]: PD window vertical additional offset
0x3858	TIMING_CTRL_88	0x20	RW	Bit[7:0]: PD window horizontal size additional cut number
0x3859	TIMING_CTRL_89	0x00	RW	Bit[7:0]: PD window vertical size additional cut number
0x385A	TIMING_CTRL_90	0x00	RW	Bit[7:0]: vblk_sw ahead row number reference to frame end
0x385B	TIMING_CTRL_91	0x00	RW	Bit[7:4]: Frame sync glitch filter cycle number Bit[3]: VSYNC output polarity 0: High level 1: Low level Bit[2]: Frame sync output polarity 0: High level 1: Low level Bit[1]: vs_ext_sync_lms_en Bit[0]: sof_option
0x385C	TIMING_CTRL_92	0x00	RW	Bit[7:0]: Frame sync output row start[15:8]
0x385D	TIMING_CTRL_93	0x00	RW	Bit[7:0]: Frame sync output row start[7:0]
0x385E	TIMING_CTRL_94	0x00	RW	Bit[7:0]: Frame sync output column start[15:8]

table 6-13 TIMING_CTRL registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x385F	TIMING_CTRL_95	0x00	RW	Bit[7:0]: Frame sync output column start[7:0]
0x3860~ 0x3862	NOT USED	–	–	Not Used
0x3863	TIMING_CTRL_99	0x00	RW	Bit[7:0]: Frame sync output width[15:8]
0x3864	TIMING_CTRL_100	0x00	RW	Bit[7:0]: Frame sync output width[7:0]
0x3865	TIMING_CTRL_101	0x00	RW	Bit[7]: Row counter initial value manual mode enable Bit[6]: Fix row counter before external frame sync signal coming enable (slave) Bit[5]: External frame sync signal reverse (slave) Bit[4]: External frame sync signal trigger enable (slave) Bit[3:0]: Sync for every N frame in frame sync mode (slave)
0x3866	TIMING_CTRL_102	0x0F	RW	Bit[7]: VBLK switch settings (a->b->a) for analog Bit[6:4]: Setting B duration Bit[3:0]: Context switch selection for frame sync mode
0x3867	TIMING_CTRL_103	0x14	RW	Bit[7:0]: First section hsize out of two sections[15:8]
0x3868	TIMING_CTRL_104	0x00	RW	Bit[7:0]: First section hsize out of two sections[7:0]
0x3869	TIMING_CTRL_105	0x00	RW	Bit[7:0]: manu_sof_offset
0x386A	TIMING_CTRL_106	0x00	RW	Bit[7:0]: manu_eof_offset[23:16]
0x386B	TIMING_CTRL_107	0x00	RW	Bit[7:0]: manu_eof_offset[15:8]
0x386C	TIMING_CTRL_108	0x00	RW	Bit[7:0]: manu_eof_offset[7:0]
0x386D~ 0x386F	NOT USED	–	–	Not Used
0x3870	TIMING_CTRL_112	–	R	Bit[7:0]: Auto size horizontal start[15:8]
0x3871	TIMING_CTRL_113	–	R	Bit[7:0]: Auto size horizontal start[7:0]
0x3872	TIMING_CTRL_114	–	R	Bit[7:0]: Auto size vertical start[15:8]
0x3873	TIMING_CTRL_115	–	R	Bit[7:0]: Auto size vertical start[7:0]
0x3874	TIMING_CTRL_116	–	R	Bit[7:0]: Auto size horizontal end[15:8]
0x3875	TIMING_CTRL_117	–	R	Bit[7:0]: Auto size horizontal end[7:0]
0x3876	TIMING_CTRL_118	–	R	Bit[7:0]: Auto size vertical end[15:8]

table 6-13 TIMING_CTRL registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x3877	TIMING_CTRL_119	–	R	Bit[7:0]: Auto size vertical end[7:0]
0x3878	TIMING_CTRL_120	–	R	Bit[7:0]: Auto size ISP horizontal output width[15:8]
0x3879	TIMING_CTRL_121	–	R	Bit[7:0]: Auto size ISP horizontal output width[7:0]
0x387A	TIMING_CTRL_122	–	R	Bit[7:0]: Auto size ISP vertical output width[15:8]
0x387B	TIMING_CTRL_123	–	R	Bit[7:0]: Auto size isp vertical output width[7:0]
0x387C	TIMING_CTRL_124	–	R	Bit[7:0]: Row counter on fly[15:8]
0x387D	TIMING_CTRL_125	–	R	Bit[7:0]: Row counter on fly[7:0]
0x387E	TIMING_CTRL_126	–	R	Bit[7:0]: Frame counter on fly[15:8]
0x387F	TIMING_CTRL_127	–	R	Bit[7:0]: Frame counter on fly[7:0]
0x3880	TIMING_CTRL_128	–	R	Bit[7:0]: Vertical blanking row number[23:16]
0x3881	TIMING_CTRL_129	–	R	Bit[7:0]: Vertical blanking row number[15:8]
0x3882	TIMING_CTRL_130	–	R	Bit[7:0]: Vertical blanking row number[7:0]
0x3883~ 0x3887	NOT USED	–	–	Not Used
0x3888	TIMING_CTRL_136	0x00	RW	Bit[7:0]: isp_x_win_pd[15:8]
0x3889	TIMING_CTRL_137	0x08	RW	Bit[7:0]: isp_x_win_pd[7:0]
0x388A	TIMING_CTRL_138	0x00	RW	Bit[7:0]: isp_y_win_pd[15:8]
0x388B	TIMING_CTRL_139	0x08	RW	Bit[7:0]: isp_y_win_pd[7:0]
0x388C	TIMING_CTRL_140	0x00	RW	Bit[7:0]: isp_x_width_pd[15:8]
0x388D	TIMING_CTRL_141	0x00	RW	Bit[7:0]: isp_x_width_pd[7:0]
0x388E	TIMING_CTRL_142	0x00	RW	Bit[7:0]: isp_y_height_pd[15:8]
0x388F	TIMING_CTRL_143	0x00	RW	Bit[7:0]: isp_y_height_pd[7:0]
0x3890	TIMING_CTRL_144	0x18	RW	Bit[7:0]: First section hsize out of two sections for second exposure[15:8]
0x3891	TIMING_CTRL_145	0x00	RW	Bit[7:0]: First section hsize out of two sections for second exposure[7:0]
0x3892	TIMING_CTRL_146	0x14	RW	Bit[7:0]: First section hsize out of two sections for third exposure[15:8]
0x3893	TIMING_CTRL_147	0x00	RW	Bit[7:0]: First section hsize out of two sections for third exposure[7:0]

table 6-13 TIMING_CTRL registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x3894	TIMING_CTRL_148	0x00	RW	Bit[7:4]: Reserved Bit[3]: Auto adjust LM distance to an odd number Bit[2]: Auto adjust MS distance to an odd number Bit[1]: Auto adjust LM distance to an even number Bit[0]: Auto adjust MS distance to an even number
0x3895~ 0x38EF	NOT USED	–	–	Not Used
0x38F0	TIMING_CTRL_240	–	W	Bit[7:1]: Not used Bit[0]: Trigger
0x38F1	TIMING_CTRL_241	–	W	Bit[7:1]: Not used Bit[0]: Trigger
0x38F2	TIMING_CTRL_242	–	W	Bit[7:2]: Not used Bit[1]: format_chg_manual_intr Bit[0]: format_chg_manual_rst

6.14 SENSOR_REG1 [0x3900 - 0x3A7D]

table 6-14 SENSOR_REG1 registers (sheet 1 of 24)

address	register name	default value	R/W	description
0x3900	REG000	0x00	RW	Bit[7]: r_y_rs_even_re Bit[6]: r_y_rs_even_all0_lcg Bit[5]: r_y_rs_even_all0_hcg Bit[4]: r_y_rs_odd_re Bit[3]: r_y_rs_odd_all0_lcg Bit[2]: r_y_rs_odd_all0_hcg Bit[1]: r_y_rp_rst_even_re Bit[0]: r_y_rp_rst_even_all0_lcg
0x3901	REG001	0x00	RW	Bit[7]: r_y_rp_rst_even_all0_hcg Bit[6]: r_y_rp_rst_odd_re Bit[5]: r_y_rp_rst_odd_all0_lcg Bit[4]: r_y_rp_rst_odd_all0_hcg Bit[3]: r_y_dfd_rp_en_even_re Bit[2]: r_y_dfd_rp_en_even_all0_lcg Bit[1]: r_y_dfd_rp_en_even_all0_hcg Bit[0]: r_y_dfd_rp_en_odd_re

table 6-14 SENSOR_REG1 registers (sheet 2 of 24)

address	register name	default value	R/W	description
0x3902	REG002	0x00	RW	Bit[7]: r_y_dfd_rp_en_odd_all0_lcg Bit[6]: r_y_dfd_rp_en_odd_all0_hcg Bit[5]: r_y_bst_neg_even_re Bit[4]: r_y_bst_neg_even_all0_lcg_16x Bit[3]: r_y_bst_neg_even_all0_hcg_16x Bit[2]: r_y_bst_neg_even_all0_lcg_8x Bit[1]: r_y_bst_neg_even_all0_hcg_8x Bit[0]: r_y_bst_neg_even_all0_lcg_4x
0x3903	REG003	0x00	RW	Bit[7]: r_y_bst_neg_even_all0_hcg_4x Bit[6]: r_y_bst_neg_even_all0_lcg_2x Bit[5]: r_y_bst_neg_even_all0_hcg_2x Bit[4]: r_y_bst_neg_even_all0_lcg_1x Bit[3]: r_y_bst_neg_even_all0_hcg_1x Bit[2]: r_y_bst_neg_odd_re Bit[1]: r_y_bst_neg_odd_all0_lcg_16x Bit[0]: r_y_bst_neg_odd_all0_hcg_16x
0x3904	REG004	0x00	RW	Bit[7]: r_y_bst_neg_odd_all0_lcg_8x Bit[6]: r_y_bst_neg_odd_all0_hcg_8x Bit[5]: r_y_bst_neg_odd_all0_lcg_4x Bit[4]: r_y_bst_neg_odd_all0_hcg_4x Bit[3]: r_y_bst_neg_odd_all0_lcg_2x Bit[2]: r_y_bst_neg_odd_all0_hcg_2x Bit[1]: r_y_bst_neg_odd_all0_lcg_1x Bit[0]: r_y_bst_neg_odd_all0_hcg_1x
0x3905	REG005	0x00	RW	Bit[7]: r_y_fdc_rp_en_even_re Bit[6]: r_y_fdc_rp_en_even_all0_lcg Bit[5]: r_y_fdc_rp_en_even_all0_hcg Bit[4]: r_y_fdc_rp_en_odd_re Bit[3]: r_y_fdc_rp_en_odd_all0_lcg Bit[2]: r_y_fdc_rp_en_odd_all0_hcg Bit[1]: r_y_col_cbar_en_re Bit[0]: r_y_col_cbar_en_all0
0x3906	REG006	0x00	RW	Bit[7]: r_y_pix_ecl_blk_en_lcg_re Bit[6]: r_y_pix_ecl_blk_en_lcg_all0 Bit[5]: r_y_pix_ecl_blk_en_hcg_re Bit[4]: r_y_pix_ecl_blk_en_hcg_all0 Bit[3]: r_y_pix_ecl_sig_en_lcg_re Bit[2]: r_y_pix_ecl_sig_en_lcg_all0_16x Bit[1]: r_y_pix_ecl_sig_en_lcg_all0_8x Bit[0]: r_y_pix_ecl_sig_en_lcg_all0_4x

table 6-14 SENSOR_REG1 registers (sheet 3 of 24)

address	register name	default value	R/W	description
0x3907	REG007	0x00	RW	Bit[7]: r_y_pix_ecl_sig_en_lcg_all0_2x Bit[6]: r_y_pix_ecl_sig_en_lcg_all0_1x Bit[5]: r_y_pix_ecl_sig_en_hcg_re Bit[4]: r_y_pix_ecl_sig_en_hcg_all0_16x Bit[3]: r_y_pix_ecl_sig_en_hcg_all0_8x Bit[2]: r_y_pix_ecl_sig_en_hcg_all0_4x Bit[1]: r_y_pix_ecl_sig_en_hcg_all0_2x Bit[0]: r_y_pix_ecl_sig_en_hcg_all0_1x
0x3908	REG008	0x00	RW	Bit[7]: r_y_pix_ecl_sig_en_top_btm_lcg_re Bit[6]: r_y_pix_ecl_sig_en_top_btm_lcg_all0 Bit[5]: r_y_pix_ecl_sig_en_top_btm_hcg_re Bit[4]: r_y_pix_ecl_sig_en_top_btm_hcg_all0 Bit[3]: r_y_pix_ecl_idle_en_top_btm_re Bit[2]: r_y_pix_ecl_idle_en_top_btm_all0_16x Bit[1]: r_y_pix_ecl_idle_en_top_btm_all0_8x Bit[0]: r_y_pix_ecl_idle_en_top_btm_all0_4x
0x3909	REG009	0x00	RW	Bit[7]: r_y_pix_ecl_idle_en_top_btm_all0_2x Bit[6]: r_y_pix_ecl_idle_en_top_btm_all0_1x Bit[5]: r_y_pix_ecl_idle_en_re Bit[4]: r_y_pix_ecl_idle_en_all0_16x Bit[3]: r_y_pix_ecl_idle_en_all0_8x Bit[2]: r_y_pix_ecl_idle_en_all0_4x Bit[1]: r_y_pix_ecl_idle_en_all0_2x Bit[0]: r_y_pix_ecl_idle_en_all0_1x
0x390A	REG00A	0x00	RW	Bit[7]: r_y_col_blsw_re Bit[6]: r_y_col_blsw_all0 Bit[5]: r_y_sh_vrhv1_re Bit[4]: r_y_sh_vrhv1_all0 Bit[3]: r_y_sh_vrhv2_re Bit[2]: r_y_sh_vrhv2_all0 Bit[1]: r_y_col_dcomp_vcn_sh_re Bit[0]: r_y_col_dcomp_vcn_sh_all0
0x390B	REG00B	0x00	RW	Bit[7]: r_y_col_dcomp_vbn_sh_re Bit[6]: r_y_col_dcomp_vbn_sh_all0 Bit[5]: r_y_col_rampbuf_vcn_sh_re Bit[4]: r_y_col_rampbuf_vcn_sh_all0 Bit[3]: r_y_col_rampbuf_vbn_sh_re Bit[2]: r_y_col_rampbuf_vbn_sh_all0 Bit[1]: r_y_col_vln_vcn_sh_re Bit[0]: r_y_col_vln_vcn_sh_all0

table 6-14 SENSOR_REG1 registers (sheet 4 of 24)

address	register name	default value	R/W	description
0x390C	REG00C	0x00	RW	Bit[7]: r_y_col_vln_vbn_sh_re Bit[6]: r_y_col_vln_vbn_sh_all0 Bit[5]: r_y_col_rampbuf_en_re Bit[4]: r_y_col_rampbuf_en_all0 Bit[3]: r_y_col_dcomp_en_re Bit[2]: r_y_col_dcomp_en_all0 Bit[1]: r_y_col_vln_en_re Bit[0]: r_y_col_vln_en_all0
0x390D	REG00D	0x00	RW	Bit[7]: r_y_col_dcomp1_rst1_re Bit[6]: r_y_col_dcomp1_rst1_all0 Bit[5]: r_y_col_dcomp1_rst2_re Bit[4]: r_y_col_dcomp1_rst2_all0 Bit[3]: r_y_col_dcomp2_rst_re Bit[2]: r_y_col_dcomp2_rst_all0 Bit[1]: r_y_col_dcomp3_en_re Bit[0]: r_y_col_dcomp3_en_all0
0x390E	REG00E	0x00	RW	Bit[7]: r_y_col_dcomp_fast_up_re Bit[6]: r_y_col_dcomp_fast_up_all0 Bit[5]: r_y_col_dcomp_bypass_casc_p_re Bit[4]: r_y_col_dcomp_bypass_casc_p_all0 Bit[3]: r_y_col_dcomp_bypass_casc_n_re Bit[2]: r_y_col_dcomp_bypass_casc_n_all0 Bit[1]: r_y_col_slpctrl_en_re Bit[0]: r_y_col_slpctrl_en_all0
0x390F	REG00F	0x00	RW	Bit[7]: r_y_col_fb_samp_en_re Bit[6]: r_y_col_fb_samp_en_all0 Bit[5]: r_y_col_fb_dcomp1_1_en_re Bit[4]: r_y_col_fb_dcomp1_1_en_all0 Bit[3]: r_y_col_fb_dcomp1_2_en_re Bit[2]: r_y_col_fb_dcomp1_2_en_all0 Bit[1]: r_y_col_count_lat_wen_bsun_re Bit[0]: r_y_col_count_lat_wen_bsun_all0
0x3910	REG010	0x00	RW	Bit[7]: r_y_col_count_sram_div_rst_re Bit[6]: r_y_col_count_sram_div_rst_all0 Bit[5]: r_y_col_count_gcgen_rst_re Bit[4]: r_y_col_count_gcgen_rst_all0 Bit[3]: r_y_col_count_lat_wen_blk_re Bit[2]: r_y_col_count_lat_wen_blk_all0 Bit[1]: r_y_col_count_lat_wen_sig_re Bit[0]: r_y_col_count_lat_wen_sig_all0

table 6-14 SENSOR_REG1 registers (sheet 5 of 24)

address	register name	default value	R/W	description
0x3911	REG011	0x00	RW	Bit[7]: r_y_col_count_lat_wen_mem_re Bit[6]: r_y_col_count_lat_wen_mem_all0 Bit[5]: r_y_ramp_integ_samp_re Bit[4]: r_y_ramp_integ_samp_all0 Bit[3]: r_y_ramp_vofs_samp_re Bit[2]: r_y_ramp_vofs_samp_all0 Bit[1]: r_y_ramp_vref_samp_re Bit[0]: r_y_ramp_vref_samp_all0
0x3912	REG012	0x00	RW	Bit[7]: r_y_psrr_dc_samp_re Bit[6]: r_y_psrr_dc_samp_all0 Bit[5]: r_y_psrr_act_rst_re Bit[4]: r_y_psrr_act_rst_all0 Bit[3]: r_y_ramp_voffset_en_re Bit[2]: r_y_ramp_voffset_en_all0 Bit[1]: r_y_ramp_buf_en_re Bit[0]: r_y_ramp_buf_en_all0
0x3913	REG013	0x00	RW	Bit[7]: r_y_ramp_cur_ass_samp_re Bit[6]: r_y_ramp_cur_ass_samp_all0 Bit[5]: r_y_ramp_current_bias_samp_re Bit[4]: r_y_ramp_current_bias_samp_all0 Bit[3]: r_y_ramp_vofs_reset_re Bit[2]: r_y_ramp_vofs_reset_all0 Bit[1]: r_y_ramp_assist_en_re Bit[0]: r_y_ramp_assist_en_all0
0x3914	REG014	0x00	RW	Bit[7]: r_y_ramp_assist_ctrl_en_re Bit[6]: r_y_ramp_assist_ctrl_en_all0 Bit[5:0]: Not used
0x3915	REG015	0x49	RW	Bit[7]: r_y_rs_even_rise_sel_scg_0_0 Bit[6]: r_y_rs_even_rise_sel_scg_0_1 Bit[5]: r_y_rs_even_rise_sel_scg_0_2 Bit[4]: r_y_rs_even_rise_sel_scg_1_0 Bit[3]: r_y_rs_even_rise_sel_scg_1_1 Bit[2]: r_y_rs_even_rise_sel_scg_1_2 Bit[1]: r_y_rs_odd_rise_sel_scg_0_0 Bit[0]: r_y_rs_odd_rise_sel_scg_0_1
0x3916	REG016	0x29	RW	Bit[7]: r_y_rs_odd_rise_sel_scg_0_2 Bit[6]: r_y_rs_odd_rise_sel_scg_1_0 Bit[5]: r_y_rs_odd_rise_sel_scg_1_1 Bit[4]: r_y_rs_odd_rise_sel_scg_1_2 Bit[3]: r_y_rp_rst_even_rise_sel_scg_0_0 Bit[2]: r_y_rp_rst_even_rise_sel_scg_0_1 Bit[1]: r_y_rp_rst_even_rise_sel_scg_0_2 Bit[0]: r_y_rp_rst_even_rise_sel_scg_1_0

table 6-14 SENSOR_REG1 registers (sheet 6 of 24)

address	register name	default value	R/W	description
0x3917	REG017	0x09	RW	Bit[7]: r_y_rp_rst_even_rise_sel_scg_1_1 Bit[6]: r_y_rp_rst_even_rise_sel_scg_1_2 Bit[5]: r_y_rp_rst_even_fall_sel_scg_0_0 Bit[4]: r_y_rp_rst_even_fall_sel_scg_1_0 Bit[3]: r_y_rp_rst_odd_rise_sel_scg_0_0 Bit[2]: r_y_rp_rst_odd_rise_sel_scg_0_1 Bit[1]: r_y_rp_rst_odd_rise_sel_scg_0_2 Bit[0]: r_y_rp_rst_odd_rise_sel_scg_1_0
0x3918	REG018	0x0A	RW	Bit[7]: r_y_rp_rst_odd_rise_sel_scg_1_1 Bit[6]: r_y_rp_rst_odd_rise_sel_scg_1_2 Bit[5]: r_y_rp_rst_odd_fall_sel_scg_0_0 Bit[4]: r_y_rp_rst_odd_fall_sel_scg_1_0 Bit[3]: r_y_dfd_rp_en_even_rise_sel_scg_0_0 Bit[2]: r_y_dfd_rp_en_even_rise_sel_scg_0_1 Bit[1]: r_y_dfd_rp_en_even_rise_sel_scg_1_0 Bit[0]: r_y_dfd_rp_en_even_rise_sel_scg_1_1
0x3919	REG019	0x4A	RW	Bit[7]: r_y_dfd_rp_en_even_fall_sel_scg_0_0 Bit[6]: r_y_dfd_rp_en_even_fall_sel_scg_0_1 Bit[5]: r_y_dfd_rp_en_even_fall_sel_scg_0_2 Bit[4]: r_y_dfd_rp_en_even_fall_sel_scg_1_0 Bit[3]: r_y_dfd_rp_en_even_fall_sel_scg_1_1 Bit[2]: r_y_dfd_rp_en_even_fall_sel_scg_1_2 Bit[1]: r_y_dfd_rp_en_odd_rise_sel_scg_0_0 Bit[0]: r_y_dfd_rp_en_odd_rise_sel_scg_0_1
0x391A	REG01A	0x92	RW	Bit[7]: r_y_dfd_rp_en_odd_rise_sel_scg_1_0 Bit[6]: r_y_dfd_rp_en_odd_rise_sel_scg_1_1 Bit[5]: r_y_dfd_rp_en_odd_fall_sel_scg_0_0 Bit[4]: r_y_dfd_rp_en_odd_fall_sel_scg_0_1 Bit[3]: r_y_dfd_rp_en_odd_fall_sel_scg_0_2 Bit[2]: r_y_dfd_rp_en_odd_fall_sel_scg_1_0 Bit[1]: r_y_dfd_rp_en_odd_fall_sel_scg_1_1 Bit[0]: r_y_dfd_rp_en_odd_fall_sel_scg_1_2
0x391B	REG01B	0xA4	RW	Bit[7]: r_y_bst_neg_even_rise_sel_scg_0_0 Bit[6]: r_y_bst_neg_even_rise_sel_scg_0_1 Bit[5]: r_y_bst_neg_even_rise_sel_scg_1_0 Bit[4]: r_y_bst_neg_even_rise_sel_scg_1_1 Bit[3]: r_y_bst_neg_even_fall_sel_scg_0_0 Bit[2]: r_y_bst_neg_even_fall_sel_scg_0_1 Bit[1]: r_y_bst_neg_even_fall_sel_scg_0_2 Bit[0]: r_y_bst_neg_even_fall_sel_scg_1_0

table 6-14 SENSOR_REG1 registers (sheet 7 of 24)

address	register name	default value	R/W	description
0x391C	REG01C	0xA9	RW	Bit[7]: r_y_bst_neg_even_fall_sel_scg_1_1 Bit[6]: r_y_bst_neg_even_fall_sel_scg_1_2 Bit[5]: r_y_bst_neg_odd_rise_sel_scg_0_0 Bit[4]: r_y_bst_neg_odd_rise_sel_scg_0_1 Bit[3]: r_y_bst_neg_odd_rise_sel_scg_1_0 Bit[2]: r_y_bst_neg_odd_rise_sel_scg_1_1 Bit[1]: r_y_bst_neg_odd_fall_sel_scg_0_0 Bit[0]: r_y_bst_neg_odd_fall_sel_scg_0_1
0x391D	REG01D	0x2A	RW	Bit[7]: r_y_bst_neg_odd_fall_sel_scg_0_2 Bit[6]: r_y_bst_neg_odd_fall_sel_scg_1_0 Bit[5]: r_y_bst_neg_odd_fall_sel_scg_1_1 Bit[4]: r_y_bst_neg_odd_fall_sel_scg_1_2 Bit[3]: r_y_fdc_rp_en_even_rise_sel_scg_0_0 Bit[2]: r_y_fdc_rp_en_even_rise_sel_scg_0_1 Bit[1]: r_y_fdc_rp_en_even_rise_sel_scg_1_0 Bit[0]: r_y_fdc_rp_en_even_rise_sel_scg_1_1
0x391E	REG01E	0xE8	RW	Bit[7]: r_y_fdc_rp_en_even_rise_sel_scg_2_0 Bit[6]: r_y_fdc_rp_en_even_rise_sel_scg_3_0 Bit[5]: r_y_fdc_rp_en_even_fall_sel_scg_0_0 Bit[4]: r_y_fdc_rp_en_even_fall_sel_scg_0_1 Bit[3]: r_y_fdc_rp_en_even_fall_sel_scg_1_0 Bit[2]: r_y_fdc_rp_en_even_fall_sel_scg_1_1 Bit[1]: r_y_fdc_rp_en_even_fall_sel_scg_2_0 Bit[0]: r_y_fdc_rp_en_even_fall_sel_scg_3_0
0x391F	REG01F	0xAE	RW	Bit[7]: r_y_fdc_rp_en_odd_rise_sel_scg_0_0 Bit[6]: r_y_fdc_rp_en_odd_rise_sel_scg_0_1 Bit[5]: r_y_fdc_rp_en_odd_rise_sel_scg_1_0 Bit[4]: r_y_fdc_rp_en_odd_rise_sel_scg_1_1 Bit[3]: r_y_fdc_rp_en_odd_rise_sel_scg_2_0 Bit[2]: r_y_fdc_rp_en_odd_rise_sel_scg_3_0 Bit[1]: r_y_fdc_rp_en_odd_fall_sel_scg_0_0 Bit[0]: r_y_fdc_rp_en_odd_fall_sel_scg_0_1
0x3920	REG020	0x8A	RW	Bit[7]: r_y_fdc_rp_en_odd_fall_sel_scg_1_0 Bit[6]: r_y_fdc_rp_en_odd_fall_sel_scg_1_1 Bit[5]: r_y_fdc_rp_en_odd_fall_sel_scg_2_0 Bit[4]: r_y_fdc_rp_en_odd_fall_sel_scg_3_0 Bit[3]: r_y_pix_ecl_blk_en_lcg_rise_sel_scg_0_0 Bit[2]: r_y_pix_ecl_blk_en_lcg_rise_sel_scg_0_1 Bit[1]: r_y_pix_ecl_blk_en_lcg_rise_sel_scg_1_0 Bit[0]: r_y_pix_ecl_blk_en_lcg_rise_sel_scg_1_1

table 6-14 SENSOR_REG1 registers (sheet 8 of 24)

address	register name	default value	R/W	description
0x3921	REG021	0x02	RW	Bit[7]: r_y_pix_ecl_blk_en_lcg_fall_sel_scg_0_0 Bit[6]: r_y_pix_ecl_blk_en_lcg_fall_sel_scg_0_1 Bit[5]: r_y_pix_ecl_blk_en_lcg_fall_sel_scg_0_2 Bit[4]: r_y_pix_ecl_blk_en_lcg_fall_sel_scg_1_0 Bit[3]: r_y_pix_ecl_blk_en_lcg_fall_sel_scg_1_1 Bit[2]: r_y_pix_ecl_blk_en_lcg_fall_sel_scg_1_2 Bit[1]: r_y_pix_ecl_blk_en_hcg_rise_sel_scg_0_0 Bit[0]: r_y_pix_ecl_blk_en_hcg_rise_sel_scg_0_1
0x3922	REG022	0x80	RW	Bit[7]: r_y_pix_ecl_blk_en_hcg_rise_sel_scg_1_0 Bit[6]: r_y_pix_ecl_blk_en_hcg_rise_sel_scg_1_1 Bit[5]: r_y_pix_ecl_blk_en_hcg_fall_sel_scg_0_0 Bit[4]: r_y_pix_ecl_blk_en_hcg_fall_sel_scg_0_1 Bit[3]: r_y_pix_ecl_blk_en_hcg_fall_sel_scg_0_2 Bit[2]: r_y_pix_ecl_blk_en_hcg_fall_sel_scg_1_0 Bit[1]: r_y_pix_ecl_blk_en_hcg_fall_sel_scg_1_1 Bit[0]: r_y_pix_ecl_blk_en_hcg_fall_sel_scg_1_2
0x3923	REG023	0x00	RW	Bit[7]: r_y_pix_ecl_sig_en_lcg_rise_sel_scg_0_0 Bit[6]: r_y_pix_ecl_sig_en_lcg_rise_sel_scg_1_0 Bit[5]: r_y_pix_ecl_sig_en_lcg_fall_sel_scg_0_0 Bit[4]: r_y_pix_ecl_sig_en_lcg_fall_sel_scg_1_0 Bit[3]: r_y_pix_ecl_sig_en_hcg_rise_sel_scg_0_0 Bit[2]: r_y_pix_ecl_sig_en_hcg_rise_sel_scg_1_0 Bit[1]: r_y_pix_ecl_sig_en_hcg_fall_sel_scg_0_0 Bit[0]: r_y_pix_ecl_sig_en_hcg_fall_sel_scg_1_0
0x3924	REG024	0xA5	RW	Bit[7]: r_y_pix_ecl_idle_en_top_btm_fall_sel_ncg_0_0 Bit[6]: r_y_pix_ecl_idle_en_top_btm_fall_sel_ncg_0_1 Bit[5]: r_y_pix_ecl_idle_en_fall_sel_ncg_0_0 Bit[4]: r_y_pix_ecl_idle_en_fall_sel_ncg_0_1 Bit[3]: r_y_col_blsw_rise_sel_ncg_0_0 Bit[2]: r_y_col_blsw_rise_sel_ncg_0_1 Bit[1]: r_y_col_blsw_rise_sel_ncg_0_2 Bit[0]: r_y_col_blsw_rise_sel_ncg_1_0
0x3925	REG025	0x0F	RW	Bit[7]: r_y_col_blsw_fall_sel_ncg_0_0 Bit[6]: r_y_col_blsw_fall_sel_ncg_0_1 Bit[5]: r_y_col_blsw_fall_sel_ncg_0_2 Bit[4]: r_y_col_blsw_fall_sel_ncg_1_0 Bit[3]: r_y_sh_vrhv1_fall_sel_ncg_0_0 Bit[2]: r_y_sh_vrhv2_fall_sel_ncg_0_0 Bit[1]: r_y_col_dcomp_vcn_sh_fall_sel_ncg_0_0 Bit[0]: r_y_col_dcomp_vbn_sh_fall_sel_ncg_0_0

table 6-14 SENSOR_REG1 registers (sheet 9 of 24)

address	register name	default value	R/W	description
0x3926	REG026	0xFE	RW	Bit[7]: r_y_col_rampbuf_vcn_sh_fall_sel_ncg_0_0 Bit[6]: r_y_col_rampbuf_vbn_sh_fall_sel_ncg_0_0 Bit[5]: r_y_col_vln_vcn_sh_fall_sel_ncg_0_0 Bit[4]: r_y_col_vln_vbn_sh_fall_sel_ncg_0_0 Bit[3]: r_y_col_rampbuf_en_rise_sel_ncg_0_0 Bit[2]: r_y_col_dcomp_en_rise_sel_ncg_0_0 Bit[1]: r_y_col_vln_en_rise_sel_ncg_0_0 Bit[0]: r_y_col_dcomp1_rst1_rise_sel_ncg_0_0
0x3927	REG027	0xAA	RW	Bit[7]: r_y_col_dcomp1_rst1_rise_sel_ncg_0_1 Bit[6]: r_y_col_dcomp1_rst2_rise_sel_ncg_0_0 Bit[5]: r_y_col_dcomp1_rst2_rise_sel_ncg_0_1 Bit[4]: r_y_col_dcomp2_rst_rise_sel_ncg_0_0 Bit[3]: r_y_col_dcomp2_rst_rise_sel_ncg_0_1 Bit[2]: r_y_col_dcomp2_rst_fall_sel_ncg_0_0 Bit[1]: r_y_col_dcomp_fast_up_rise_sel_ncg_0_0 Bit[0]: r_y_col_dcomp_fast_up_rise_sel_ncg_0_1
0x3928	REG028	0x95	RW	Bit[7]: r_y_col_fb_samp_en_rise_sel_ncg_0_0 Bit[6]: r_y_col_fb_samp_en_rise_sel_ncg_0_1 Bit[5]: r_y_col_fb_samp_en_rise_sel_ncg_0_2 Bit[4]: r_y_col_fb_dcomp1_1_en_rise_sel_ncg_0_0 Bit[3]: r_y_col_fb_dcomp1_1_en_fall_sel_ncg_0_0 Bit[2]: r_y_col_fb_dcomp1_2_en_rise_sel_ncg_0_0 Bit[1]: r_y_col_fb_dcomp1_2_en_fall_sel_ncg_0_0 Bit[0]: r_y_col_count_lat_wen_blk_rise_sel_ncg_0_0
0x3929	REG029	0x80	RW	Bit[7]: r_y_col_count_lat_wen_blk_fall_sel_ncg_0_0 Bit[6]: r_y_col_count_lat_wen_sig_rise_sel_ncg_0_0 Bit[5]: r_y_col_count_lat_wen_sig_rise_sel_ncg_0_1 Bit[4]: r_y_col_count_lat_wen_sig_fall_sel_ncg_0_0 Bit[3]: r_y_col_count_lat_wen_sig_fall_sel_ncg_0_1 Bit[2]: r_y_col_count_lat_wen_mem_rise_sel_ncg_0_0 Bit[1]: r_y_col_count_lat_wen_mem_rise_sel_ncg_0_1 Bit[0]: r_y_col_count_lat_wen_mem_fall_sel_ncg_0_0
0x392A	REG02A	0x2A	RW	Bit[7]: r_y_col_count_lat_wen_mem_fall_sel_ncg_0_1 Bit[6]: r_y_ramp_integ_samp_rise_sel_ncg_0_0 Bit[5]: r_y_ramp_integ_samp_fall_sel_ncg_0_0 Bit[4]: r_y_ramp_vofs_samp_rise_sel_ncg_0_0 Bit[3]: r_y_ramp_vofs_samp_fall_sel_ncg_0_0 Bit[2]: r_y_ramp_vref_samp_rise_sel_ncg_0_0 Bit[1]: r_y_ramp_vref_samp_fall_sel_ncg_0_0 Bit[0]: r_y_psrr_dc_samp_rise_sel_ncg_0_0

table 6-14 SENSOR_REG1 registers (sheet 10 of 24)

address	register name	default value	R/W	description
0x392B	REG02B	0xAA	RW	Bit[7]: r_y_psrr_dc_samp_fall_sel_ncg_0_0 Bit[6]: r_y_psrr_act_rst_rise_sel_ncg_0_0 Bit[5]: r_y_psrr_act_rst_fall_sel_ncg_0_0 Bit[4]: r_y_ramp_voffset_en_fall_sel_ncg_0_0 Bit[3]: r_y_ramp_buf_en_rise_sel_ncg_0_0 Bit[2]: r_y_ramp_cur_ass_samp_rise_sel_ncg_0_0 Bit[1]: r_y_ramp_cur_ass_samp_fall_sel_ncg_0_0 Bit[0]: r_y_ramp_current_bias_samp_rise_sel_ncg_0_0
0x392C	REG02C	0xB0	RW	Bit[7]: r_y_ramp_current_bias_samp_fall_sel_ncg_0_0 Bit[6]: r_y_ramp_vofs_reset_rise_sel_ncg_0_0 Bit[5]: r_y_ramp_vofs_reset_fall_sel_ncg_0_0 Bit[4]: r_y_ramp_assist_en_fall_sel_ncg_0_0 Bit[3]: r_y_ramp_assist_ctrl_en_fall_sel_ncg_0_0 Bit[2:0]: Not used
0x392D	REG02D	0x04	RW	Bit[7:0]: r_y_rs_even_rise_opt_scg_0[7:0]
0x392E	REG02E	0x04	RW	Bit[7:0]: r_y_rs_even_rise_opt_scg_1[7:0]
0x392F	REG02F	0x00	RW	Bit[7:0]: r_y_rs_even_rise_scg_0[15:8]
0x3930	REG030	0x00	RW	Bit[7:0]: r_y_rs_even_rise_scg_0[7:0]
0x3931	REG031	0x00	RW	Bit[7:0]: r_y_rs_even_rise_scg_1[15:8]
0x3932	REG032	0x00	RW	Bit[7:0]: r_y_rs_even_rise_scg_1[7:0]
0x3933	REG033	0x00	RW	Bit[7:0]: r_y_rs_even_fall_scg_0[7:0]
0x3934	REG034	0x04	RW	Bit[7:0]: r_y_rs_even_fall_scg_1[7:0]
0x3935	REG035	0x00	RW	Bit[7:0]: r_y_rs_even_fall_scg_2[7:0]
0x3936	REG036	0x04	RW	Bit[7:0]: r_y_rs_even_fall_scg_3[7:0]
0x3937	REG037	0x04	RW	Bit[7:0]: r_y_rs_odd_rise_opt_scg_0[7:0]
0x3938	REG038	0x04	RW	Bit[7:0]: r_y_rs_odd_rise_opt_scg_1[7:0]
0x3939	REG039	0x00	RW	Bit[7:0]: r_y_rs_odd_rise_scg_0[15:8]
0x393A	REG03A	0x00	RW	Bit[7:0]: r_y_rs_odd_rise_scg_0[7:0]
0x393B	REG03B	0x00	RW	Bit[7:0]: r_y_rs_odd_rise_scg_1[15:8]
0x393C	REG03C	0x00	RW	Bit[7:0]: r_y_rs_odd_rise_scg_1[7:0]
0x393D	REG03D	0x00	RW	Bit[7:0]: r_y_rs_odd_fall_scg_0[7:0]
0x393E	REG03E	0x04	RW	Bit[7:0]: r_y_rs_odd_fall_scg_1[7:0]
0x393F	REG03F	0x00	RW	Bit[7:0]: r_y_rs_odd_fall_scg_2[7:0]

table 6-14 SENSOR_REG1 registers (sheet 11 of 24)

address	register name	default value	R/W	description
0x3940	REG040	0x04	RW	Bit[7:0]: r_y_rs_odd_fall_scg_3[7:0]
0x3941	REG041	0x02	RW	Bit[7:0]: r_y_rp_rst_even_rise_opt_scg_0[7:0]
0x3942	REG042	0x02	RW	Bit[7:0]: r_y_rp_rst_even_rise_opt_scg_1[7:0]
0x3943	REG043	0x02	RW	Bit[7:0]: r_y_rp_rst_even_fall_opt_scg_0[7:0]
0x3944	REG044	0x02	RW	Bit[7:0]: r_y_rp_rst_even_fall_opt_scg_1[7:0]
0x3945	REG045	0x02	RW	Bit[7:0]: r_y_rp_rst_odd_rise_opt_scg_0[7:0]
0x3946	REG046	0x02	RW	Bit[7:0]: r_y_rp_rst_odd_rise_opt_scg_1[7:0]
0x3947	REG047	0x02	RW	Bit[7:0]: r_y_rp_rst_odd_fall_opt_scg_0[7:0]
0x3948	REG048	0x02	RW	Bit[7:0]: r_y_rp_rst_odd_fall_opt_scg_1[7:0]
0x3949	REG049	0x02	RW	Bit[7:0]: r_y_dfd_rp_en_even_rise_opt_scg_0[7:0]
0x394A	REG04A	0x02	RW	Bit[7:0]: r_y_dfd_rp_en_even_rise_opt_scg_1[7:0]
0x394B	REG04B	0x02	RW	Bit[7:0]: r_y_dfd_rp_en_even_fall_opt_scg_0[7:0]
0x394C	REG04C	0x02	RW	Bit[7:0]: r_y_dfd_rp_en_even_fall_opt_scg_1[7:0]
0x394D	REG04D	0x02	RW	Bit[7:0]: r_y_dfd_rp_en_odd_rise_opt_scg_0[7:0]
0x394E	REG04E	0x02	RW	Bit[7:0]: r_y_dfd_rp_en_odd_rise_opt_scg_1[7:0]
0x394F	REG04F	0x02	RW	Bit[7:0]: r_y_dfd_rp_en_odd_fall_opt_scg_0[7:0]
0x3950	REG050	0x02	RW	Bit[7:0]: r_y_dfd_rp_en_odd_fall_opt_scg_1[7:0]
0x3951	REG051	0x02	RW	Bit[7:0]: r_y_bst_neg_even_rise_opt_scg_0[7:0]
0x3952	REG052	0x02	RW	Bit[7:0]: r_y_bst_neg_even_rise_opt_scg_1[7:0]
0x3953	REG053	0x02	RW	Bit[7:0]: r_y_bst_neg_even_fall_opt_scg_0[7:0]
0x3954	REG054	0x02	RW	Bit[7:0]: r_y_bst_neg_even_fall_opt_scg_1[7:0]
0x3955	REG055	0x02	RW	Bit[7:0]: r_y_bst_neg_odd_rise_opt_scg_0[7:0]
0x3956	REG056	0x02	RW	Bit[7:0]: r_y_bst_neg_odd_rise_opt_scg_1[7:0]
0x3957	REG057	0x02	RW	Bit[7:0]: r_y_bst_neg_odd_fall_opt_scg_0[7:0]
0x3958	REG058	0x02	RW	Bit[7:0]: r_y_bst_neg_odd_fall_opt_scg_1[7:0]
0x3959	REG059	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_even_rise_opt_scg_0[7:0]
0x395A	REG05A	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_even_rise_opt_scg_1[7:0]
0x395B	REG05B	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_even_rise_opt_scg_2[15:8]
0x395C	REG05C	0x04	RW	Bit[7:0]: r_y_fdc_rp_en_even_rise_opt_scg_2[7:0]
0x395D	REG05D	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_even_rise_opt_scg_3[15:8]

table 6-14 SENSOR_REG1 registers (sheet 12 of 24)

address	register name	default value	R/W	description
0x395E	REG05E	0x04	RW	Bit[7:0]: r_y_fdc_rp_en_even_rise_opt_scg_3[7:0]
0x395F	REG05F	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_even_fall_opt_scg_0[7:0]
0x3960	REG060	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_even_fall_opt_scg_1[7:0]
0x3961	REG061	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_even_fall_opt_scg_2[15:8]
0x3962	REG062	0x04	RW	Bit[7:0]: r_y_fdc_rp_en_even_fall_opt_scg_2[7:0]
0x3963	REG063	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_even_fall_opt_scg_3[15:8]
0x3964	REG064	0x04	RW	Bit[7:0]: r_y_fdc_rp_en_even_fall_opt_scg_3[7:0]
0x3965	REG065	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_odd_rise_opt_scg_0[7:0]
0x3966	REG066	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_odd_rise_opt_scg_1[7:0]
0x3967	REG067	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_odd_rise_opt_scg_2[15:8]
0x3968	REG068	0x04	RW	Bit[7:0]: r_y_fdc_rp_en_odd_rise_opt_scg_2[7:0]
0x3969	REG069	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_odd_rise_opt_scg_3[15:8]
0x396A	REG06A	0x04	RW	Bit[7:0]: r_y_fdc_rp_en_odd_rise_opt_scg_3[7:0]
0x396B	REG06B	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_odd_fall_opt_scg_0[7:0]
0x396C	REG06C	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_odd_fall_opt_scg_1[7:0]
0x396D	REG06D	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_odd_fall_opt_scg_2[15:8]
0x396E	REG06E	0x04	RW	Bit[7:0]: r_y_fdc_rp_en_odd_fall_opt_scg_2[7:0]
0x396F	REG06F	0x00	RW	Bit[7:0]: r_y_fdc_rp_en_odd_fall_opt_scg_3[15:8]
0x3970	REG070	0x04	RW	Bit[7:0]: r_y_fdc_rp_en_odd_fall_opt_scg_3[7:0]
0x3971	REG071	0x06	RW	Bit[7:0]: r_y_col_cbar_en_fall_ncg_0[7:0]
0x3972	REG072	0x04	RW	Bit[7:0]: r_y_pix_ecl_blk_en_lcg_rise_opt_scg_0[7:0]
0x3973	REG073	0x00	RW	Bit[7:0]: r_y_pix_ecl_blk_en_lcg_rise_opt_scg_1[7:0]
0x3974	REG074	0x00	RW	Bit[7:0]: r_y_pix_ecl_blk_en_lcg_fall_opt_scg_0[15:8]
0x3975	REG075	0x04	RW	Bit[7:0]: r_y_pix_ecl_blk_en_lcg_fall_opt_scg_0[7:0]
0x3976	REG076	0x00	RW	Bit[7:0]: r_y_pix_ecl_blk_en_lcg_fall_opt_scg_1[15:8]
0x3977	REG077	0x00	RW	Bit[7:0]: r_y_pix_ecl_blk_en_lcg_fall_opt_scg_1[7:0]
0x3978	REG078	0x04	RW	Bit[7:0]: r_y_pix_ecl_blk_en_hcg_rise_opt_scg_0[7:0]
0x3979	REG079	0x00	RW	Bit[7:0]: r_y_pix_ecl_blk_en_hcg_rise_opt_scg_1[7:0]
0x397A	REG07A	0x00	RW	Bit[7:0]: r_y_pix_ecl_blk_en_hcg_fall_opt_scg_0[15:8]
0x397B	REG07B	0x04	RW	Bit[7:0]: r_y_pix_ecl_blk_en_hcg_fall_opt_scg_0[7:0]

table 6-14 SENSOR_REG1 registers (sheet 13 of 24)

address	register name	default value	R/W	description
0x397C	REG07C	0x00	RW	Bit[7:0]: r_y_pix_ecl_blk_en_hcg_fall_opt_scg_1[15:8]
0x397D	REG07D	0x00	RW	Bit[7:0]: r_y_pix_ecl_blk_en_hcg_fall_opt_scg_1[7:0]
0x397E	REG07E	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_lcg_rise_opt_scg_0[15:8]
0x397F	REG07F	0x04	RW	Bit[7:0]: r_y_pix_ecl_sig_en_lcg_rise_opt_scg_0[7:0]
0x3980	REG080	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_lcg_rise_opt_scg_1[15:8]
0x3981	REG081	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_lcg_rise_opt_scg_1[7:0]
0x3982	REG082	0x04	RW	Bit[7:0]: r_y_pix_ecl_sig_en_lcg_fall_opt_scg_0[7:0]
0x3983	REG083	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_lcg_fall_opt_scg_1[7:0]
0x3984	REG084	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_hcg_rise_opt_scg_0[15:8]
0x3985	REG085	0x04	RW	Bit[7:0]: r_y_pix_ecl_sig_en_hcg_rise_opt_scg_0[7:0]
0x3986	REG086	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_hcg_rise_opt_scg_1[15:8]
0x3987	REG087	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_hcg_rise_opt_scg_1[7:0]
0x3988	REG088	0x04	RW	Bit[7:0]: r_y_pix_ecl_sig_en_hcg_fall_opt_scg_0[7:0]
0x3989	REG089	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_hcg_fall_opt_scg_1[7:0]
0x398A	REG08A	0x04	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_lcg_rise_scg_0[7:0]
0x398B	REG08B	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_lcg_rise_scg_1[7:0]
0x398C	REG08C	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_lcg_fall_scg_0[15:8]
0x398D	REG08D	0x04	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_lcg_fall_scg_0[7:0]
0x398E	REG08E	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_lcg_fall_scg_1[15:8]
0x398F	REG08F	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_lcg_fall_scg_1[7:0]
0x3990	REG090	0x04	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_hcg_rise_scg_0[7:0]
0x3991	REG091	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_hcg_rise_scg_1[7:0]
0x3992	REG092	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_hcg_fall_scg_0[15:8]

table 6-14 SENSOR_REG1 registers (sheet 14 of 24)

address	register name	default value	R/W	description
0x3993	REG093	0x04	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_hcg_fall_scg_0[7:0]
0x3994	REG094	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_hcg_fall_scg_1[15:8]
0x3995	REG095	0x00	RW	Bit[7:0]: r_y_pix_ecl_sig_en_top_btm_hcg_fall_scg_1[7:0]
0x3996	REG096	0x04	RW	Bit[7:0]: r_y_pix_ecl_idle_en_top_btm_fall_opt_ncg_0[7:0]
0x3997	REG097	0x04	RW	Bit[7:0]: r_y_pix_ecl_idle_en_top_btm_rise_ncg_0[7:0]
0x3998	REG098	0x02	RW	Bit[7:0]: r_y_pix_ecl_idle_en_top_btm_rise_ncg_1[7:0]
0x3999	REG099	0x00	RW	Bit[7:0]: r_y_pix_ecl_idle_en_top_btm_fall_ncg_0[15:8]
0x399A	REG09A	0x04	RW	Bit[7:0]: r_y_pix_ecl_idle_en_top_btm_fall_ncg_0[7:0]
0x399B	REG09B	0x04	RW	Bit[7:0]: r_y_pix_ecl_idle_en_fall_opt_ncg_0[7:0]
0x399C	REG09C	0x04	RW	Bit[7:0]: r_y_pix_ecl_idle_en_rise_ncg_0[7:0]
0x399D	REG09D	0x02	RW	Bit[7:0]: r_y_pix_ecl_idle_en_rise_ncg_1[7:0]
0x399E	REG09E	0x00	RW	Bit[7:0]: r_y_pix_ecl_idle_en_fall_ncg_0[15:8]
0x399F	REG09F	0x04	RW	Bit[7:0]: r_y_pix_ecl_idle_en_fall_ncg_0[7:0]
0x39A0	REG0A0	0x02	RW	Bit[7:0]: r_y_col_blsw_rise_opt_ncg_0[7:0]
0x39A1	REG0A1	0x00	RW	Bit[7:0]: r_y_col_blsw_rise_opt_ncg_1[15:8]
0x39A2	REG0A2	0x18	RW	Bit[7:0]: r_y_col_blsw_rise_opt_ncg_1[7:0]
0x39A3	REG0A3	0x00	RW	Bit[7:0]: r_y_col_blsw_fall_opt_ncg_0[15:8]
0x39A4	REG0A4	0x02	RW	Bit[7:0]: r_y_col_blsw_fall_opt_ncg_0[7:0]
0x39A5	REG0A5	0x00	RW	Bit[7:0]: r_y_col_blsw_fall_opt_ncg_1[15:8]
0x39A6	REG0A6	0x01	RW	Bit[7:0]: r_y_col_blsw_fall_opt_ncg_1[7:0]
0x39A7	REG0A7	0x01	RW	Bit[7:0]: r_y_sh_vrhv1_fall_opt_ncg_0[7:0]
0x39A8	REG0A8	0x01	RW	Bit[7:0]: r_y_sh_vrhv1_rise_ncg_0[7:0]
0x39A9	REG0A9	0x01	RW	Bit[7:0]: r_y_sh_vrhv2_fall_opt_ncg_0[7:0]
0x39AA	REG0AA	0x01	RW	Bit[7:0]: r_y_sh_vrhv2_rise_ncg_0[7:0]
0x39AB	REG0AB	0x01	RW	Bit[7:0]: r_y_col_dcomp_vcn_sh_fall_opt_ncg_0[7:0]
0x39AC	REG0AC	0x00	RW	Bit[7:0]: r_y_col_dcomp_vcn_sh_rise_ncg_0[7:0]
0x39AD	REG0AD	0x01	RW	Bit[7:0]: r_y_col_dcomp_vcn_sh_rise_ncg_1[7:0]

table 6-14 SENSOR_REG1 registers (sheet 15 of 24)

address	register name	default value	R/W	description
0x39AE	REG0AE	0x00	RW	Bit[7:0]: r_y_col_dcomp_vcn_sh_fall_ncg_0[7:0]
0x39AF	REG0AF	0x01	RW	Bit[7:0]: r_y_col_dcomp_vbn_sh_fall_opt_ncg_0[7:0]
0x39B0	REG0B0	0x00	RW	Bit[7:0]: r_y_col_dcomp_vbn_sh_rise_ncg_0[7:0]
0x39B1	REG0B1	0x01	RW	Bit[7:0]: r_y_col_dcomp_vbn_sh_rise_ncg_1[7:0]
0x39B2	REG0B2	0x00	RW	Bit[7:0]: r_y_col_dcomp_vbn_sh_fall_ncg_0[7:0]
0x39B3	REG0B3	0x01	RW	Bit[7:0]: r_y_col_rampbuf_vcn_sh_fall_opt_ncg_0[7:0]
0x39B4	REG0B4	0x00	RW	Bit[7:0]: r_y_col_rampbuf_vcn_sh_rise_ncg_0[7:0]
0x39B5	REG0B5	0x01	RW	Bit[7:0]: r_y_col_rampbuf_vcn_sh_rise_ncg_1[7:0]
0x39B6	REG0B6	0x00	RW	Bit[7:0]: r_y_col_rampbuf_vcn_sh_fall_ncg_0[7:0]
0x39B7	REG0B7	0x01	RW	Bit[7:0]: r_y_col_rampbuf_vbn_sh_fall_opt_ncg_0[7:0]
0x39B8	REG0B8	0x00	RW	Bit[7:0]: r_y_col_rampbuf_vbn_sh_rise_ncg_0[7:0]
0x39B9	REG0B9	0x01	RW	Bit[7:0]: r_y_col_rampbuf_vbn_sh_rise_ncg_1[7:0]
0x39BA	REG0BA	0x00	RW	Bit[7:0]: r_y_col_rampbuf_vbn_sh_fall_ncg_0[7:0]
0x39BB	REG0BB	0x01	RW	Bit[7:0]: r_y_col_vln_vcn_sh_fall_opt_ncg_0[7:0]
0x39BC	REG0BC	0x00	RW	Bit[7:0]: r_y_col_vln_vcn_sh_rise_ncg_0[7:0]
0x39BD	REG0BD	0x01	RW	Bit[7:0]: r_y_col_vln_vcn_sh_rise_ncg_1[7:0]
0x39BE	REG0BE	0x00	RW	Bit[7:0]: r_y_col_vln_vcn_sh_fall_ncg_0[7:0]
0x39BF	REG0BF	0x01	RW	Bit[7:0]: r_y_col_vln_vbn_sh_fall_opt_ncg_0[7:0]
0x39C0	REG0C0	0x00	RW	Bit[7:0]: r_y_col_vln_vbn_sh_rise_ncg_0[7:0]
0x39C1	REG0C1	0x01	RW	Bit[7:0]: r_y_col_vln_vbn_sh_rise_ncg_1[7:0]
0x39C2	REG0C2	0x00	RW	Bit[7:0]: r_y_col_vln_vbn_sh_fall_ncg_0[7:0]
0x39C3	REG0C3	0x01	RW	Bit[7:0]: r_y_col_rampbuf_en_rise_opt_ncg_0[7:0]
0x39C4	REG0C4	0x01	RW	Bit[7:0]: r_y_col_rampbuf_en_fall_ncg_0[7:0]
0x39C5	REG0C5	0x01	RW	Bit[7:0]: r_y_col_dcomp_en_rise_opt_ncg_0[7:0]
0x39C6	REG0C6	0x01	RW	Bit[7:0]: r_y_col_dcomp_en_fall_ncg_0[7:0]
0x39C7	REG0C7	0x01	RW	Bit[7:0]: r_y_col_vln_en_rise_opt_ncg_0[7:0]
0x39C8	REG0C8	0x00	RW	Bit[7:0]: r_y_col_vln_en_rise_ncg_0[15:8]
0x39C9	REG0C9	0x02	RW	Bit[7:0]: r_y_col_vln_en_rise_ncg_0[7:0]
0x39CA	REG0CA	0x01	RW	Bit[7:0]: r_y_col_vln_en_fall_ncg_0[7:0]
0x39CB	REG0CB	0x01	RW	Bit[7:0]: r_y_col_vln_en_fall_ncg_1[7:0]

table 6-14 SENSOR_REG1 registers (sheet 16 of 24)

address	register name	default value	R/W	description
0x39CC	REG0CC	0x02	RW	Bit[7:0]: r_y_col_dcomp1_rst1_rise_opt_ncg_0[7:0]
0x39CD	REG0CD	0x08	RW	Bit[7:0]: r_y_col_dcomp1_rst1_fall_x1_ncg_0[7:0]
0x39CE	REG0CE	0x08	RW	Bit[7:0]: r_y_col_dcomp1_rst1_fall_x2_ncg_0[7:0]
0x39CF	REG0CF	0x08	RW	Bit[7:0]: r_y_col_dcomp1_rst1_fall_x4_ncg_0[7:0]
0x39D0	REG0D0	0x08	RW	Bit[7:0]: r_y_col_dcomp1_rst1_fall_x8_ncg_0[7:0]
0x39D1	REG0D1	0x02	RW	Bit[7:0]: r_y_col_dcomp1_rst2_rise_opt_ncg_0[7:0]
0x39D2	REG0D2	0x08	RW	Bit[7:0]: r_y_col_dcomp1_rst2_fall_x1_ncg_0[7:0]
0x39D3	REG0D3	0x08	RW	Bit[7:0]: r_y_col_dcomp1_rst2_fall_x2_ncg_0[7:0]
0x39D4	REG0D4	0x08	RW	Bit[7:0]: r_y_col_dcomp1_rst2_fall_x4_ncg_0[7:0]
0x39D5	REG0D5	0x08	RW	Bit[7:0]: r_y_col_dcomp1_rst2_fall_x8_ncg_0[7:0]
0x39D6	REG0D6	0x02	RW	Bit[7:0]: r_y_col_dcomp2_rst_rise_opt_ncg_0[7:0]
0x39D7	REG0D7	0x08	RW	Bit[7:0]: r_y_col_dcomp2_rst_fall_opt_ncg_0[7:0]
0x39D8	REG0D8	0x01	RW	Bit[7:0]: r_y_col_dcomp3_en_rise_ncg_0[7:0]
0x39D9	REG0D9	0x01	RW	Bit[7:0]: r_y_col_dcomp3_en_fall_ncg_0[7:0]
0x39DA	REG0DA	0x00	RW	Bit[7:0]: r_y_col_dcomp_fast_up_rise_opt_ncg_0[15:8]
0x39DB	REG0DB	0x04	RW	Bit[7:0]: r_y_col_dcomp_fast_up_rise_opt_ncg_0[7:0]
0x39DC	REG0DC	0x01	RW	Bit[7:0]: r_y_col_dcomp_fast_up_rise_ncg_0[7:0]
0x39DD	REG0DD	0x08	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x1_ncg_0[7:0]
0x39DE	REG0DE	0x08	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x2_ncg_0[7:0]
0x39DF	REG0DF	0x08	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x4_ncg_0[7:0]
0x39E0	REG0E0	0x08	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x8_ncg_0[7:0]
0x39E1	REG0E1	0x00	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x1_ncg_1[15:8]
0x39E2	REG0E2	0x08	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x1_ncg_1[7:0]
0x39E3	REG0E3	0x00	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x2_ncg_1[15:8]
0x39E4	REG0E4	0x08	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x2_ncg_1[7:0]
0x39E5	REG0E5	0x00	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x4_ncg_1[15:8]
0x39E6	REG0E6	0x08	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x4_ncg_1[7:0]
0x39E7	REG0E7	0x00	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x8_ncg_1[15:8]
0x39E8	REG0E8	0x08	RW	Bit[7:0]: r_y_col_dcomp_fast_up_fall_x8_ncg_1[7:0]

table 6-14 SENSOR_REG1 registers (sheet 17 of 24)

address	register name	default value	R/W	description
0x39E9	REG0E9	0x04	RW	Bit[7:0]: r_y_col_dcomp_bypass_casc_p_rise_ncg_0[7:0]
0x39EA	REG0EA	0x01	RW	Bit[7:0]: r_y_col_dcomp_bypass_casc_p_fall_ncg_0[7:0]
0x39EB	REG0EB	0x04	RW	Bit[7:0]: r_y_col_dcomp_bypass_casc_n_rise_ncg_0[7:0]
0x39EC	REG0EC	0x01	RW	Bit[7:0]: r_y_col_dcomp_bypass_casc_n_fall_ncg_0[7:0]
0x39ED	REG0ED	0x04	RW	Bit[7:0]: r_y_col_slpctrl_en_rise_ncg_0[7:0]
0x39EE	REG0EE	0x02	RW	Bit[7:0]: r_y_col_slpctrl_en_fall_ncg_0[7:0]
0x39EF	REG0EF	0x01	RW	Bit[7:0]: r_y_col_fb_samp_en_rise_opt_ncg_0[7:0]
0x39F0	REG0F0	0x01	RW	Bit[7:0]: r_y_col_fb_samp_en_fall_ncg_0[7:0]
0x39F1	REG0F1	0x04	RW	Bit[7:0]: r_y_col_fb_dcomp1_1_en_rise_opt_ncg_0[7:0]
0x39F2	REG0F2	0x04	RW	Bit[7:0]: r_y_col_fb_dcomp1_1_en_fall_opt_ncg_0[7:0]
0x39F3	REG0F3	0x04	RW	Bit[7:0]: r_y_col_fb_dcomp1_2_en_rise_opt_ncg_0[7:0]
0x39F4	REG0F4	0x04	RW	Bit[7:0]: r_y_col_fb_dcomp1_2_en_fall_opt_ncg_0[7:0]
0x39F5	REG0F5	0x01	RW	Bit[7:0]: r_y_col_count_lat_wen_bsun_rise_ncg_0[7:0]
0x39F6	REG0F6	0x04	RW	Bit[7:0]: r_y_col_count_lat_wen_bsun_fall_x1_ncg_0[7:0]
0x39F7	REG0F7	0x04	RW	Bit[7:0]: r_y_col_count_lat_wen_bsun_fall_x2_ncg_0[7:0]
0x39F8	REG0F8	0x04	RW	Bit[7:0]: r_y_col_count_lat_wen_bsun_fall_x4_ncg_0[7:0]
0x39F9	REG0F9	0x04	RW	Bit[7:0]: r_y_col_count_lat_wen_bsun_fall_x8_ncg_0[7:0]
0x39FA	REG0FA	0x0A	RW	Bit[7:0]: r_y_col_count_sram_div_rst_rise_ncg_0[7:0]
0x39FB	REG0FB	0x0F	RW	Bit[7:0]: r_y_col_count_sram_div_rst_fall_ncg_0[7:0]
0x39FC	REG0FC	0x14	RW	Bit[7:0]: r_y_col_count_gcgen_rst_rise_ncg_0[7:0]
0x39FD	REG0FD	0x00	RW	Bit[7:0]: r_y_col_count_gcgen_rst_rise_ncg_1[7:0]
0x39FE	REG0FE	0x00	RW	Bit[7:0]: r_y_col_count_gcgen_rst_rise_ncg_2[15:8]
0x39FF	REG0FF	0x02	RW	Bit[7:0]: r_y_col_count_gcgen_rst_rise_ncg_2[7:0]
0x3A00	REG100	0x19	RW	Bit[7:0]: r_y_col_count_gcgen_rst_fall_ncg_0[7:0]

table 6-14 SENSOR_REG1 registers (sheet 18 of 24)

address	register name	default value	R/W	description
0x3A01	REG101	0x00	RW	Bit[7:0]: r_y_col_count_gcgen_rst_fall_ncg_1[7:0]
0x3A02	REG102	0x00	RW	Bit[7:0]: r_y_col_count_gcgen_rst_fall_ncg_2[15:8]
0x3A03	REG103	0x07	RW	Bit[7:0]: r_y_col_count_gcgen_rst_fall_ncg_2[7:0]
0x3A04	REG104	0x00	RW	Bit[7:0]: r_y_col_count_lat_wen_blk_rise_opt_ncg_0[15:8]
0x3A05	REG105	0x02	RW	Bit[7:0]: r_y_col_count_lat_wen_blk_rise_opt_ncg_0[7:0]
0x3A06	REG106	0x00	RW	Bit[7:0]: r_y_col_count_lat_wen_blk_fall_opt_ncg_0[15:8]
0x3A07	REG107	0x07	RW	Bit[7:0]: r_y_col_count_lat_wen_blk_fall_opt_ncg_0[7:0]
0x3A08	REG108	0x05	RW	Bit[7:0]: r_y_col_count_lat_wen_sig_rise_opt_ncg_0[7:0]
0x3A09	REG109	0x0A	RW	Bit[7:0]: r_y_col_count_lat_wen_sig_fall_opt_ncg_0[7:0]
0x3A0A	REG10A	0x05	RW	Bit[7:0]: r_y_col_count_lat_wen_mem_rise_opt_ncg_0[7:0]
0x3A0B	REG10B	0x0A	RW	Bit[7:0]: r_y_col_count_lat_wen_mem_fall_opt_ncg_0[7:0]
0x3A0C	REG10C	0x01	RW	Bit[7:0]: r_y_ramp_integ_samp_rise_opt_ncg_0[7:0]
0x3A0D	REG10D	0x08	RW	Bit[7:0]: r_y_ramp_integ_samp_fall_opt_ncg_0[7:0]
0x3A0E	REG10E	0x01	RW	Bit[7:0]: r_y_ramp_vofs_samp_rise_opt_ncg_0[7:0]
0x3A0F	REG10F	0x08	RW	Bit[7:0]: r_y_ramp_vofs_samp_fall_opt_ncg_0[7:0]
0x3A10	REG110	0x01	RW	Bit[7:0]: r_y_ramp_vref_samp_rise_opt_ncg_0[7:0]
0x3A11	REG111	0x08	RW	Bit[7:0]: r_y_ramp_vref_samp_fall_opt_ncg_0[7:0]
0x3A12	REG112	0x01	RW	Bit[7:0]: r_y_psrr_dc_samp_rise_opt_ncg_0[7:0]
0x3A13	REG113	0x08	RW	Bit[7:0]: r_y_psrr_dc_samp_fall_opt_ncg_0[7:0]
0x3A14	REG114	0x01	RW	Bit[7:0]: r_y_psrr_act_rst_rise_opt_ncg_0[7:0]
0x3A15	REG115	0x0A	RW	Bit[7:0]: r_y_psrr_act_rst_fall_opt_ncg_0[7:0]
0x3A16	REG116	0x01	RW	Bit[7:0]: r_y_ramp_voffset_en_fall_opt_ncg_0[7:0]
0x3A17	REG117	0x01	RW	Bit[7:0]: r_y_ramp_voffset_en_rise_ncg_0[7:0]
0x3A18	REG118	0x01	RW	Bit[7:0]: r_y_ramp_buf_en_rise_opt_ncg_0[7:0]
0x3A19	REG119	0x01	RW	Bit[7:0]: r_y_ramp_buf_en_fall_ncg_0[7:0]

table 6-14 SENSOR_REG1 registers (sheet 19 of 24)

address	register name	default value	R/W	description
0x3A1A	REG11A	0x01	RW	Bit[7:0]: r_y_ramp_cur_ass_samp_rise_opt_ncg_0[7:0]
0x3A1B	REG11B	0x08	RW	Bit[7:0]: r_y_ramp_cur_ass_samp_fall_opt_ncg_0[7:0]
0x3A1C	REG11C	0x01	RW	Bit[7:0]: r_y_ramp_current_bias_samp_rise_opt_ncg_0[7:0]
0x3A1D	REG11D	0x08	RW	Bit[7:0]: r_y_ramp_current_bias_samp_fall_opt_ncg_0[7:0]
0x3A1E	REG11E	0x01	RW	Bit[7:0]: r_y_ramp_vofs_reset_rise_opt_ncg_0[7:0]
0x3A1F	REG11F	0x08	RW	Bit[7:0]: r_y_ramp_vofs_reset_fall_opt_ncg_0[7:0]
0x3A20	REG120	0x00	RW	Bit[7:0]: r_y_ramp_assist_en_fall_opt_ncg_0[15:8]
0x3A21	REG121	0x00	RW	Bit[7:0]: r_y_ramp_assist_en_fall_opt_ncg_0[7:0]
0x3A22	REG122	0x00	RW	Bit[7:0]: r_y_ramp_assist_en_rise_ncg_0[7:0]
0x3A23	REG123	0x00	RW	Bit[7:0]: r_y_ramp_assist_en_rise_ncg_2[7:0]
0x3A24	REG124	0x00	RW	Bit[7:0]: r_y_ramp_assist_en_fall_ncg_0[7:0]
0x3A25	REG125	0x04	RW	Bit[7:0]: r_y_ramp_assist_en_fall_ncg_1[7:0]
0x3A26	REG126	0x04	RW	Bit[7:0]: r_y_ramp_assist_en_fall_ncg_2[7:0]
0x3A27	REG127	0x01	RW	Bit[7:0]: r_y_ramp_assist_ctrl_en_fall_opt_ncg_0[7:0]
0x3A28	REG128	0x01	RW	Bit[7:0]: r_y_ramp_assist_ctrl_en_rise_ncg_0[7:0]
0x3A29	REG129	0x00	RW	Bit[7:4]: r_y_ramp_vofs_aux_scg_hcg_x8[3:0] Bit[3:0]: r_y_ramp_vofs_aux_scg_hcg_x4[3:0]
0x3A2A	REG12A	0x00	RW	Bit[7:4]: r_y_ramp_vofs_aux_scg_hcg_x2[3:0] Bit[3:0]: r_y_ramp_vofs_aux_scg_hcg_x1[3:0]
0x3A2B	REG12B	0x00	RW	Bit[7:4]: r_y_ramp_vofs_aux_scg_lcg_x8[3:0] Bit[3:0]: r_y_ramp_vofs_aux_scg_lcg_x4[3:0]
0x3A2C	REG12C	0x00	RW	Bit[7:4]: r_y_ramp_vofs_aux_scg_lcg_x2[3:0] Bit[3:0]: r_y_ramp_vofs_aux_scg_lcg_x1[3:0]
0x3A2D	REG12D	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_vofs_aux_sw_scg_hcg_x8[5:0]
0x3A2E	REG12E	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_vofs_aux_sw_scg_hcg_x4[5:0]
0x3A2F	REG12F	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_vofs_aux_sw_scg_hcg_x2[5:0]
0x3A30	REG130	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_vofs_aux_sw_scg_hcg_x1[5:0]

table 6-14 SENSOR_REG1 registers (sheet 20 of 24)

address	register name	default value	R/W	description
0x3A31	REG131	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_vofs_aux_sw_scg_lcg_x8[5:0]
0x3A32	REG132	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_vofs_aux_sw_scg_lcg_x4[5:0]
0x3A33	REG133	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_vofs_aux_sw_scg_lcg_x2[5:0]
0x3A34	REG134	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_vofs_aux_sw_scg_lcg_x1[5:0]
0x3A35	REG135	0x00	RW	Bit[7:6]: r_y_psrr_gain_ctrl_scg_hcg_x8[1:0] Bit[5:4]: r_y_psrr_gain_ctrl_scg_hcg_x4[1:0] Bit[3:2]: r_y_psrr_gain_ctrl_scg_hcg_x2[1:0] Bit[1:0]: r_y_psrr_gain_ctrl_scg_hcg_x1[1:0]
0x3A36	REG136	0x00	RW	Bit[7:6]: r_y_psrr_gain_ctrl_scg_lcg_x8[1:0] Bit[5:4]: r_y_psrr_gain_ctrl_scg_lcg_x4[1:0] Bit[3:2]: r_y_psrr_gain_ctrl_scg_lcg_x2[1:0] Bit[1:0]: r_y_psrr_gain_ctrl_scg_lcg_x1[1:0]
0x3A37	REG137	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_psrr_res_sw_scg_hcg_x8[5:0]
0x3A38	REG138	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_psrr_res_sw_scg_hcg_x4[5:0]
0x3A39	REG139	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_psrr_res_sw_scg_hcg_x2[5:0]
0x3A3A	REG13A	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_psrr_res_sw_scg_hcg_x1[5:0]
0x3A3B	REG13B	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_psrr_res_sw_scg_lcg_x8[5:0]
0x3A3C	REG13C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_psrr_res_sw_scg_lcg_x4[5:0]
0x3A3D	REG13D	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_psrr_res_sw_scg_lcg_x2[5:0]
0x3A3E	REG13E	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_psrr_res_sw_scg_lcg_x1[5:0]
0x3A3F	REG13F	0x00	RW	Bit[7]: Not used Bit[6:4]: r_y_psrr_passive_bw_scg_hcg_x8[2:0] Bit[3]: Not used Bit[2:0]: r_y_psrr_passive_bw_scg_hcg_x4[2:0]
0x3A40	REG140	0x00	RW	Bit[7]: Not used Bit[6:4]: r_y_psrr_passive_bw_scg_hcg_x2[2:0] Bit[3]: Not used Bit[2:0]: r_y_psrr_passive_bw_scg_hcg_x1[2:0]

table 6-14 SENSOR_REG1 registers (sheet 21 of 24)

address	register name	default value	R/W	description
0x3A41	REG141	0x00	RW	Bit[7]: Not used Bit[6:4]: r_y_psrr_passive_bw_scg_lcg_x8[2:0] Bit[3]: Not used Bit[2:0]: r_y_psrr_passive_bw_scg_lcg_x4[2:0]
0x3A42	REG142	0x00	RW	Bit[7]: Not used Bit[6:4]: r_y_psrr_passive_bw_scg_lcg_x2[2:0] Bit[3]: Not used Bit[2:0]: r_y_psrr_passive_bw_scg_lcg_x1[2:0]
0x3A43	REG143	0x00	RW	Bit[7]: Not used Bit[6:0]: r_y_psrr_sw_gain_scg_hcg_x8[6:0]
0x3A44	REG144	0x00	RW	Bit[7]: Not used Bit[6:0]: r_y_psrr_sw_gain_scg_hcg_x4[6:0]
0x3A45	REG145	0x00	RW	Bit[7]: Not used Bit[6:0]: r_y_psrr_sw_gain_scg_hcg_x2[6:0]
0x3A46	REG146	0x00	RW	Bit[7]: Not used Bit[6:0]: r_y_psrr_sw_gain_scg_hcg_x1[6:0]
0x3A47	REG147	0x00	RW	Bit[7]: Not used Bit[6:0]: r_y_psrr_sw_gain_scg_lcg_x8[6:0]
0x3A48	REG148	0x00	RW	Bit[7]: Not used Bit[6:0]: r_y_psrr_sw_gain_scg_lcg_x4[6:0]
0x3A49	REG149	0x00	RW	Bit[7]: Not used Bit[6:0]: r_y_psrr_sw_gain_scg_lcg_x2[6:0]
0x3A4A	REG14A	0x00	RW	Bit[7]: Not used Bit[6:0]: r_y_psrr_sw_gain_scg_lcg_x1[6:0]
0x3A4B	REG14B	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_vofs_scg_hcg_x8[4:0]
0x3A4C	REG14C	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_vofs_scg_hcg_x4[4:0]
0x3A4D	REG14D	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_vofs_scg_hcg_x2[4:0]
0x3A4E	REG14E	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_vofs_scg_hcg_x1[4:0]
0x3A4F	REG14F	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_vofs_scg_lcg_x8[4:0]
0x3A50	REG150	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_vofs_scg_lcg_x4[4:0]
0x3A51	REG151	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_vofs_scg_lcg_x2[4:0]

table 6-14 SENSOR_REG1 registers (sheet 22 of 24)

address	register name	default value	R/W	description
0x3A52	REG152	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_vofs_scg_lcg_x1[4:0]
0x3A53	REG153	0x00	RW	Bit[7:4]: r_y_ramp_vref_scg_hcg_x8[3:0] Bit[3:0]: r_y_ramp_vref_scg_hcg_x4[3:0]
0x3A54	REG154	0x00	RW	Bit[7:4]: r_y_ramp_vref_scg_hcg_x2[3:0] Bit[3:0]: r_y_ramp_vref_scg_hcg_x1[3:0]
0x3A55	REG155	0x00	RW	Bit[7:4]: r_y_ramp_vref_scg_lcg_x8[3:0] Bit[3:0]: r_y_ramp_vref_scg_lcg_x4[3:0]
0x3A56	REG156	0x00	RW	Bit[7:4]: r_y_ramp_vref_scg_lcg_x2[3:0] Bit[3:0]: r_y_ramp_vref_scg_lcg_x1[3:0]
0x3A57	REG157	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_rampbuf_aux_scg_hcg_x8[4:0]
0x3A58	REG158	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_rampbuf_aux_scg_hcg_x4[4:0]
0x3A59	REG159	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_rampbuf_aux_scg_hcg_x2[4:0]
0x3A5A	REG15A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_rampbuf_aux_scg_hcg_x1[4:0]
0x3A5B	REG15B	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_rampbuf_aux_scg_lcg_x8[4:0]
0x3A5C	REG15C	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_rampbuf_aux_scg_lcg_x4[4:0]
0x3A5D	REG15D	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_rampbuf_aux_scg_lcg_x2[4:0]
0x3A5E	REG15E	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_rampbuf_aux_scg_lcg_x1[4:0]
0x3A5F	REG15F	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_cur_ass_code_scg_hcg_x8[5:0]
0x3A60	REG160	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_cur_ass_code_scg_hcg_x4[5:0]
0x3A61	REG161	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_cur_ass_code_scg_hcg_x2[5:0]
0x3A62	REG162	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_cur_ass_code_scg_hcg_x1[5:0]
0x3A63	REG163	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_cur_ass_code_scg_lcg_x8[5:0]
0x3A64	REG164	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_cur_ass_code_scg_lcg_x4[5:0]

table 6-14 SENSOR_REG1 registers (sheet 23 of 24)

address	register name	default value	R/W	description
0x3A65	REG165	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_cur_ass_code_scg_lcg_x2[5:0]
0x3A66	REG166	0x00	RW	Bit[7:6]: Not used Bit[5:0]: r_y_ramp_cur_ass_code_scg_lcg_x1[5:0]
0x3A67	REG167	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_calibr_code_scg_hcg_x8[4:0]
0x3A68	REG168	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_calibr_code_scg_hcg_x4[4:0]
0x3A69	REG169	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_calibr_code_scg_hcg_x2[4:0]
0x3A6A	REG16A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_calibr_code_scg_hcg_x1[4:0]
0x3A6B	REG16B	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_calibr_code_scg_lcg_x8[4:0]
0x3A6C	REG16C	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_calibr_code_scg_lcg_x4[4:0]
0x3A6D	REG16D	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_calibr_code_scg_lcg_x2[4:0]
0x3A6E	REG16E	0x00	RW	Bit[7:5]: Not used Bit[4:0]: r_y_ramp_calibr_code_scg_lcg_x1[4:0]
0x3A6F	REG16F	0x00	RW	Bit[7]: r_y_ramp_cur_assist_en_scg_hcg_x8 Bit[6]: r_y_ramp_cur_assist_en_scg_hcg_x4 Bit[5]: r_y_ramp_cur_assist_en_scg_hcg_x2 Bit[4]: r_y_ramp_cur_assist_en_scg_hcg_x1 Bit[3]: r_y_ramp_cur_assist_en_scg_lcg_x8 Bit[2]: r_y_ramp_cur_assist_en_scg_lcg_x4 Bit[1]: r_y_ramp_cur_assist_en_scg_lcg_x2 Bit[0]: r_y_ramp_cur_assist_en_scg_lcg_x1
0x3A70	REG170	0x00	RW	Bit[7]: r_y_col_count_codesave_en_x8 Bit[6]: r_y_col_count_codesave_en_x4 Bit[5]: r_y_col_count_codesave_en_x2 Bit[4]: r_y_col_count_codesave_en_x1 Bit[3:0]: Not used
0x3A71	REG171	0x00	RW	Bit[7:4]: r_y_col_count_en_div_x8[3:0] Bit[3:0]: r_y_col_count_en_div_x4[3:0]
0x3A72	REG172	0x00	RW	Bit[7:4]: r_y_col_count_en_div_x2[3:0] Bit[3:0]: r_y_col_count_en_div_x1[3:0]
0x3A73	REG173	0x20	RW	Bit[7:5]: Not used Bit[4:0]: r_y_blksun_sig_lcg_x8[4:0]

table 6-14 SENSOR_REG1 registers (sheet 24 of 24)

address	register name	default value	R/W	description
0x3A74	REG174	0x20	RW	Bit[7:5]: Not used Bit[4:0]: r_y_blksun_sig_lcg_x4[4:0]
0x3A75	REG175	0x20	RW	Bit[7:5]: Not used Bit[4:0]: r_y_blksun_sig_lcg_x2[4:0]
0x3A76	REG176	0x20	RW	Bit[7:5]: Not used Bit[4:0]: r_y_blksun_sig_lcg_x1[4:0]
0x3A77	REG177	0x20	RW	Bit[7:5]: Not used Bit[4:0]: r_y_blksun_sig_hcg_x8[4:0]
0x3A78	REG178	0x20	RW	Bit[7:5]: Not used Bit[4:0]: r_y_blksun_sig_hcg_x4[4:0]
0x3A79	REG179	0x20	RW	Bit[7:5]: Not used Bit[4:0]: r_y_blksun_sig_hcg_x2[4:0]
0x3A7A	REG17A	0x20	RW	Bit[7:5]: Not used Bit[4:0]: r_y_blksun_sig_hcg_x1[4:0]
0x3A7B	REG17B	0x00	RW	Bit[7]: r_y_col_vln_l_sel_x8 Bit[6]: r_y_col_vln_l_sel_x4 Bit[5]: r_y_col_vln_l_sel_x2 Bit[4]: r_y_col_vln_l_sel_x1 Bit[3:0]: Not used
0x3A7C	REG17C	0x00	RW	Bit[7]: r_y_col_dcomp_selcap_x8 Bit[6]: r_y_col_dcomp_selcap_x4 Bit[5]: r_y_col_dcomp_selcap_x2 Bit[4]: r_y_col_dcomp_selcap_x1 Bit[3:0]: Not used
0x3A7D	REG17D	0x00	RW	Bit[7]: r_y_col_rampbuf_compens_byp_x8 Bit[6]: r_y_col_rampbuf_compens_byp_x4 Bit[5]: r_y_col_rampbuf_compens_byp_x2 Bit[4]: r_y_col_rampbuf_compens_byp_x1 Bit[3:0]: Not used

6.15 STROBE [0x3C80 - 0x3C85]

table 6-15 STROBE registers

address	register name	default value	R/W	description
0x3C80	RSTRB	0x00	RW	Bit[7]: Strobe on/off Bit[6]: Strobe polarity 0: Active high 1 Active low Bit[5:4]: width_in_xenon Bit[3]: Reserved Bit[2:0]: Mode 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3C81	RSVD	–	–	Reserved
0x3C82	STROBE ADD DUMMY	0x00	RW	Bit[7:0]: Dummy line number added at strobe[15:8]
0x3C83	STROBE ADD DUMMY	0x00	RW	Bit[7:0]: Dummy line number added at strobe[7:0]
0x3C84	STROBE CTL1	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: start_point_sel 00: SOF 01: end_of_sample 10: end_of_precharge 11: Not used Bit[3]: strobe_md4_repeat Bit[2]: strobe_repeat_enable Bit[1:0]: strobe_lantency 00: Strobe generated at next frame 01: Delay one frame, strobe generated 2 frames later 10: Delay one frame, strobe generated 3 frames later 11: Delay one frame, strobe generated 4 frames later
0x3C85	STROBE WIDTH	0x00	RW	Bit[7:2]: strobe_pulse_width_step Bit[1:0]: strobe_pulse_width_gain strobe_pulse width = 128 * (2**gain) * (step+1) * sclk_period

6.16 OTP_SC [0x3D80 - 0x3DAF]

table 6-16 OTP_SC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3D80	R PGM CTR	–	R	Bit[7]: otp_pgenb_n Bit[6:0]: Not used
0x3D81	R LOAD CTR	–	R	Bit[7]: otp_load Bit[6]: Not used Bit[5]: otp_bist_err Bit[4]: otp_bist_done Bit[3:1]: Not used Bit[0]: otp_rd
0x3D82	R PGM PULSE	0x7D	RW	Bit[7:0]: contrl_prgram_strbe_pulse by 16*Tsclk
0x3D83	R LOAD PULSE	0x10	RW	Bit[7:5]: Not used Bit[4:0]: contrl_load_strbe_pulse by 2*Tsclk
0x3D84	R MODE CTRL	0x1C	RW	Bit[7]: pgm_dis Bit[6]: manu_mode_en Bit[5]: Reserved Bit[4]: Update load setting 1: Update dpc1_st_adr by load setting Bit[3]: 14-bit hsize for DPC sort feature Bit[2]: Select SMIC or TSMC 0: SMIC 1: TSMC Bit[1]: Clock switch select 1: otp_sram clock will switch to reg_bus clock Bit[0]: bank_sram_switch
0x3D85	R REG85	0x0B	RW	Bit[7]: dpc_sort_en Bit[6]: otp_bist_comp_val Bit[5]: Compare select 0: Compare with SRAM 1: Compare with 0/1 Bit[4]: otp_bist_en Bit[3]: pwup_load_en Bit[2]: wkup_load_en Bit[1]: hw_ld_setting_en Bit[0]: sw_ld_setting_en
0x3D86	SRAM TEST SIGNALS	0x11	RW	Bit[7:0]: RAMS[15:8]
0x3D87	R PS2CS	0x30	RW	Bit[7:0]: RAMS[7:0]
0x3D88	R STT PT H	0x00	RW	Bit[7:0]: start_addr_for_manu_mode[15:8]
0x3D89	R STT PT L	0x00	RW	Bit[7:0]: start_addr_for_manu_mode[7:0]

table 6-16 OTP_SC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3D8A	R END PT H	0x03	RW	Bit[7:0]: end_addr_for_manu_mode[15:8]
0x3D8B	R END PT L	0xFF	RW	Bit[7:0]: end_addr_for_manu_mode[7:0]
0x3D8C	R SETTING ADR STT PT H	0x00	RW	Bit[7:0]: start_addr_for_load_setting[15:8]
0x3D8D	R SETTING ADR STT PT L	0x10	RW	Bit[7:0]: start_low_addr_for_load_setting[7:0]
0x3D8E	OTP BIST ERR ADR H	–	R	Bit[7:0]: otp_bist_err_adr[15:8]
0x3D8F	OTP BIST ERR ADR L	–	R	Bit[7:0]: otp_bist_err_adr[7:0]
0x3D90	R BASE ADR H	0x00	RW	Bit[7:0]: efuse_base_address[15:8]
0x3D91	R BASE ADR L	0x00	RW	Bit[7:0]: efuse_base_address[7:0]
0x3D92	PGENB TIMING	0x1F	RW	Bit[7:4]: t_pgenb_end Bit[3:0]: t_pgenb_start
0x3D93	VDDQ TIMING	0x46	RW	Bit[7:4]: t_vddq_end Bit[3:0]: t_vddq_start
0x3D94	OTP STRBE GAP PGM	0x04	RW	Bit[7:0]: Gap between strobe pulse when programming
0x3D95	OTP STRBE GAP LOAD	0x05	RW	Bit[7:4]: Not used Bit[3:0]: Gap between strobe pulse when loading
0x3D96	SRAM RM	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: ps_to_csb_time_control by 16*Tsclk
0x3D97	AEN SETUP HOLD TIME	0x0F	RW	Bit[7:5]: Not used Bit[4:0]: AEN to RDEN/PGMEN setup and hold time by 2*Tsclk
0x3D98	A HOLD TIME	0x62	RW	Bit[7:4]: A to AEN hold when programming by 2*Tsclk Bit[3:0]: A to AEN hold when loading by 2*Tsclk
0x3D99~ 0x3DA3	RSVD	–	–	Reserved
0x3DA4	SLOPE REG	0x24	RW	Bit[7:2]: slope_end Bit[1:0]: slope_sreg
0x3DA5~ 0x3DA9	RSVD	–	–	Reserved
0x3DAA	R DPC 1ST STT ADR H	0x00	RW	Bit[7:0]: first_dpc_start_adr[15:8]
0x3DAB	R DPC 1ST STT ADR L	0x00	RW	Bit[7:0]: first_dpc_start_adr[7:0]

table 6-16 OTP_SC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3DAC	R DPC 2ND STT ADR H	0x00	RW	Bit[7:0]: second_dpc_start_adr[15:8]
0x3DAD	R DPC 2ND STT ADR L	0x00	RW	Bit[7:0]: second_dpc_start_adr[7:0]
0x3DAE	R DPC END ADR H	0x00	RW	Bit[7:0]: dpc_end_adr[15:8]
0x3DAF	R DPC END ADR L	0x00	RW	Bit[7:0]: dpc_end_adr[7:0]

6.17 SENSOR_FREX [0x3F85 - 0x3F9F]

table 6-17 SENSOR_FREX registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3F85	FREX EXP	0x00	RW	Bit[7:0]: frex_exp[23:16]
0x3F86	FREX EXP	0x00	RW	Bit[7:0]: frex_exp[15:8]
0x3F87	FREX EXP	0x05	RW	Bit[7:0]: frex_exp[7:0]
0x3F88	NOT USED	–	–	Not Used
0x3F89	STROBE WIDTH	0x00	RW	Bit[7:4]: Not used Bit[3:0]: strobe_width[19:16]
0x3F8A	STROBE WIDTH	0x06	RW	Bit[7:0]: strobe_width[15:8]
0x3F8B	STROBE WIDTH	0x00	RW	Bit[7:0]: strobe_width[7:0]
0x3F8C	SHUTTER DLY	0x00	RW	Bit[7:5]: Not used Bit[4:0]: shutter_dly[12:8]
0x3F8D	SHUTTER DLY	0x44	RW	Bit[7:0]: shutter_dly[7:0]
0x3F8E	FREX PCHG WIDTH	0x1F	RW	Bit[7:0]: frex_pchg_width[15:8]
0x3F8F	FREX PCHG WIDTH	0x40	RW	Bit[7:0]: frex_pchg_width[7:0]
0x3F90	DATOUT DLY	0x00	RW	Bit[7:0]: datout_dly[15:8]
0x3F91	DATOUT DLY	0x01	RW	Bit[7:0]: datout_dly[7:0]
0x3F92	STROBE DLY	0x00	RW	Bit[7:5]: Not used Bit[4:0]: strobe_dly[12:8]
0x3F93	STROBE DLY	0x00	RW	Bit[7:0]: strobe_dly[7:0]
0x3F94~ 0x3F9D	NOT USED	–	–	Not Used

table 6-17 SENSOR_FREX registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3F9E	R1E	0x03	RW	Bit[7:1]: Not used Bit[0]: frex_i2c_req_repeat_trig_sel 0: SOF 1: EOF
0x3F9F	FREX REQ	0x04	RW	Bit[7]: frex_i2c_req (self clearing) Bit[6]: frex_i2c_req_repeat (debug) Bit[5]: frex_strobe_out_sel Bit[4]: frex_nopchg Bit[3]: frex_strobe polarity Bit[2]: frex_shutter polarity Bit[1]: frex_i from pad in Bit[0]: no_latch at SOF for frex_i2c_req

6.18 BLC_L [0x4000 - 0x40EF]

table 6-18 BLC_L registers (sheet 1 of 10)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0xF8	RW	Bit[7]: offset_trig_en Bit[6]: exp_trig_en Bit[5]: gain_trig_en Bit[4]: fmt_trig_en Bit[3]: rst_trig_en Bit[2]: man_trig_en Bit[1]: blc_freeze Bit[0]: blc_always_update
0x4001	BLC CTRL01	0x07	RW	Bit[7]: r_gain_chg_mf_mode Bit[6]: r_fmt_chg_mf_mode Bit[5]: r_off_chg_mf_mode Bit[4]: r_rst_mf_mode Bit[3]: r_man_avg_en Bit[2]: r_gain_chg_mf_en Bit[1]: r_fmt_chg_mf_en Bit[0]: r_off_chg_mf_en
0x4002	BLC CTRL02	0xD3	RW	Bit[7:4]: For debug Bit[3]: v173_dis Bit[2]: sram_ini Bit[1]: format_trig_beh Bit[0]: gain_trig_beh
0x4003	BLC CTRL03	0x05	RW	Bit[7:0]: rst_trig_fn
0x4004	BLC CTRL04	0x05	RW	Bit[7:0]: fmt_trig_fn

table 6-18 BLC_L registers (sheet 2 of 10)

address	register name	default value	R/W	description
0x4005	BLC CTRL05	0x05	RW	Bit[7:0]: gain_trig_fn
0x4006	BLC CTRL06	0x05	RW	Bit[7:0]: off_trig_fn
0x4007	BLC CTRL07	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: avg_weight
0x4008	OFF TRIG TH	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_trig_th[9:8]
0x4009	OFF TRIG TH	0x05	RW	Bit[7:0]: off_trig_th[7:0]
0x400A	HWIN OFF	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: hwin_off[11:8]
0x400B	HWIN OFF	0x20	RW	Bit[7:0]: hwin_off[7:0]
0x400C	HWIN PAD	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: hwin_pad[11:8]
0x400D	HWIN PAD	0x20	RW	Bit[7:0]: hwin_pad[7:0]
0x400E	CTRL0E	0xC2	RW	CTRL0E
0x400F	CTRL0F	0x94	RW	CTRL0F
0x4010	BLC CTRL10	0xE8	RW	Bit[7]: zero_ln_out_en Bit[6]: blk_ln_out_en Bit[5]: dither_en Bit[4]: realgain_cmp_en Bit[3]: median_filter_en Bit[2]: disable_target_adjust Bit[1]: manualy_set_hsize Bit[0]: manualy_set_ln_num
0x4011	BLC CTRL11	0x01	RW	Bit[7:6]: Not used Bit[5]: man_off_en Bit[4]: one_ch_en Bit[3]: adp_k Bit[2]: adp_switch Bit[1]: color_diff_en Bit[0]: channel_diff_en
0x4012	BLC CTRL12	0x8C	RW	Bit[7]: Not used Bit[6]: hdr_en Bit[5]: hdr_man Bit[4]: ch_num_man Bit[3]: dcblc_en Bit[2]: blc_en Bit[1:0]: bypass_mode
0x4013	BLC CTRL13	0x40	RW	Bit[7:0]: blk_ln_num
0x4014	BLC CTRL14	0x40	RW	Bit[7:0]: zero_ln_num

table 6-18 BLC_L registers (sheet 3 of 10)

address	register name	default value	R/W	description
0x4015	BLC CTRL15	0x02	RW	Bit[7:0]: bl_start
0x4016	BLC CTRL16	0x09	RW	Bit[7:0]: bl_end
0x4017	BLC CTRL17	0x00	RW	Bit[7:0]: zl_start
0x4018	BLC CTRL18	0x07	RW	Bit[7:0]: zl_end
0x4019	BLK LVL TARGET	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: blk_lvl_target[9:8]
0x401A	BLK LVL TARGET	0x40	RW	Bit[7:0]: blk_lvl_target[7:0]
0x401B	BLC CTRL1B	0x08	RW	Bit[7:0]: mf_th
0x401C	RND GAIN TH	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: rnd_gain_th[9:8]
0x401D	RND GAIN TH	0x10	RW	Bit[7:0]: rnd_gain_th[7:0]
0x401E	OFF LIM TH	0x02	RW	Bit[7:3]: Reserved Bit[2:0]: off_lim_th[10:8]
0x401F	OFF LIM TH	0x00	RW	Bit[7:0]: off_lim_th[7:0]
0x4020	KCOEF B	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_b[12:8]
0x4021	KCOEF B	0x10	RW	Bit[7:0]: kcoef_b[7:0]
0x4022	KCOEF GB	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_gb[12:8]
0x4023	KCOEF GB	0x20	RW	Bit[7:0]: kcoef_gb[7:0]
0x4024	KCOEF GR	0x03	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_gr[12:8]
0x4025	KCOEF GR	0xFF	RW	Bit[7:0]: kcoef_gr[7:0]
0x4026	KCOEF R	0x03	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_r[12:8]
0x4027	KCOEF R	0xEF	RW	Bit[7:0]: kcoef_r[7:0]
0x4028	GAIN DEBUG	0x00	RW	Bit[7:0]: gain_debug[7:0]
0x4029	HOVERALP	0x08	RW	Bit[7:0]: Hoveralp[7:0]
0x402A	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[31:24]
0x402B	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[23:16]
0x402C	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[15:8]
0x402D	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[7:0]

table 6-18 BLC_L registers (sheet 4 of 10)

address	register name	default value	R/W	description
0x402E~ 0x402F	NOT USED	–	–	Not Used
0x4030	CMP ALPHA EXP0 B	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_b[11:8]
0x4031	CMP ALPHA EXP0 B	0x10	RW	Bit[7:0]: cmp_alpha_exp0_b[7:0]
0x4032	CMP ALPHA EXP0 GB	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_gb[11:8]
0x4033	CMP ALPHA EXP0 GB	0x10	RW	Bit[7:0]: cmp_alpha_exp0_gb[7:0]
0x4034	CMP ALPHA EXP0 GR	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_gr[11:8]
0x4035	CMP ALPHA EXP0 GR	0x10	RW	Bit[7:0]: cmp_alpha_exp0_gr[7:0]
0x4036	CMP ALPHA EXP0 R	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_r[11:8]
0x4037	CMP ALPHA EXP0 R	0x10	RW	Bit[7:0]: cmp_alpha_exp0_r[7:0]
0x4038	CMP ALPHA EXP1 B	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_b[11:8]
0x4039	CMP ALPHA EXP1 B	0x10	RW	Bit[7:0]: cmp_alpha_exp1_b[7:0]
0x403A	CMP ALPHA EXP1 GB	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_gb[11:8]
0x403B	CMP ALPHA EXP1 GB	0x10	RW	Bit[7:0]: cmp_alpha_exp1_gb[7:0]
0x403C	CMP ALPHA EXP1 GR	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_gr[11:8]
0x403D	CMP ALPHA EXP1 GR	0x10	RW	Bit[7:0]: cmp_alpha_exp1_gr[7:0]
0x403E	CMP ALPHA EXP1 R	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_r[11:8]
0x403F	CMP ALPHA EXP1 R	0x10	RW	Bit[7:0]: cmp_alpha_exp1_r[7:0]
0x4040	CMP BETA EXP0 B	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_b[11:8]
0x4041	CMP BETA EXP0 B	0x10	RW	Bit[7:0]: cmp_beta_exp0_b[7:0]
0x4042	CMP BETA EXP0 GB	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_gb[11:8]
0x4043	CMP BETA EXP0 GB	0x10	RW	Bit[7:0]: cmp_beta_exp0_gb[7:0]
0x4044	CMP BETA EXP0 GR	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_gr[11:8]
0x4045	CMP BETA EXP0 GR	0x10	RW	Bit[7:0]: cmp_beta_exp0_gr[7:0]

table 6-18 BLC_L registers (sheet 5 of 10)

address	register name	default value	R/W	description
0x4046	CMP BETA EXP0 R	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_r[11:8]
0x4047	CMP BETA EXP0 GR	0x10	RW	Bit[7:0]: cmp_beta_exp0_r[7:0]
0x4048	CMP BETA EXP1 B	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_b[11:8]
0x4049	CMP BETA EXP1 B	0x10	RW	Bit[7:0]: cmp_beta_exp1_b[7:0]
0x404A	CMP BETA EXP1 GB	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_gb[11:8]
0x404B	CMP BETA EXP1 GB	0x10	RW	Bit[7:0]: cmp_beta_exp1_gb[7:0]
0x404C	CMP BETA EXP1 GR	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_gr[11:8]
0x404D	CMP BETA EXP1 GR	0x10	RW	Bit[7:0]: cmp_beta_exp1_gr[7:0]
0x404E	CMP BETA EXP1 R	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_r[11:8]
0x404F	CMP BETA EXP1 R	0x10	RW	Bit[7:0]: cmp_beta_exp1_r[7:0]
0x4050	HSIZE	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Hsize high (IH_SW-8) bits
0x4051	HSIZE	0x00	RW	Bit[7:0]: Hsize[7:0]
0x4052	BLC CTRL52	0x02	RW	Bit[7:0]: dc_th1_exp0
0x4053	BLC CTRL53	0x04	RW	Bit[7:0]: dc_th2_exp0
0x4054	BLC CTRL54	0x02	RW	Bit[7:0]: dc_th1_exp1
0x4055	BLC CTRL55	0x04	RW	Bit[7:0]: dc_th2_exp1
0x4056	BLC CTRL56	0x25	RW	Bit[7:6]: Not used Bit[5:4]: shift_gain Bit[3]: cut_bit Bit[2]: out_bit Bit[1:0]: in_bit
0x4057	BLC CTRL57	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Chn
0x4058~ 0x405F	RSVD	–	–	Reserved
0x4060	OFFSET 0	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_0[9:8]
0x4061	OFFSET 0	0x00	RW	Bit[7:0]: offset_0[7:0]

table 6-18 BLC_L registers (sheet 6 of 10)

address	register name	default value	R/W	description
0x4062	OFFSET 1	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_1[9:8]
0x4063	OFFSET 1	0x00	RW	Bit[7:0]: offset_1[7:0]
0x4064	OFFSET 2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_2[9:8]
0x4065	OFFSET 2	0x00	RW	Bit[7:0]: offset_2[7:0]
0x4066	OFFSET 3	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_3[9:8]
0x4067	OFFSET 3	0x00	RW	Bit[7:0]: offset_3[7:0]
0x4068	OFFSET 4	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_4[9:8]
0x4069	OFFSET 4	0x00	RW	Bit[7:0]: offset_4[7:0]
0x406A	OFFSET 5	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_5[9:8]
0x406B	OFFSET 5	0x00	RW	Bit[7:0]: offset_5[7:0]
0x406C	OFFSET 6	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_6[9:8]
0x406D	OFFSET 6	0x00	RW	Bit[7:0]: offset_6[7:0]
0x406E	OFFSET 7	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_7[9:8]
0x406F	OFFSET 7	0x00	RW	Bit[7:0]: offset_7[7:0]
0x4070	OFFSET 8	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_8[9:8]
0x4071	OFFSET 8	0x00	RW	Bit[7:0]: offset_8[7:0]
0x4072	OFFSET 9	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_9[9:8]
0x4073	OFFSET 9	0x00	RW	Bit[7:0]: offset_9[7:0]
0x4074	OFFSET 10	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_10[9:8]
0x4075	OFFSET 10	0x00	RW	Bit[7:0]: offset_10[7:0]
0x4076	OFFSET 11	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_11[9:8]
0x4077	OFFSET 11	0x00	RW	Bit[7:0]: offset_11[7:0]
0x4078	OFFSET 12	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_12[9:8]

table 6-18 BLC_L registers (sheet 7 of 10)

address	register name	default value	R/W	description
0x4079	OFFSET 12	0x00	RW	Bit[7:0]: offset_12[7:0]
0x407A	OFFSET 13	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_13[9:8]
0x407B	OFFSET 13	0x00	RW	Bit[7:0]: offset_13[7:0]
0x407C	OFFSET 14	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_14[9:8]
0x407D	OFFSET 14	0x00	RW	Bit[7:0]: offset_14[7:0]
0x407E	OFFSET 15	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_15[9:8]
0x407F	OFFSET 15	0x00	RW	Bit[7:0]: offset_15[7:0]
0x4080	OFFSET 16	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_16[9:8]
0x4081	OFFSET 16	0x00	RW	Bit[7:0]: offset_16[7:0]
0x4082	OFFSET 17	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_17[9:8]
0x4083	OFFSET 17	0x00	RW	Bit[7:0]: offset_17[7:0]
0x4084	OFFSET 18	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_18[9:8]
0x4085	OFFSET 18	0x00	RW	Bit[7:0]: offset_18[7:0]
0x4086	OFFSET 19	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_19[9:8]
0x4087	OFFSET 19	0x00	RW	Bit[7:0]: offset_19[7:0]
0x4088	OFFSET 20	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_20[9:8]
0x4089	OFFSET 20	0x00	RW	Bit[7:0]: offset_20[7:0]
0x408A	OFFSET 21	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_21[9:8]
0x408B	OFFSET 21	0x00	RW	Bit[7:0]: offset_21[7:0]
0x408C	OFFSET 22	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_22[9:8]
0x408D	OFFSET 22	0x00	RW	Bit[7:0]: offset_22[7:0]
0x408E	OFFSET 23	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_23[9:8]
0x408F	OFFSET 23	0x00	RW	Bit[7:0]: offset_23[7:0]

table 6-18 BLC_L registers (sheet 8 of 10)

address	register name	default value	R/W	description
0x4090	OFFSET 24	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_24[9:8]
0x4091	OFFSET 24	0x00	RW	Bit[7:0]: offset_24[7:0]
0x4092	OFFSET 25	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_25[9:8]
0x4093	OFFSET 25	0x00	RW	Bit[7:0]: offset_25[7:0]
0x4094	OFFSET 26	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_26[9:8]
0x4095	OFFSET 26	0x00	RW	Bit[7:0]: offset_26[7:0]
0x4096	OFFSET 27	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_27[9:8]
0x4097	OFFSET 27	0x00	RW	Bit[7:0]: offset_27[7:0]
0x4098	OFFSET 28	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_28[9:8]
0x4099	OFFSET 28	0x00	RW	Bit[7:0]: offset_28[7:0]
0x409A	OFFSET 29	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_29[9:8]
0x409B	OFFSET 29	0x00	RW	Bit[7:0]: offset_29[7:0]
0x409C	OFFSET 30	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_30[9:8]
0x409D	OFFSET 30	0x00	RW	Bit[7:0]: offset_30[7:0]
0x409E	OFFSET 31	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_31[9:8]
0x409F	OFFSET 31	0x00	RW	Bit[7:0]: offset_31[7:0]
0x40A0	BLC CTRLA0	0x00	RW	Bit[7:0]: sram_base_addr_z_sum
0x40A1	BLC CTRLA1	0x40	RW	Bit[7:0]: sram_base_addr_z_cnt
0x40A2	BLC CTRLA2	0x20	RW	Bit[7:0]: sram_base_addr_b_sum
0x40A3	BLC CTRLA3	0x48	RW	Bit[7:0]: sram_base_addr_b_cnt
0x40A4	BLC CTRLA4	0x64	RW	Bit[7:0]: sram_base_addr_z_avg
0x40A5	BLC CTRLA5	0x6C	RW	Bit[7:0]: sram_base_addr_b_avg
0x40A6	BLC CTRLA6	0xA0	RW	Bit[7:0]: sram_base_addr_pre_offset_a
0x40A7	BLC CTRLA7	0xA8	RW	Bit[7:0]: sram_base_addr_cur_offset_a
0x40A8	BLC CTRLA8	0xB0	RW	Bit[7:0]: sram_base_addr_pre_offset_b

table 6-18 BLC_L registers (sheet 9 of 10)

address	register name	default value	R/W	description
0x40A9	BLC CTRLA9	0xB8	RW	Bit[7:0]: sram_base_addr_cur_offset_b
0x40AA	BLC CTRLAA	0xC0	RW	Bit[7:0]: sram_base_addr_pre_offset_c
0x40AB	BLC CTRLAB	0xC8	RW	Bit[7:0]: sram_base_addr_cur_offset_c
0x40AC	BLC CTRLAC	0x07	RW	Bit[7:0]: b_cal_step_cnt_ch16
0x40AD	BLC CTRLAB	0x05	RW	Bit[7:0]: b_cal_step_cnt_ch8
0x40AE	BLC CTRLAE	0x04	RW	Bit[7:0]: b_cal_step_cnt_ch4
0x40AF	BLC CTRLAF	0x01	RW	Bit[7:0]: z_cal_step_cnt
0x40B0	BLC CTRLB0	0x64	RW	Bit[7:0]: r_cal_ph_cnt
0x40B1	BLC CTRLB1	0x28	RW	Bit[7:0]: div_mul_start
0x40B2	BLC CTRLB2	0x50	RW	Bit[7:0]: div_mul_end
0x40B3	BLC CTRLB3	0x00	RW	BLC_CTRLB3
0x40B4	BLC CTRLB4	0xD0	RW	Bit[7:0]: sram_base_addr_pre_64_offset_a
0x40B5	BLC CTRLB4	0xD8	RW	Bit[7:0]: sram_base_addr_pre_64_offset_b
0x40B6	BLC CTRLB4	0xE0	RW	Bit[7:0]: sram_base_addr_pre_64_offset_c
0x40B7~ 0x40BF	NOT USED	–	–	Not Used
0x40C0	BLC TARGET	–	R	Bit[7:6]: Reserved Bit[5:0]: blc_target[13:8]
0x40C1	BLC TARGET	–	R	Bit[7:0]: blc_target[7:0]
0x40C2	SRAM CTRL	0x11	RW	Bit[7]: Reserved Bit[6]: sram_test Bit[5:0]: sram_rm[13:8]
0x40C3	SRAM CTRL	0x30	RW	Bit[7:0]: sram_rm[7:0]
0x40C4~ 0x40CF	NOT USED	–	–	Not Used
0x40D0	OFFSET CAL FRAC0	–	R	Bit[7:0]: offset_cal_frac0[7:0]
0x40D1	OFFSET CAL FRAC1	–	R	Bit[7:0]: offset_cal_frac1[7:0]
0x40D2	OFFSET CAL FRAC2	–	R	Bit[7:0]: offset_cal_frac2[7:0]
0x40D3	OFFSET CAL FRAC3	–	R	Bit[7:0]: offset_cal_frac3[7:0]
0x40D4	OFFSET CAL FRAC4	–	R	Bit[7:0]: offset_cal_frac4[7:0]
0x40D5	OFFSET CAL FRAC5	–	R	Bit[7:0]: offset_cal_frac5[7:0]
0x40D6	OFFSET CAL FRAC6	–	R	Bit[7:0]: offset_cal_frac6[7:0]

table 6-18 BLC_L registers (sheet 10 of 10)

address	register name	default value	R/W	description
0x40D7	OFFSET CAL FRAC7	–	R	Bit[7:0]: offset_cal_frac7[7:0]
0x40D8	OFFSET CAL FRAC8	–	R	Bit[7:0]: offset_cal_frac8[7:0]
0x40D9	OFFSET CAL FRAC9	–	R	Bit[7:0]: offset_cal_frac9[7:0]
0x40DA	OFFSET CAL FRACA	–	R	Bit[7:0]: offset_cal_fraca[7:0]
0x40DB	OFFSET CAL FRACB	–	R	Bit[7:0]: offset_cal_fracb[7:0]
0x40DC	OFFSET CAL FRACC	–	R	Bit[7:0]: offset_cal_fracc[7:0]
0x40DD	OFFSET CAL FRACD	–	R	Bit[7:0]: offset_cal_fracd[7:0]
0x40DE	OFFSET CAL FRACE	–	R	Bit[7:0]: offset_cal_frace[7:0]
0x40DF	OFFSET CAL FRACF	–	R	Bit[7:0]: offset_cal_fracf[7:0]
0x40E0	OFFSET CAL FRAC10	–	R	Bit[7:0]: offset_cal_frac10[7:0]
0x40E1	OFFSET CAL FRAC11	–	R	Bit[7:0]: offset_cal_frac11[7:0]
0x40E2	OFFSET CAL FRAC12	–	R	Bit[7:0]: offset_cal_frac12[7:0]
0x40E3	OFFSET CAL FRAC13	–	R	Bit[7:0]: offset_cal_frac13[7:0]
0x40E4	OFFSET CAL FRAC14	–	R	Bit[7:0]: offset_cal_frac14[7:0]
0x40E5	OFFSET CAL FRAC15	–	R	Bit[7:0]: offset_cal_frac15[7:0]
0x40E6	OFFSET CAL FRAC16	–	R	Bit[7:0]: offset_cal_frac16[7:0]
0x40E7	OFFSET CAL FRAC17	–	R	Bit[7:0]: offset_cal_frac17[7:0]
0x40E8	OFFSET CAL FRAC18	–	R	Bit[7:0]: offset_cal_frac18[7:0]
0x40E9	OFFSET CAL FRAC19	–	R	Bit[7:0]: offset_cal_frac19[7:0]
0x40EA	OFFSET CAL FRAC1A	–	R	Bit[7:0]: offset_cal_frac1a[7:0]
0x40EB	OFFSET CAL FRAC1B	–	R	Bit[7:0]: offset_cal_frac1b[7:0]
0x40EC	OFFSET CAL FRAC1C	–	R	Bit[7:0]: offset_cal_frac1c[7:0]
0x40ED	OFFSET CAL FRAC1D	–	R	Bit[7:0]: offset_cal_frac1d[7:0]
0x40EE	OFFSET CAL FRAC1E	–	R	Bit[7:0]: offset_cal_frac1e[7:0]
0x40EF	OFFSET CAL FRAC1F	–	R	Bit[7:0]: offset_cal_frac1f[7:0]

6.19 BLC_M [0x4900 - 0x49EF]

table 6-19 BLC_M registers (sheet 1 of 10)

address	register name	default value	R/W	description
0x4900	BLC CTRL00	0xF8	RW	Bit[7]: offset_trig_en Bit[6]: exp_trig_en Bit[5]: gain_trig_en Bit[4]: fmt_trig_en Bit[3]: rst_trig_en Bit[2]: man_trig_en Bit[1]: blc_freeze Bit[0]: blc_always_update
0x4901	BLC CTRL01	0x07	RW	Bit[7]: r_gain_chg_mf_mode Bit[6]: r_fmt_chg_mf_mode Bit[5]: r_off_chg_mf_mode Bit[4]: r_rst_mf_mode Bit[3]: r_man_avg_en Bit[2]: r_gain_chg_mf_en Bit[1]: r_fmt_chg_mf_en Bit[0]: r_off_chg_mf_en
0x4902	BLC CTRL02	0xD3	RW	Bit[7:4]: For debug Bit[3]: v173_dis Bit[2]: sram_ini Bit[1]: format_trig_beh Bit[0]: gain_trig_beh
0x4903	BLC CTRL03	0x05	RW	Bit[7:0]: rst_trig_fn
0x4904	BLC CTRL04	0x05	RW	Bit[7:0]: fmt_trig_fn
0x4905	BLC CTRL05	0x05	RW	Bit[7:0]: gain_trig_fn
0x4906	BLC CTRL06	0x05	RW	Bit[7:0]: off_trig_fn
0x4907	BLC CTRL07	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: avg_weight
0x4908	OFF TRIG TH	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_trig_th[9:8]
0x4909	OFF TRIG TH	0x05	RW	Bit[7:0]: off_trig_th[7:0]
0x490A	HWIN OFF	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: hwin_off[11:8]
0x490B	HWIN OFF	0x20	RW	Bit[7:0]: hwin_off[7:0]
0x490C	HWIN PAD	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: hwin_pad[11:8]
0x490D	HWIN PAD	0x20	RW	Bit[7:0]: hwin_pad[7:0]

table 6-19 BLC_M registers (sheet 2 of 10)

address	register name	default value	R/W	description
0x490E	CTRL0E	0xC2	RW	CTRL0E
0x490F	CTRL0F	0x94	RW	CTRL0F
0x4910	BLC CTRL10	0xE8	RW	Bit[7]: zero_ln_out_en Bit[6]: blk_ln_out_en Bit[5]: dither_en Bit[4]: realgain_cmp_en Bit[3]: median_filter_en Bit[2]: disable_target_adjust Bit[1]: manualy_set_hsize Bit[0]: manualy_set_ln_num
0x4911	BLC CTRL11	0x01	RW	Bit[7:6]: Not used Bit[5]: man_off_en Bit[4]: one_ch_en Bit[3]: adp_k Bit[2]: adp_switch Bit[1]: color_diff_en Bit[0]: channel_diff_en
0x4912	BLC CTRL12	0x8C	RW	Bit[7]: Not used Bit[6]: hdr_en Bit[5]: hdr_man Bit[4]: ch_num_man Bit[3]: dcblc_en Bit[2]: blc_en Bit[1:0]: bypass_mode
0x4913	BLC CTRL13	0x40	RW	Bit[7:0]: blk_ln_num
0x4914	BLC CTRL14	0x40	RW	Bit[7:0]: zero_ln_num
0x4915	BLC CTRL15	0x02	RW	Bit[7:0]: bl_start
0x4916	BLC CTRL16	0x09	RW	Bit[7:0]: bl_end
0x4917	BLC CTRL17	0x00	RW	Bit[7:0]: zl_start
0x4918	BLC CTRL18	0x07	RW	Bit[7:0]: zl_end
0x4919	BLK LVL TARGET	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: blk_lvl_target[9:8]
0x491A	BLK LVL TARGET	0x40	RW	Bit[7:0]: blk_lvl_target[7:0]
0x491B	BLC CTRL1B	0x08	RW	Bit[7:0]: mf_th
0x491C	RND GAIN TH	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: rnd_gain_th[9:8]
0x491D	RND GAIN TH	0x10	RW	Bit[7:0]: rnd_gain_th[7:0]
0x491E	OFF LIM TH	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: off_lim_th[11:8]

table 6-19 BLC_M registers (sheet 3 of 10)

address	register name	default value	R/W	description
0x491F	OFF LIM TH	0x00	RW	Bit[7:0]: off_lim_th[7:0]
0x4920	KCOEF B	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_b[12:8]
0x4921	KCOEF B	0x10	RW	Bit[7:0]: kcoef_b[7:0]
0x4922	KCOEF GB	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_gb[12:8]
0x4923	KCOEF GB	0x20	RW	Bit[7:0]: kcoef_gb[7:0]
0x4924	KCOEF GR	0x03	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_gr[12:8]
0x4925	KCOEF GR	0xFF	RW	Bit[7:0]: kcoef_gr[7:0]
0x4926	KCOEF R	0x03	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_r[12:8]
0x4927	KCOEF R	0xEF	RW	Bit[7:0]: kcoef_r[7:0]
0x4928	GAIN DEBUG	0x00	RW	Bit[7:0]: gain_debug[7:0]
0x4929	HOVERALP	0x08	RW	Bit[7:0]: Hoveralp[7:0]
0x492A	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[31:24]
0x492B	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[23:16]
0x492C	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[15:8]
0x492D	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[7:0]
0x492E~ 0x492F	RSVD	–	–	Reserved
0x4930	CMP ALPHA EXP0 B	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_b[11:8]
0x4931	CMP ALPHA EXP0 B	0x10	RW	Bit[7:0]: cmp_alpha_exp0_b[7:0]
0x4932	CMP ALPHA EXP0 GB	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_gb[11:8]
0x4933	CMP ALPHA EXP0 GB	0x10	RW	Bit[7:0]: cmp_alpha_exp0_gb[7:0]
0x4934	CMP ALPHA EXP0 GR	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_gr[11:8]
0x4935	CMP ALPHA EXP0 GR	0x10	RW	Bit[7:0]: cmp_alpha_exp0_gr[7:0]
0x4936	CMP ALPHA EXP0 R	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_r[11:8]
0x4937	CMP ALPHA EXP0 R	0x10	RW	Bit[7:0]: cmp_alpha_exp0_r[7:0]

table 6-19 BLC_M registers (sheet 4 of 10)

address	register name	default value	R/W	description
0x4938	CMP ALPHA EXP1 B	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_b[11:8]
0x4939	CMP ALPHA EXP1 B	0x10	RW	Bit[7:0]: cmp_alpha_exp1_b[7:0]
0x493A	CMP ALPHA EXP1 GB	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_gb[11:8]
0x493B	CMP ALPHA EXP1 GB	0x10	RW	Bit[7:0]: cmp_alpha_exp1_gb[7:0]
0x493C	CMP ALPHA EXP1 GR	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_gr[11:8]
0x493D	CMP ALPHA EXP1 GR	0x10	RW	Bit[7:0]: cmp_alpha_exp1_gr[7:0]
0x493E	CMP ALPHA EXP1 R	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_r[11:8]
0x493F	CMP ALPHA EXP1 R	0x10	RW	Bit[7:0]: cmp_alpha_exp1_r[7:0]
0x4940	CMP BETA EXP0 B	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_b[11:8]
0x4941	CMP BETA EXP0 B	0x10	RW	Bit[7:0]: cmp_beta_exp0_b[7:0]
0x4942	CMP BETA EXP0 GB	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_gb[11:8]
0x4943	CMP BETA EXP0 GB	0x10	RW	Bit[7:0]: cmp_beta_exp0_gb[7:0]
0x4944	CMP BETA EXP0 GR	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_gr[11:8]
0x4945	CMP BETA EXP0 GR	0x10	RW	Bit[7:0]: cmp_beta_exp0_gr[7:0]
0x4946	CMP BETA EXP0 R	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_r[11:8]
0x4947	CMP BETA EXP0 GR	0x10	RW	Bit[7:0]: cmp_beta_exp0_r[7:0]
0x4948	CMP BETA EXP1 B	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_b[11:8]
0x4949	CMP BETA EXP1 B	0x10	RW	Bit[7:0]: cmp_beta_exp1_b[7:0]
0x494A	CMP BETA EXP1 GB	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_gb[11:8]
0x494B	CMP BETA EXP1 GB	0x10	RW	Bit[7:0]: cmp_beta_exp1_gb[7:0]
0x494C	CMP BETA EXP1 GR	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_gr[11:8]
0x494D	CMP BETA EXP1 GR	0x10	RW	Bit[7:0]: cmp_beta_exp1_gr[7:0]
0x494E	CMP BETA EXP1 R	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_r[11:8]

table 6-19 BLC_M registers (sheet 5 of 10)

address	register name	default value	R/W	description
0x494F	CMP BETA EXP1 R	0x10	RW	Bit[7:0]: cmp_beta_exp1_r[7:0]
0x4950	HSIZE	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Hsize high (IH_SW-8) bits
0x4951	HSIZE	0x00	RW	Bit[7:0]: Hsize[7:0]
0x4952	BLC CTRL52	0x02	RW	Bit[7:0]: dc_th1_exp0
0x4953	BLC CTRL53	0x04	RW	Bit[7:0]: dc_th2_exp0
0x4954	BLC CTRL54	0x02	RW	Bit[7:0]: dc_th1_exp1
0x4955	BLC CTRL55	0x04	RW	Bit[7:0]: dc_th2_exp1
0x4956	BLC CTRL56	0x25	RW	Bit[7:6]: Not used Bit[5:4]: shift_gain Bit[3]: cut_bit Bit[2]: out_bit Bit[1:0]: in_bit
0x4957	BLC CTRL57	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Chn
0x4958~ 0x495F	RSVD	–	–	Reserved
0x4960	OFFSET 0	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_0[9:8]
0x4961	OFFSET 0	0x00	RW	Bit[7:0]: offset_0[7:0]
0x4962	OFFSET 1	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_1[9:8]
0x4963	OFFSET 1	0x00	RW	Bit[7:0]: offset_1[7:0]
0x4964	OFFSET 2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_2[9:8]
0x4965	OFFSET 2	0x00	RW	Bit[7:0]: offset_2[7:0]
0x4966	OFFSET 3	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_3[9:8]
0x4967	OFFSET 3	0x00	RW	Bit[7:0]: offset_3[7:0]
0x4968	OFFSET 4	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_4[9:8]
0x4969	OFFSET 4	0x00	RW	Bit[7:0]: offset_4[7:0]
0x496A	OFFSET 5	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_5[9:8]
0x496B	OFFSET 5	0x00	RW	Bit[7:0]: offset_5[7:0]

table 6-19 BLC_M registers (sheet 6 of 10)

address	register name	default value	R/W	description
0x496C	OFFSET 6	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_6[9:8]
0x496D	OFFSET 6	0x00	RW	Bit[7:0]: offset_6[7:0]
0x496E	OFFSET 7	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_7[9:8]
0x496F	OFFSET 7	0x00	RW	Bit[7:0]: offset_7[7:0]
0x4970	OFFSET 8	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_8[9:8]
0x4971	OFFSET 8	0x00	RW	Bit[7:0]: offset_8[7:0]
0x4972	OFFSET 9	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_9[9:8]
0x4973	OFFSET 9	0x00	RW	Bit[7:0]: offset_9[7:0]
0x4974	OFFSET 10	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_10[9:8]
0x4975	OFFSET 10	0x00	RW	Bit[7:0]: offset_10[7:0]
0x4976	OFFSET 11	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_11[9:8]
0x4977	OFFSET 11	0x00	RW	Bit[7:0]: offset_11[7:0]
0x4978	OFFSET 12	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_12[9:8]
0x4979	OFFSET 12	0x00	RW	Bit[7:0]: offset_12[7:0]
0x497A	OFFSET 13	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_13[9:8]
0x497B	OFFSET 13	0x00	RW	Bit[7:0]: offset_13[7:0]
0x497C	OFFSET 14	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_14[9:8]
0x497D	OFFSET 14	0x00	RW	Bit[7:0]: offset_14[7:0]
0x497E	OFFSET 15	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_15[9:8]
0x497F	OFFSET 15	0x00	RW	Bit[7:0]: offset_15[7:0]
0x4980	OFFSET 16	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_16[9:8]
0x4981	OFFSET 16	0x00	RW	Bit[7:0]: offset_16[7:0]
0x4982	OFFSET 17	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_17[9:8]

table 6-19 BLC_M registers (sheet 7 of 10)

address	register name	default value	R/W	description
0x4983	OFFSET 17	0x00	RW	Bit[7:0]: offset_17[7:0]
0x4984	OFFSET 18	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_18[9:8]
0x4985	OFFSET 18	0x00	RW	Bit[7:0]: offset_18[7:0]
0x4986	OFFSET 19	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_19[9:8]
0x4987	OFFSET 19	0x00	RW	Bit[7:0]: offset_19[7:0]
0x4988	OFFSET 20	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_20[9:8]
0x4989	OFFSET 20	0x00	RW	Bit[7:0]: offset_20[7:0]
0x498A	OFFSET 21	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_21[9:8]
0x498B	OFFSET 21	0x00	RW	Bit[7:0]: offset_21[7:0]
0x498C	OFFSET 22	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_22[9:8]
0x498D	OFFSET 22	0x00	RW	Bit[7:0]: offset_22[7:0]
0x498E	OFFSET 23	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_23[9:8]
0x498F	OFFSET 23	0x00	RW	Bit[7:0]: offset_23[7:0]
0x4990	OFFSET 24	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_24[9:8]
0x4991	OFFSET 24	0x00	RW	Bit[7:0]: offset_24[7:0]
0x4992	OFFSET 25	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_25[9:8]
0x4993	OFFSET 25	0x00	RW	Bit[7:0]: offset_25[7:0]
0x4994	OFFSET 26	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_26[9:8]
0x4995	OFFSET 26	0x00	RW	Bit[7:0]: offset_26[7:0]
0x4996	OFFSET 27	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_27[9:8]
0x4997	OFFSET 27	0x00	RW	Bit[7:0]: offset_27[7:0]
0x4998	OFFSET 28	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_28[9:8]
0x4999	OFFSET 28	0x00	RW	Bit[7:0]: offset_28[7:0]

table 6-19 BLC_M registers (sheet 8 of 10)

address	register name	default value	R/W	description
0x499A	OFFSET 29	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_29[9:8]
0x499B	OFFSET 29	0x00	RW	Bit[7:0]: offset_29[7:0]
0x499C	OFFSET 30	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_30[9:8]
0x499D	OFFSET 30	0x00	RW	Bit[7:0]: offset_30[7:0]
0x499E	OFFSET 31	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_31[9:8]
0x499F	OFFSET 31	0x00	RW	Bit[7:0]: offset_31[7:0]
0x49A0	BLC CTRLA0	0x00	RW	Bit[7:0]: sram_base_addr_z_sum
0x49A1	BLC CTRLA1	0x40	RW	Bit[7:0]: sram_base_addr_z_cnt
0x49A2	BLC CTRLA2	0x20	RW	Bit[7:0]: sram_base_addr_b_sum
0x49A3	BLC CTRLA3	0x48	RW	Bit[7:0]: sram_base_addr_b_cnt
0x49A4	BLC CTRLA4	0x64	RW	Bit[7:0]: sram_base_addr_z_avg
0x49A5	BLC CTRLA5	0x6C	RW	Bit[7:0]: sram_base_addr_b_avg
0x49A6	BLC CTRLA6	0xA0	RW	Bit[7:0]: sram_base_addr_pre_offset_a
0x49A7	BLC CTRLA7	0xA8	RW	Bit[7:0]: sram_base_addr_cur_offset_a
0x49A8	BLC CTRLA8	0xB0	RW	Bit[7:0]: sram_base_addr_pre_offset_b
0x49A9	BLC CTRLA9	0xB8	RW	Bit[7:0]: sram_base_addr_cur_offset_b
0x49AA	BLC CTRLAA	0xC0	RW	Bit[7:0]: sram_base_addr_pre_offset_c
0x49AB	BLC CTRLAB	0xC8	RW	Bit[7:0]: sram_base_addr_cur_offset_c
0x49AC	BLC CTRLAC	0x07	RW	Bit[7:0]: b_cal_step_cnt_ch16
0x49AD	BLC CTRLAB	0x05	RW	Bit[7:0]: b_cal_step_cnt_ch8
0x49AE	BLC CTRLAE	0x04	RW	Bit[7:0]: b_cal_step_cnt_ch4
0x49AF	BLC CTRLAF	0x01	RW	Bit[7:0]: z_cal_step_cnt
0x49B0	BLC CTRLB0	0x64	RW	Bit[7:0]: r_cal_ph_cnt
0x49B1	BLC CTRLB1	0x28	RW	Bit[7:0]: div_mul_start
0x49B2	BLC CTRLB2	0x50	RW	Bit[7:0]: div_mul_end
0x49B3	BLC CTRLB3	0x00	RW	Bit[7:0]: blc_ctrlb3
0x49B4	BLC CTRLB4	0xD0	RW	Bit[7:0]: sram_base_addr_pre_64_offset_a
0x49B5	BLC CTRLB4	0xD8	RW	Bit[7:0]: sram_base_addr_pre_64_offset_b

table 6-19 BLC_M registers (sheet 9 of 10)

address	register name	default value	R/W	description
0x49B6	BLC CTRLB4	0xE0	RW	Bit[7:0]: sram_base_addr_pre_64_offset_c
0x49B7~ 0x49BF	RSVD	–	–	Reserved
0x49C0	BLC TARGET	–	R	Bit[7:6]: Reserved Bit[5:0]: blc_target[13:8]
0x49C1	BLC TARGET	–	R	Bit[7:0]: blc_target[7:0]
0x49C2	SRAM CTRL	0x11	RW	Bit[7]: Reserved Bit[6]: sram_test Bit[5:0]: sram_rm[13:8]
0x49C3	SRAM CTRL	0x30	RW	Bit[7:0]: sram_rm[7:0]
0x49C4~ 0x49CF	RSVD	–	–	Reserved
0x49D0	OFFSET CAL FRAC0	–	R	Bit[7:0]: offset_cal_frac0[7:0]
0x49D1	OFFSET CAL FRAC1	–	R	Bit[7:0]: offset_cal_frac1[7:0]
0x49D2	OFFSET CAL FRAC2	–	R	Bit[7:0]: offset_cal_frac2[7:0]
0x49D3	OFFSET CAL FRAC3	–	R	Bit[7:0]: offset_cal_frac3[7:0]
0x49D4	OFFSET CAL FRAC4	–	R	Bit[7:0]: offset_cal_frac4[7:0]
0x49D5	OFFSET CAL FRAC5	–	R	Bit[7:0]: offset_cal_frac5[7:0]
0x49D6	OFFSET CAL FRAC6	–	R	Bit[7:0]: offset_cal_frac6[7:0]
0x49D7	OFFSET CAL FRAC7	–	R	Bit[7:0]: offset_cal_frac7[7:0]
0x49D8	OFFSET CAL FRAC8	–	R	Bit[7:0]: offset_cal_frac8[7:0]
0x49D9	OFFSET CAL FRAC9	–	R	Bit[7:0]: offset_cal_frac9[7:0]
0x49DA	OFFSET CAL FRACA	–	R	Bit[7:0]: offset_cal_fraca[7:0]
0x49DB	OFFSET CAL FRACB	–	R	Bit[7:0]: offset_cal_fracb[7:0]
0x49DC	OFFSET CAL FRACC	–	R	Bit[7:0]: offset_cal_fracc[7:0]
0x49DD	OFFSET CAL FRACD	–	R	Bit[7:0]: offset_cal_fracd[7:0]
0x49DE	OFFSET CAL FRACE	–	R	Bit[7:0]: offset_cal_frace[7:0]
0x49DF	OFFSET CAL FRACF	–	R	Bit[7:0]: offset_cal_fracf[7:0]
0x49E0	OFFSET CAL FRAC10	–	R	Bit[7:0]: offset_cal_frac10[7:0]
0x49E1	OFFSET CAL FRAC11	–	R	Bit[7:0]: offset_cal_frac11[7:0]
0x49E2	OFFSET CAL FRAC12	–	R	Bit[7:0]: offset_cal_frac12[7:0]
0x49E3	OFFSET CAL FRAC13	–	R	Bit[7:0]: offset_cal_frac13[7:0]

table 6-19 BLC_M registers (sheet 10 of 10)

address	register name	default value	R/W	description
0x49E4	OFFSET CAL FRAC14	–	R	Bit[7:0]: offset_cal_frac14[7:0]
0x49E5	OFFSET CAL FRAC15	–	R	Bit[7:0]: offset_cal_frac15[7:0]
0x49E6	OFFSET CAL FRAC16	–	R	Bit[7:0]: offset_cal_frac16[7:0]
0x49E7	OFFSET CAL FRAC17	–	R	Bit[7:0]: offset_cal_frac17[7:0]
0x49E8	OFFSET CAL FRAC18	–	R	Bit[7:0]: offset_cal_frac18[7:0]
0x49E9	OFFSET CAL FRAC19	–	R	Bit[7:0]: offset_cal_frac19[7:0]
0x49EA	OFFSET CAL FRAC1A	–	R	Bit[7:0]: offset_cal_frac1a[7:0]
0x49EB	OFFSET CAL FRAC1B	–	R	Bit[7:0]: offset_cal_frac1b[7:0]
0x49EC	OFFSET CAL FRAC1C	–	R	Bit[7:0]: offset_cal_frac1c[7:0]
0x49ED	OFFSET CAL FRAC1D	–	R	Bit[7:0]: offset_cal_frac1d[7:0]
0x49EE	OFFSET CAL FRAC1E	–	R	Bit[7:0]: offset_cal_frac1e[7:0]
0x49EF	OFFSET CAL FRAC1F	–	R	Bit[7:0]: offset_cal_frac1f[7:0]

6.20 BLC_S [0x4A00 - 0x4AEF]

table 6-20 BLC_S registers (sheet 1 of 11)

address	register name	default value	R/W	description
0x4A00	BLC CTRL00	0xF8	RW	Bit[7]: offset_trig_en Bit[6]: exp_trig_en Bit[5]: gain_trig_en Bit[4]: fmt_trig_en Bit[3]: rst_trig_en Bit[2]: man_trig_en Bit[1]: blc_freeze Bit[0]: blc_always_update
0x4A01	BLC CTRL01	0x07	RW	Bit[7]: r_gain_chg_mf_mode Bit[6]: r_fmt_chg_mf_mode Bit[5]: r_off_chg_mf_mode Bit[4]: r_rst_mf_mode Bit[3]: r_man_avg_en Bit[2]: r_gain_chg_mf_en Bit[1]: r_fmt_chg_mf_en Bit[0]: r_off_chg_mf_en

table 6-20 BLC_S registers (sheet 2 of 11)

address	register name	default value	R/W	description
0x4A02	BLC CTRL02	0xD3	RW	Bit[7:4]: for_debug Bit[3]: v173_dis Bit[2]: sram_ini Bit[1]: format_trig_beh Bit[0]: gain_trig_beh
0x4A03	BLC CTRL03	0x05	RW	Bit[7:0]: rst_trig_fn
0x4A04	BLC CTRL04	0x05	RW	Bit[7:0]: fmt_trig_fn
0x4A05	BLC CTRL05	0x05	RW	Bit[7:0]: gain_trig_fn
0x4A06	BLC CTRL06	0x05	RW	Bit[7:0]: off_trig_fn
0x4A07	BLC CTRL07	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: avg_weight
0x4A08	OFF TRIG TH	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: off_trig_th[9:8]
0x4A09	OFF TRIG TH	0x05	RW	Bit[7:0]: off_trig_th[7:0]
0x4A0A	HWIN OFF	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: hwin_off[11:8]
0x4A0B	HWIN OFF	0x20	RW	Bit[7:0]: hwin_off[7:0]
0x4A0C	HWIN PAD	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: hwin_pad[11:8]
0x4A0D	HWIN PAD	0x20	RW	Bit[7:0]: hwin_pad[7:0]
0x4A0E	CTRL0E	0xC2	RW	CTRL0E
0x4A0F	CTRL0F	0x94	RW	CTRL0F
0x4A10	BLC CTRL10	0xE8	RW	Bit[7]: zero_ln_out_en Bit[6]: blk_ln_out_en Bit[5]: dither_en Bit[4]: realgain_cmp_en Bit[3]: median_filter_en Bit[2]: disable_target_adjust Bit[1]: manualy_set_hsize Bit[0]: manualy_set_ln_num
0x4A11	BLC CTRL11	0x01	RW	Bit[7:6]: Not used Bit[5]: man_off_en Bit[4]: one_ch_en Bit[3]: adp_k Bit[2]: adp_switch Bit[1]: color_diff_en Bit[0]: channel_diff_en

table 6-20 BLC_S registers (sheet 3 of 11)

address	register name	default value	R/W	description
0x4A12	BLC CTRL12	0x8C	RW	Bit[7]: Not used Bit[6]: hdr_en Bit[5]: hdr_man Bit[4]: ch_num_man Bit[3]: dcblc_en Bit[2]: blc_en Bit[1:0]: bypass_mode
0x4A13	BLC CTRL13	0x40	RW	Bit[7:0]: blk_ln_num
0x4A14	BLC CTRL14	0x40	RW	Bit[7:0]: zero_ln_num
0x4A15	BLC CTRL15	0x02	RW	Bit[7:0]: bl_start
0x4A16	BLC CTRL16	0x09	RW	Bit[7:0]: bl_end
0x4A17	BLC CTRL17	0x00	RW	Bit[7:0]: zl_start
0x4A18	BLC CTRL18	0x07	RW	Bit[7:0]: zl_end
0x4A19	BLK LVL TARGET	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: blk_lvl_target[9:8]
0x4A1A	BLK LVL TARGET	0x40	RW	Bit[7:0]: blk_lvl_target[7:0]
0x4A1B	BLC CTRL1B	0x08	RW	Bit[7:0]: mf_th
0x4A1C	RND GAIN TH	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: rnd_gain_th[9:8]
0x4A1D	RND GAIN TH	0x10	RW	Bit[7:0]: rnd_gain_th[7:0]
0x4A1E	OFF LIM TH	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: off_lim_th[11:8]
0x4A1F	OFF LIM TH	0x00	RW	Bit[7:0]: off_lim_th[7:0]
0x4A20	KCOEF B	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_b[12:8]
0x4A21	KCOEF B	0x10	RW	Bit[7:0]: kcoef_b[7:0]
0x4A22	KCOEF GB	0x04	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_gb[12:8]
0x4A23	KCOEF GB	0x20	RW	Bit[7:0]: kcoef_gb[7:0]
0x4A24	KCOEF GR	0x03	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_gr[12:8]
0x4A25	KCOEF GR	0xFF	RW	Bit[7:0]: kcoef_gr[7:0]
0x4A26	KCOEF R	0x03	RW	Bit[7:5]: Reserved Bit[4:0]: kcoef_r[12:8]
0x4A27	KCOEF R	0xEF	RW	Bit[7:0]: kcoef_r[7:0]

table 6-20 BLC_S registers (sheet 4 of 11)

address	register name	default value	R/W	description
0x4A28	GAIN DEBUG	0x00	RW	Bit[7:0]: gain_debug[7:0]
0x4A29	HOVERALP	0x08	RW	Bit[7:0]: Hoveralp[7:0]
0x4A2A	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[31:24]
0x4A2B	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[23:16]
0x4A2C	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[15:8]
0x4A2D	DIGI GAIN MAP	0x78	RW	Bit[7:0]: digi_gain_map[7:0]
0x4A2E~ 0x4A2F	RSVD	–	–	Reserved
0x4A30	CMP ALPHA EXP0 B	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_b[11:8]
0x4A31	CMP ALPHA EXP0 B	0x10	RW	Bit[7:0]: cmp_alpha_exp0_b[7:0]
0x4A32	CMP ALPHA EXP0 GB	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_gb[11:8]
0x4A33	CMP ALPHA EXP0 GB	0x10	RW	Bit[7:0]: cmp_alpha_exp0_gb[7:0]
0x4A34	CMP ALPHA EXP0 GR	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_gr[11:8]
0x4A35	CMP ALPHA EXP0 GR	0x10	RW	Bit[7:0]: cmp_alpha_exp0_gr[7:0]
0x4A36	CMP ALPHA EXP0 R	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp0_r[11:8]
0x4A37	CMP ALPHA EXP0 R	0x10	RW	Bit[7:0]: cmp_alpha_exp0_r[7:0]
0x4A38	CMP ALPHA EXP1 B	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_b[11:8]
0x4A39	CMP ALPHA EXP1 B	0x10	RW	Bit[7:0]: cmp_alpha_exp1_b[7:0]
0x4A3A	CMP ALPHA EXP1 GB	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_gb[11:8]
0x4A3B	CMP ALPHA EXP1 GB	0x10	RW	Bit[7:0]: cmp_alpha_exp1_gb[7:0]
0x4A3C	CMP ALPHA EXP1 GR	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_gr[11:8]
0x4A3D	CMP ALPHA EXP1 GR	0x10	RW	Bit[7:0]: cmp_alpha_exp1_gr[7:0]
0x4A3E	CMP ALPHA EXP1 R	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_alpha_exp1_r[11:8]
0x4A3F	CMP ALPHA EXP1 R	0x10	RW	Bit[7:0]: cmp_alpha_exp1_r[7:0]
0x4A40	CMP BETA EXP0 B	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_b[11:8]

table 6-20 BLC_S registers (sheet 5 of 11)

address	register name	default value	R/W	description
0x4A41	CMP BETA EXP0 B	0x10	RW	Bit[7:0]: cmp_beta_exp0_b[7:0]
0x4A42	CMP BETA EXP0 GB	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_gb[11:8]
0x4A43	CMP BETA EXP0 GB	0x10	RW	Bit[7:0]: cmp_beta_exp0_gb[7:0]
0x4A44	CMP BETA EXP0 GR	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_gr[11:8]
0x4A45	CMP BETA EXP0 GR	0x10	RW	Bit[7:0]: cmp_beta_exp0_gr[7:0]
0x4A46	CMP BETA EXP0 R	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp0_r[11:8]
0x4A47	CMP BETA EXP0 GR	0x10	RW	Bit[7:0]: cmp_beta_exp0_r[7:0]
0x4A48	CMP BETA EXP1 B	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_b[11:8]
0x4A49	CMP BETA EXP1 B	0x10	RW	Bit[7:0]: cmp_beta_exp1_b[7:0]
0x4A4A	CMP BETA EXP1 GB	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_gb[11:8]
0x4A4B	CMP BETA EXP1 GB	0x10	RW	Bit[7:0]: cmp_beta_exp1_gb[7:0]
0x4A4C	CMP BETA EXP1 GR	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_gr[11:8]
0x4A4D	CMP BETA EXP1 GR	0x10	RW	Bit[7:0]: cmp_beta_exp1_gr[7:0]
0x4A4E	CMP BETA EXP1 R	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmp_beta_exp1_r[11:8]
0x4A4F	CMP BETA EXP1 R	0x10	RW	Bit[7:0]: cmp_beta_exp1_r[7:0]
0x4A50	HSIZE	0x00	RW	Bit[7:5]: Reserved Bit[4:0]: Hsize high (IH_SW-8) bits
0x4A51	HSIZE	0x00	RW	Bit[7:0]: Hsize[7:0]
0x4A52	BLC CTRL52	0x02	RW	Bit[7:0]: dc_th1_exp0
0x4A53	BLC CTRL53	0x04	RW	Bit[7:0]: dc_th2_exp0
0x4A54	BLC CTRL54	0x02	RW	Bit[7:0]: dc_th1_exp1
0x4A55	BLC CTRL55	0x04	RW	Bit[7:0]: dc_th2_exp1
0x4A56	BLC CTRL56	0x25	RW	Bit[7:6]: Not used Bit[5:4]: shift_gain Bit[3]: cut_bit Bit[2]: out_bit Bit[1:0]: in_bit

table 6-20 BLC_S registers (sheet 6 of 11)

address	register name	default value	R/W	description
0x4A57	BLC CTRL57	0x20	RW	Bit[7:6]: Reserved Bit[5:0]: Chn
0x4A58~ 0x4A5F	RSVD	–	–	Reserved
0x4A60	OFFSET 0	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_0[9:8]
0x4A61	OFFSET 0	0x00	RW	Bit[7:0]: offset_0[7:0]
0x4A62	OFFSET 1	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_1[9:8]
0x4A63	OFFSET 1	0x00	RW	Bit[7:0]: offset_1[7:0]
0x4A64	OFFSET 2	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_2[9:8]
0x4A65	OFFSET 2	0x00	RW	Bit[7:0]: offset_2[7:0]
0x4A66	OFFSET 3	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_3[9:8]
0x4A67	OFFSET 3	0x00	RW	Bit[7:0]: offset_3[7:0]
0x4A68	OFFSET 4	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_4[9:8]
0x4A69	OFFSET 4	0x00	RW	Bit[7:0]: offset_4[7:0]
0x4A6A	OFFSET 5	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_5[9:8]
0x4A6B	OFFSET 5	0x00	RW	Bit[7:0]: offset_5[7:0]
0x4A6C	OFFSET 6	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_6[9:8]
0x4A6D	OFFSET 6	0x00	RW	Bit[7:0]: offset_6[7:0]
0x4A6E	OFFSET 7	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_7[9:8]
0x4A6F	OFFSET 7	0x00	RW	Bit[7:0]: offset_7[7:0]
0x4A70	OFFSET 8	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_8[9:8]
0x4A71	OFFSET 8	0x00	RW	Bit[7:0]: offset_8[7:0]
0x4A72	OFFSET 9	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_9[9:8]
0x4A73	OFFSET 9	0x00	RW	Bit[7:0]: offset_9[7:0]

table 6-20 BLC_S registers (sheet 7 of 11)

address	register name	default value	R/W	description
0x4A74	OFFSET 10	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_10[9:8]
0x4A75	OFFSET 10	0x00	RW	Bit[7:0]: offset_10[7:0]
0x4A76	OFFSET 11	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_11[9:8]
0x4A77	OFFSET 11	0x00	RW	Bit[7:0]: offset_11[7:0]
0x4A78	OFFSET 12	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_12[9:8]
0x4A79	OFFSET 12	0x00	RW	Bit[7:0]: offset_12[7:0]
0x4A7A	OFFSET 13	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_13[9:8]
0x4A7B	OFFSET 13	0x00	RW	Bit[7:0]: offset_13[7:0]
0x4A7C	OFFSET 14	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_14[9:8]
0x4A7D	OFFSET 14	0x00	RW	Bit[7:0]: offset_14[7:0]
0x4A7E	OFFSET 15	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_15[9:8]
0x4A7F	OFFSET 15	0x00	RW	Bit[7:0]: offset_15[7:0]
0x4A80	OFFSET 16	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_16[9:8]
0x4A81	OFFSET 16	0x00	RW	Bit[7:0]: offset_16[7:0]
0x4A82	OFFSET 17	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_17[9:8]
0x4A83	OFFSET 17	0x00	RW	Bit[7:0]: offset_17[7:0]
0x4A84	OFFSET 18	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_18[9:8]
0x4A85	OFFSET 18	0x00	RW	Bit[7:0]: offset_18[7:0]
0x4A86	OFFSET 19	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_19[9:8]
0x4A87	OFFSET 19	0x00	RW	Bit[7:0]: offset_19[7:0]
0x4A88	OFFSET 20	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_20[9:8]
0x4A89	OFFSET 20	0x00	RW	Bit[7:0]: offset_20[7:0]
0x4A8A	OFFSET 21	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_21[9:8]

table 6-20 BLC_S registers (sheet 8 of 11)

address	register name	default value	R/W	description
0x4A8B	OFFSET 21	0x00	RW	Bit[7:0]: offset_21[7:0]
0x4A8C	OFFSET 22	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_22[9:8]
0x4A8D	OFFSET 22	0x00	RW	Bit[7:0]: offset_22[7:0]
0x4A8E	OFFSET 23	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_23[9:8]
0x4A8F	OFFSET 23	0x00	RW	Bit[7:0]: offset_23[7:0]
0x4A90	OFFSET 24	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_24[9:8]
0x4A91	OFFSET 24	0x00	RW	Bit[7:0]: offset_24[7:0]
0x4A92	OFFSET 25	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_25[9:8]
0x4A93	OFFSET 25	0x00	RW	Bit[7:0]: offset_25[7:0]
0x4A94	OFFSET 26	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_26[9:8]
0x4A95	OFFSET 26	0x00	RW	Bit[7:0]: offset_26[7:0]
0x4A96	OFFSET 27	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_27[9:8]
0x4A97	OFFSET 27	0x00	RW	Bit[7:0]: offset_27[7:0]
0x4A98	OFFSET 28	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_28[9:8]
0x4A99	OFFSET 28	0x00	RW	Bit[7:0]: offset_28[7:0]
0x4A9A	OFFSET 29	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_29[9:8]
0x4A9B	OFFSET 29	0x00	RW	Bit[7:0]: offset_29[7:0]
0x4A9C	OFFSET 30	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_30[9:8]
0x4A9D	OFFSET 30	0x00	RW	Bit[7:0]: offset_30[7:0]
0x4A9E	OFFSET 31	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: offset_31[9:8]
0x4A9F	OFFSET 31	0x00	RW	Bit[7:0]: offset_31[7:0]
0x4AA0	BLC CTRLA0	0x00	RW	Bit[7:0]: sram_base_addr_z_sum
0x4AA1	BLC CTRLA1	0x40	RW	Bit[7:0]: sram_base_addr_z_cnt
0x4AA2	BLC CTRLA2	0x20	RW	Bit[7:0]: sram_base_addr_b_sum

table 6-20 BLC_S registers (sheet 9 of 11)

address	register name	default value	R/W	description
0x4AA3	BLC CTRLA3	0x48	RW	Bit[7:0]: sram_base_addr_b_cnt
0x4AA4	BLC CTRLA4	0x64	RW	Bit[7:0]: sram_base_addr_z_avg
0x4AA5	BLC CTRLA5	0x6C	RW	Bit[7:0]: sram_base_addr_b_avg
0x4AA6	BLC CTRLA6	0xA0	RW	Bit[7:0]: sram_base_addr_pre_offset_a
0x4AA7	BLC CTRLA7	0xA8	RW	Bit[7:0]: sram_base_addr_cur_offset_a
0x4AA8	BLC CTRLA8	0xB0	RW	Bit[7:0]: sram_base_addr_pre_offset_b
0x4AA9	BLC CTRLA9	0xB8	RW	Bit[7:0]: sram_base_addr_cur_offset_b
0x4AAA	BLC CTRLAA	0xC0	RW	Bit[7:0]: sram_base_addr_pre_offset_c
0x4AAB	BLC CTRLAB	0xC8	RW	Bit[7:0]: sram_base_addr_cur_offset_c
0x4AAC	BLC CTRLAC	0x07	RW	Bit[7:0]: b_cal_step_cnt_ch16
0x4AAD	BLC CTRLAB	0x05	RW	Bit[7:0]: b_cal_step_cnt_ch8
0x4AAE	BLC CTRLAE	0x04	RW	Bit[7:0]: b_cal_step_cnt_ch4
0x4AAF	BLC CTRLAF	0x01	RW	Bit[7:0]: z_cal_step_cnt
0x4AB0	BLC CTRLB0	0x64	RW	Bit[7:0]: r_cal_ph_cnt
0x4AB1	BLC CTRLB1	0x28	RW	Bit[7:0]: div_mul_start
0x4AB2	BLC CTRLB2	0x50	RW	Bit[7:0]: div_mul_end
0x4AB3	BLC CTRLB3	0x00	RW	Bit[7:0]: blc_ctrlb3
0x4AB4	BLC CTRLB4	0xD0	RW	Bit[7:0]: sram_base_addr_pre_64_offset_a
0x4AB5	BLC CTRLB4	0xD8	RW	Bit[7:0]: sram_base_addr_pre_64_offset_b
0x4AB6	BLC CTRLB4	0xE0	RW	Bit[7:0]: sram_base_addr_pre_64_offset_c
0x4AB7~ 0x4ABF	RSVD	–	–	Reserved
0x4AC0	BLC TARGET	–	R	Bit[7:6]: Reserved Bit[5:0]: blc_target[13:8]
0x4AC1	BLC TARGET	–	R	Bit[7:0]: blc_target[7:0]
0x4AC2	SRAM CTRL	0x11	RW	Bit[7]: Reserved Bit[6]: sram_test Bit[5:0]: sram_rm[13:8]
0x4AC3	SRAM CTRL	0x30	RW	Bit[7:0]: sram_rm[7:0]
0x4AC4~ 0x4ACF	RSVD	–	–	Reserved
0x4AD0	OFFSET CAL FRAC0	–	R	Bit[7:0]: offset_cal_frac0[7:0]

table 6-20 BLC_S registers (sheet 10 of 11)

address	register name	default value	R/W	description
0x4AD1	OFFSET CAL FRAC1	–	R	Bit[7:0]: offset_cal_frac1[7:0]
0x4AD2	OFFSET CAL FRAC2	–	R	Bit[7:0]: offset_cal_frac2[7:0]
0x4AD3	OFFSET CAL FRAC3	–	R	Bit[7:0]: offset_cal_frac3[7:0]
0x4AD4	OFFSET CAL FRAC4	–	R	Bit[7:0]: offset_cal_frac4[7:0]
0x4AD5	OFFSET CAL FRAC5	–	R	Bit[7:0]: offset_cal_frac5[7:0]
0x4AD6	OFFSET CAL FRAC6	–	R	Bit[7:0]: offset_cal_frac6[7:0]
0x4AD7	OFFSET CAL FRAC7	–	R	Bit[7:0]: offset_cal_frac7[7:0]
0x4AD8	OFFSET CAL FRAC8	–	R	Bit[7:0]: offset_cal_frac8[7:0]
0x4AD9	OFFSET CAL FRAC9	–	R	Bit[7:0]: offset_cal_frac9[7:0]
0x4ADA	OFFSET CAL FRACA	–	R	Bit[7:0]: offset_cal_fraca[7:0]
0x4ADB	OFFSET CAL FRACB	–	R	Bit[7:0]: offset_cal_fracb[7:0]
0x4ADC	OFFSET CAL FRACC	–	R	Bit[7:0]: offset_cal_fracc[7:0]
0x4ADD	OFFSET CAL FRACD	–	R	Bit[7:0]: offset_cal_fracd[7:0]
0x4ADE	OFFSET CAL FRACE	–	R	Bit[7:0]: offset_cal_frace[7:0]
0x4ADF	OFFSET CAL FRACF	–	R	Bit[7:0]: offset_cal_fracf[7:0]
0x4AE0	OFFSET CAL FRAC10	–	R	Bit[7:0]: offset_cal_frac10[7:0]
0x4AE1	OFFSET CAL FRAC11	–	R	Bit[7:0]: offset_cal_frac11[7:0]
0x4AE2	OFFSET CAL FRAC12	–	R	Bit[7:0]: offset_cal_frac12[7:0]
0x4AE3	OFFSET CAL FRAC13	–	R	Bit[7:0]: offset_cal_frac13[7:0]
0x4AE4	OFFSET CAL FRAC14	–	R	Bit[7:0]: offset_cal_frac14[7:0]
0x4AE5	OFFSET CAL FRAC15	–	R	Bit[7:0]: offset_cal_frac15[7:0]
0x4AE6	OFFSET CAL FRAC16	–	R	Bit[7:0]: offset_cal_frac16[7:0]
0x4AE7	OFFSET CAL FRAC17	–	R	Bit[7:0]: offset_cal_frac17[7:0]
0x4AE8	OFFSET CAL FRAC18	–	R	Bit[7:0]: offset_cal_frac18[7:0]
0x4AE9	OFFSET CAL FRAC19	–	R	Bit[7:0]: offset_cal_frac19[7:0]
0x4AEA	OFFSET CAL FRAC1A	–	R	Bit[7:0]: offset_cal_frac1a[7:0]
0x4AEB	OFFSET CAL FRAC1B	–	R	Bit[7:0]: offset_cal_frac1b[7:0]
0x4AEC	OFFSET CAL FRAC1C	–	R	Bit[7:0]: offset_cal_frac1c[7:0]
0x4AED	OFFSET CAL FRAC1D	–	R	Bit[7:0]: offset_cal_frac1d[7:0]
0x4AEE	OFFSET CAL FRAC1E	–	R	Bit[7:0]: offset_cal_frac1e[7:0]

table 6-20 BLC_S registers (sheet 11 of 11)

address	register name	default value	R/W	description
0x4AEF	OFFSET CAL FRAC1F	–	R	Bit[7:0]: offset_cal_frac1f[7:0]

6.21 FC [0x4200 - 0x4203]

table 6-21 FC registers

address	register name	default value	R/W	description
0x4200	FC_0	0x06	RW	Bit[7:4]: Not used Bit[3]: sof_after_line0 Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fc_rst
0x4201	FC_1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_on_no
0x4202	FC_2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_off_no
0x4203	FC_3	0x81	RW	Bit[7]: zero_line_mask_dis Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.22 ISP_FC [0x4220 - 0x4223]

table 6-22 ISP_FC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4220	FC_0	0x06	RW	Bit[7:4]: Reserved Bit[3]: sof_after_line0 Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fc_rst

table 6-22 ISP_FC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4221	FC_1	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: frame_on_no
0x4222	FC_2	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: frame_off_no
0x4223	FC_3	0x81	RW	Bit[7]: zero_line_mask_dis Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis

6.23 window [0x4280 - 0x429B]

table 6-23 window registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4280	WINDOW_D4V2_V10_0	0x00	RW	Bit[7:0]: Manual window horizontal start point[15:8]
0x4281	WINDOW_D4V2_V10_1	0x00	RW	Bit[7:0]: Manual window horizontal start point[7:0]
0x4282	WINDOW_D4V2_V10_2	0x00	RW	Bit[7:0]: Manual window vertical start point[15:8]
0x4283	WINDOW_D4V2_V10_3	0x00	RW	Bit[7:0]: Manual window vertical start point[7:0]
0x4284	WINDOW_D4V2_V10_4	0x00	RW	Bit[7:0]: Manual window horizontal size[15:8]
0x4285	WINDOW_D4V2_V10_5	0x00	RW	Bit[7:0]: Manual window horizontal size[7:0]
0x4286	WINDOW_D4V2_V10_6	0x00	RW	Bit[7:0]: Manual window vertical size[15:8]
0x4287	WINDOW_D4V2_V10_7	0x00	RW	Bit[7:0]: Manual window vertical size[7:0]
0x4288	WINDOW_D4V2_V10_8	0x07	RW	Bit[7:6]: eof_o options Bit[5:4]: sof_o options Bit[3]: Window manual mode enable Bit[2]: hwin_en Bit[1]: vwin_en Bit[0]: Window enable

table 6-23 window registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4289	WINDOW_D4V2_V10_9	0x00	RW	Bit[7:6]: emb_eof_sel Bit[5]: emb_eof_auto Bit[4]: vblk_req_dummy_sof_en Bit[3]: vblk_req_dummy_eof_en Bit[2]: blk_out_en Bit[1:0]: dummy_seof_sel
0x428A	WINDOW_D4V2_V10_10	0x00	RW	Bit[7:0]: dummy_pos[15:8]
0x428B	WINDOW_D4V2_V10_11	0x0A	RW	Bit[7:0]: dummy_pos[7:0]
0x428C	WINDOW_D4V2_V10_12	0x80	RW	Bit[7:0]: emb_eof_pos[15:8]
0x428D	WINDOW_D4V2_V10_13	0x00	RW	Bit[7:0]: emb_eof_pos[7:0]
0x428E	WINDOW_D4V2_V10_14	0x00	RW	Bit[7:0]: eof_pos[7:0]
0x428F	WINDOW_D4V2_V10_15	0x00	RW	Bit[7:1]: Not used Bit[0]: cnt_rd_latch_en
0x4290	WINDOW_D4V2_V10_16	–	R	Bit[7:0]: L window horizontal input size[15:8]
0x4291	WINDOW_D4V2_V10_17	–	R	Bit[7:0]: L window horizontal input size[7:0]
0x4292	WINDOW_D4V2_V10_18	–	R	Bit[7:0]: L window vertical input size[15:8]
0x4293	WINDOW_D4V2_V10_19	–	R	Bit[7:0]: L window vertical input size[7:0]
0x4294	WINDOW_D4V2_V10_20	–	R	Bit[7:0]: hcnt_m[15:8]
0x4295	WINDOW_D4V2_V10_21	–	R	Bit[7:0]: hcnt_m[7:0]
0x4296	WINDOW_D4V2_V10_22	–	R	Bit[7:0]: vcnt_m[15:8]
0x4297	WINDOW_D4V2_V10_23	–	R	Bit[7:0]: vcnt_m[7:0]
0x4298	WINDOW_D4V2_V10_24	–	R	Bit[7:0]: hcnt_s[15:8]
0x4299	WINDOW_D4V2_V10_25	–	R	Bit[7:0]: hcnt_s[7:0]
0x429A	WINDOW_D4V2_V10_26	–	R	Bit[7:0]: vcnt_s[15:8]
0x429B	WINDOW_D4V2_V10_27	–	R	Bit[7:0]: vcnt_s[7:0]

6.24 TEST_MODE [0x4300 - 0x4314]

table 6-24 TEST_MODE registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4300	TEST B	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_b[11:8]
0x4301	TEST B	0x00	RW	Bit[7:0]: test_b[7:0]
0x4302	TEST GB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_gb[11:8]
0x4303	TEST GB	0x00	RW	Bit[7:0]: test_gb[7:0]
0x4304	TEST GR	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_gr[11:8]
0x4305	TEST GR	0x00	RW	Bit[7:0]: test_gr[7:0]
0x4306	TEST R	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_r[11:8]
0x4307	TEST R	0x00	RW	Bit[7:0]: test_r[7:0]
0x4308	TEST MODE	0x00	RW	Bit[7:6]: Not used Bit[5:3]: r_bit_swap Bit[2]: r_pn9_bit_rev Bit[1]: pn9_en Bit[0]: fix_color_en
0x4309	TEST W	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_w[11:8]
0x430A	TEST W	0x00	RW	Bit[7:0]: test_w[7:0]
0x430B	CLIP MAX HI	0xFF	RW	Bit[7:0]: clip_max_hi[7:0]
0x430C	CLIP MAX LO	0xFF	RW	Bit[7:0]: clip_max_lo[7:0]
0x430D	CLIP MIN HI	0x00	RW	Bit[7:0]: clip_min_hi[7:0]
0x430E	CLIP MIN LO	0x00	RW	Bit[7:0]: clip_min_lo[7:0]
0x430F	PN31 CTRL	0x02	RW	Bit[7:3]: Reserved Bit[2]: r_pn31_lsb_first Bit[1]: r_pn31_sof_rst_en Bit[0]: r_pn31_href_rst_en
0x4310	CLIP MAX HI 16	0xFF	RW	Bit[7:0]: clip_max_hi_16[7:0]
0x4311	CLIP MAX LO 16	0xFF	RW	Bit[7:0]: clip_max_lo_16[7:0]
0x4312	CLIP MIN HI 16	0x00	RW	Bit[7:0]: clip_min_hi_16[7:0]
0x4313	CLIP MIN LO 16	0x00	RW	Bit[7:0]: clip_min_lo_16[7:0]

table 6-24 TEST_MODE registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4314	R BIT SWAP 12 DIS	0x04	RW	Bit[7:2]: Reserved Bit[1:0]: r_bit_swap_16[1:0]

6.25 DATA_SYNC [0x4500 - 0x4547]

table 6-25 DATA_SYNC registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x4500	DATA_SYNC_0	0x02	RW	Bit[7:0]: fifo_rdly
0x4501	DATA_SYNC_1	0x00	RW	Bit[7:4]: Not used Bit[3]: bitline_shift_up_sel 0: Auto 1: Manual Bit[2]: bitline_shift_up Bit[1]: srclk1_inv Bit[0]: srclk0_inv
0x4502	DATA_SYNC_2	0x00	RW	Bit[7:0]: Offset
0x4503	DATA_SYNC_3	0x0F	RW	Bit[7]: vskip4_od Bit[6:4]: hskip_odd_pixel Bit[3]: vbin4_avg Bit[2:0]: hbin_avg
0x4504	DATA_SYNC_4	0x00	RW	Bit[7]: fifo_rdly_manu Bit[6]: sub_gate_dis Bit[5:4]: Not used Bit[3]: dig_hsub2_af_sfifo Bit[2]: dig_hbin2_af_sfifo Bit[1]: dig_avg_after_sync_fifo Bit[0]: dig_skip_od_after_sync_fifo
0x4505	DATA_SYNC_5	0x00	RW	Bit[7:0]: Reserved for data_sync
0x4506	DATA_SYNC_6	0x00	RW	Bit[7]: sync_fifo_mode_man_en Bit[6:4]: sync_fifo_mode_man Bit[3]: sync_fifo_flip_man_en Bit[2]: sync_fifo_flip_man Bit[1]: sync_fifo_srclk_gt_dis Bit[0]: sync_fifo_sof_rst_en

table 6-25 DATA_SYNC registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x4507	DATA_SYNC_7	0x00	RW	Bit[7]: sync_fifo_tx_swap_man_en Bit[6:5]: tx_swap_man_01 Bit[4:3]: tx_swap_man_23 Bit[2]: Reserved Bit[1]: sync_fifo_bist_clk_sel Bit[0]: tx_man_en
0x4508	DATA_SYNC_8	0x00	RW	Bit[7:0]: tx_man
0x4509	DATA_SYNC_9	0x05	RW	Bit[7]: hdr_4c_1111_href_opt Bit[6]: hdr_4c_cg_mode Bit[5:4]: href_out_opt Bit[3]: Not used Bit[2]: vref_lat_en Bit[1]: vref_align_w_l Bit[0]: hs_rd
0x450A	DATA_SYNC_10	0x08	RW	Bit[7:0]: srf_man
0x450B	DATA_SYNC_11	0x00	RW	Bit[7]: buf_half_0_en_man Bit[6]: buf_half_0_en Bit[5]: buf_0_num_man_en Bit[4:0]: buf_0_num_man
0x450C	DATA_SYNC_12	0x00	RW	Bit[7]: vblk_href_out_en Bit[6]: half_0_offset_man_en Bit[5:4]: half_0_offset_man Bit[3]: stg_dmy_rw_mask Bit[2]: half_1_offset_man_en Bit[1:0]: half_1_offset_man
0x450D	DATA_SYNC_13	0x20	RW	Bit[7:6]: Not used Bit[5:0]: two_pipe_padding_num
0x450E	DATA_SYNC_14	0x00	RW	Bit[7:0]: href_gap[15:8]
0x450F	DATA_SYNC_15	0x20	RW	Bit[7:0]: href_gap[7:0]
0x4510	DATA_SYNC_16	0x00	RW	Bit[7]: Served10 Bit[6]: Separate even/odd row flag Bit[5]: href_rise_opt 0: Early HREF (default) 1: Low HREF Bit[4]: Treat 4C as Bayer Bit[3]: merge_col Bit[2]: hdr_man_en Bit[1]: color_man_en Bit[0]: chn_man_en

table 6-25 DATA_SYNC registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x4511	DATA_SYNC_17	0x00	RW	Bit[7]: ch_inc_man_en Bit[6:4]: ch_inc_man Bit[3]: ch_man_opt Bit[2]: bin_2c_hdr_flag_opt Bit[1]: merge_bl01 Bit[0]: ln_02_merge
0x4512	DATA_SYNC_18	0x00	RW	Bit[7:0]: blc_chn_man_01_0
0x4513	DATA_SYNC_19	0x00	RW	Bit[7:0]: blc_chn_man_01_1
0x4514	DATA_SYNC_20	0x00	RW	Bit[7:0]: blc_chn_man_23_0
0x4515	DATA_SYNC_21	0x00	RW	Bit[7:0]: blc_chn_man_23_1
0x4516	DATA_SYNC_22	0x00	RW	Bit[7:0]: blc_chn_man_45_0
0x4517	DATA_SYNC_23	0x00	RW	Bit[7:0]: blc_chn_man_45_1
0x4518	DATA_SYNC_24	0x00	RW	Bit[7:0]: blc_chn_man_67_0
0x4519	DATA_SYNC_25	0x00	RW	Bit[7:0]: blc_chn_man_67_1
0x451A	DATA_SYNC_26	0x00	RW	Bit[7:0]: blc_color_man01_0
0x451B	DATA_SYNC_27	0x00	RW	Bit[7:0]: blc_color_man01_1
0x451C	DATA_SYNC_28	0x00	RW	Bit[7:0]: blc_color_man23_0
0x451D	DATA_SYNC_29	0x00	RW	Bit[7:0]: blc_color_man23_1
0x451E	DATA_SYNC_30	0x00	RW	Bit[7:0]: blc_color_man45_0
0x451F	DATA_SYNC_31	0x00	RW	Bit[7:0]: blc_color_man45_1
0x4520	DATA_SYNC_32	0x00	RW	Bit[7:0]: blc_color_man67_0
0x4521	DATA_SYNC_33	0x00	RW	Bit[7:0]: blc_color_man67_1
0x4522	DATA_SYNC_34	0x00	RW	Bit[7:4]: blc_hdr_man01_0 Bit[3:0]: blc_hdr_man01_1
0x4523	DATA_SYNC_35	0x00	RW	Bit[7:4]: blc_hdr_man23_0 Bit[3:0]: blc_hdr_man23_1
0x4524	DATA_SYNC_36	0x00	RW	Bit[7:4]: blc_hdr_man45_0 Bit[3:0]: blc_hdr_man45_1
0x4525	DATA_SYNC_37	0x00	RW	Bit[7:4]: blc_hdr_man67_0 Bit[3:0]: blc_hdr_man67_1
0x4526	DATA_SYNC_38	0x00	RW	Bit[7:0]: Served26
0x4527	DATA_SYNC_39	0x18	RW	Bit[7:0]: vref_lat_thresh
0x4528~ 0x453F	RSVD	–	–	Reserved

table 6-25 DATA_SYNC registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x4540	DATA_SYNC_64	0x11	RW	Bit[7:0]: sram_ctrl[15:8]
0x4541	DATA_SYNC_65	0x30	RW	Bit[7:0]: sram_ctrl[7:0]
0x4542	DATA_SYNC_66	0x00	RW	Bit[7:4]: out_st_man Bit[3]: Not used Bit[2]: out_st_man_en Bit[1]: stg3_man_en Bit[0]: stg2_man_en
0x4543	DATA_SYNC_67	0x00	RW	Bit[7]: Not used Bit[6:5]: wr_m_remap Bit[4]: wr_m_remap_en Bit[3]: Not used Bit[2:1]: wr_l_remap Bit[0]: wr_l_remap_en
0x4544	DATA_SYNC_68	0x00	RW	Bit[7:5]: Not used Bit[4]: stg2_2c_mask Bit[3]: stg3_2c_mask Bit[2:1]: wr_s_remap Bit[0]: wr_s_remap_en
0x4545	DATA_SYNC_69	0x00	RW	Bit[7:4]: Not used Bit[3]: href_dly_out_en Bit[2]: ln_shift_sel Bit[1]: ln_shift_even_flag_sel Bit[0]: expo3_cnt_opt
0x4546	DATA_SYNC_70	0x00	RW	Bit[7:0]: href_dly_out_num[15:8]
0x4547	DATA_SYNC_71	0x00	RW	Bit[7:0]: href_dly_out_num[7:0]

6.26 LR_PIPE_STITCH [0x4580 - 0x458B]

table 6-26 LR_PIPE_STITCH registers

address	register name	default value	R/W	description
0x4580	LR_PIPE_STITCH_0	0x00	RW	Bit[7]: Bypass if there is only left or right image Bit[6]: Valid mask enable Bit[5]: D2V2 output enable Bit[4]: Left horizontal size manual enable Bit[3]: Right horizontal size manual enable Bit[2]: Frame reset enable Bit[1]: Boundary pixel manual enable Bit[0]: Module enable
0x4581	LR_PIPE_STITCH_1	0x40	RW	Bit[7:0]: Boundary pixel manual value[7:0]
0x4582	LR_PIPE_STITCH_2	0x04	RW	Bit[7:4]: Not used Bit[3]: Clock gating disable Bit[2]: SRAM always enable Bit[1]: Debug mode enable Bit[0]: SRAM start size manual enable
0x4583	LR_PIPE_STITCH_3	0x00	RW	Bit[7:0]: Manual left horizontal size[15:8]
0x4584	LR_PIPE_STITCH_4	0x00	RW	Bit[7:0]: Manual left horizontal size[7:0]
0x4585	LR_PIPE_STITCH_5	0x00	RW	Bit[7:0]: Manual right horizontal size[15:8]
0x4586	LR_PIPE_STITCH_6	0x00	RW	Bit[7:0]: Manual right horizontal size[7:0]
0x4587	LR_PIPE_STITCH_7	0x00	RW	Bit[7:0]: Manual read start size[15:8]
0x4588	LR_PIPE_STITCH_8	0x00	RW	Bit[7:0]: Manual read start size[7:0]
0x4589	LR_PIPE_STITCH_9	0x11	RW	Bit[7:0]: SRAM control[15:8]
0x458A	LR_PIPE_STITCH_10	0x30	RW	Bit[7:0]: SRAM control[7:0]
0x458B	LR_PIPE_STITCH_11	0xFF	RW	Bit[7:4]: Valid mask for left Bit[3:0]: Valid mask for right

6.27 LR_PD_STITCH [0x45C0 - 0x45CB]

table 6-27 LR_PD_STITCH registers

address	register name	default value	R/W	description
0x45C0	LR_PD_STITCH_0	0x00	RW	Bit[7]: Bypass if there is only left or right image Bit[6]: Valid mask enable Bit[5]: D2V2 output enable Bit[4]: Left horizontal size manual enable Bit[3]: Right horizontal size manual enable Bit[2]: Frame reset enable Bit[1]: Boundary pixel manual enable Bit[0]: Module enable
0x45C1	LR_PD_STITCH_1	0x40	RW	Bit[7:0]: Boundary pixel manual value[7:0]
0x45C2	LR_PD_STITCH_2	0x04	RW	Bit[7:4]: Not used Bit[3]: Clock gating disable Bit[2]: SRAM always enable Bit[1]: Debug mode enable Bit[0]: SRAM start size manual enable
0x45C3	LR_PD_STITCH_3	0x00	RW	Bit[7:0]: Manual left horizontal size[15:8]
0x45C4	LR_PD_STITCH_4	0x00	RW	Bit[7:0]: Manual left horizontal size[7:0]
0x45C5	LR_PD_STITCH_5	0x00	RW	Bit[7:0]: Manual right horizontal size[15:8]
0x45C6	LR_PD_STITCH_6	0x00	RW	Bit[7:0]: Manual right horizontal size[7:0]
0x45C7	LR_PD_STITCH_7	0x00	RW	Bit[7:0]: Manual read start size[15:8]
0x45C8	LR_PD_STITCH_8	0x00	RW	Bit[7:0]: Manual read start size[7:0]
0x45C9	LR_PD_STITCH_9	0x11	RW	Bit[7:0]: SRAM control[15:8]
0x45CA	LR_PD_STITCH_10	0x30	RW	Bit[7:0]: SRAM control[7:0]
0x45CB	LR_PD_STITCH_11	0xFF	RW	Bit[7:4]: Valid mask for left Bit[3:0]: Valid mask for right

6.28 VFIFO [0x4600 - 0x460D]

table 6-28 VFIFO registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4600	VFIFO_30_0	0x01	RW	Bit[7:0]: RAM output start size[15:8]
0x4601	VFIFO_30_1	0x00	RW	Bit[7:0]: RAM output start size[7:0]
0x4602	VFIFO_30_2	0x00	RW	Bit[7:4]: Start address adjustment Bit[3]: SOF clear disable Bit[2]: BIST selection Bit[1]: SRAM high frequency mode enable Bit[0]: RAM bypass
0x4603	VFIFO_30_3	0x11	RW	Bit[7]: FO mirror 4x fix disable Bit[6]: RAM mirror disable Bit[5]: FI mirror swap disable Bit[4]: Frame reset enable Bit[3]: RAM output start at fixed size Bit[2]: Line gap manual mode enable Bit[1]: Start manual mode enable Bit[0]: FO read write condition enable
0x4604	VFIFO_30_4	0x00	RW	Bit[7:4]: Hblank adjustment Bit[3:0]: Ready low count
0x4605	RSVD	–	–	Reserved
0x4606	VFIFO_30_6	0x11	RW	Bit[7:0]: SRAM BIST RM[15:8]
0x4607	VFIFO_30_7	0x30	RW	Bit[7:0]: SRAM BIST RM[7:0]
0x4608	VFIFO_30_8	0x00	RW	Bit[7:0]: Manual line gap[15:8]
0x4609	VFIFO_30_9	0x04	RW	Bit[7:0]: Manual line gap[7:0]
0x460A	VFIFO_30_10	–	R	Bit[7:5]: Not used Bit[4]: fo_underflow This register can only be manually cleared Bit[3]: SRAM1 overflow This register can only be manually cleared Bit[2]: SRAM0 overflow This register can only be manually cleared Bit[1]: SRAM1 underflow This register can only be manually cleared Bit[0]: SRAM0 underflow This register can only be manually cleared

table 6-28 VFIFO registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x460B	VFIFO_30_11	0x03	RW	Bit[7:2]: Not used Bit[1]: Option to optimize SRAM utilization in mirror mode Bit[0]: sof_clr_line_en
0x460C	VFIFO_30_12	–	W	Bit[7:5]: Not used Bit[4]: Clear fo_underflow flag Bit[3]: Clear SRAM1 overflow flag Bit[2]: Clear SRAM0 overflow flag Bit[1]: Clear SRAM1 underflow flag Bit[0]: Clear SRAM0 underflow flag
0x460D	VFIFO_30_13	0x00	RW	Bit[7:1]: Not used Bit[0]: stat_sof_rst_en

6.29 PD_FIFO control [0x4640 - 0x464F]

table 6-29 PD_FIFO registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4640	VFIFO_40_0	0x00	RW	Bit[7:0]: start size[15:8]
0x4641	VFIFO_40_1	0x30	RW	Bit[7:0]: start size[7:0]
0x4642	VFIFO_40_2	0x42	RW	Bit[7:4]: min_packet_size Bit[3]: Not used Bit[2:0]: fo_rdy_threshold
0x4643	VFIFO_40_3	0x00	RW	Bit[7:4]: start_opt[3:0] Bit[3]: For pd_mode Bit[2]: d2v1_mode Bit[1]: hsize_man_en Bit[0]: man_start_mode
0x4644	VFIFO_40_4	0x40	RW	Bit[7]: sram_dy_st_mask_en Bit[6]: rd_index_init_sof_reset_delay_en Bit[5]: always_fix_packet_size Bit[4]: sof_clr_dis Bit[3]: default_sram1 Bit[2]: r_fo_miff_4x_fix_dis Bit[1]: vfifo_mirror_dis Bit[0]: mirr_fi_swap_dis

table 6-29 PD_FIFO registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4645	VFIFO_40_5	0xB3	RW	Bit[7]: fifo_data_cnt_adj_en Bit[6]: pd_pkt_size_eq_in_hsize Bit[5]: eof_trig_chk_sram_empty_en Bit[4]: pd_mode_en Bit[3:0]: rdy_low[3:0]
0x4646	VFIFO_40_6	–	R	Bit[7:4]: Not used Bit[3]: rg_ram_full Bit[2]: rg_ram_empty Bit[1]: rg_fofull Bit[0]: rg_foempty
0x4647	VFIFO_40_7	0x02	RW	Bit[7:4]: Not used Bit[3:0]: sram_full_margin
0x4648	VFIFO_40_8	0x11	RW	Bit[7:0]: sram_ctrl[15:8]
0x4649	VFIFO_40_9	0x30	RW	Bit[7:0]: sram_ctrl[7:0]
0x464A	VFIFO_40_10	0x00	RW	Bit[7:0]: hsize_man[15:8]
0x464B	VFIFO_40_11	0x00	RW	Bit[7:0]: hsize_man[7:0]
0x464C	VFIFO_40_12	0x01	RW	Bit[7:3]: Not used Bit[2]: manual_swap Bit[1]: manual_swap_en Bit[0]: dummy_data_filter_en
0x464D~ 0x464E	NOT USED	–	–	Not Used
0x464F	VFIFO_40_15	–	R	Bit[7:1]: Not used Bit[0]: ddf_overflow

6.30 MIPI_CORE [0x4800 - 0x487A, 0x48C0 - 0x48C5]

table 6-30 MIPI_CORE registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x4800	MIPI_CORE_0	0x04	RW	Bit[7]: Select sc_valid Bit[6]: Enable vertical clock gating Bit[5]: Enable clock gating Bit[4]: Enable line sync Bit[3]: Not used Bit[2]: Invert output PCLK Bit[1]: first_bit 0: Not used 1: First bit is 1 Bit[0]: lpx_p_sel Select manual parameter or auto parameter
0x4801	NOT USED	–	–	Not Used
0x4802	MIPI_CORE_2	0x00	RW	Bit[7]: hs_prepare_sel Select manual parameter or auto parameter Bit[6]: clk_prepare_sel Select manual parameter or auto parameter Bit[5]: clk_post_sel Select manual parameter or auto parameter Bit[4]: clk_trail_sel Select manual parameter or auto parameter Bit[3]: hs_exit_sel Select manual parameter or auto parameter Bit[2]: hs_zero_sel Select manual parameter or auto parameter Bit[1]: hs_trail_sel Select manual parameter or auto parameter Bit[0]: clk_zero_sel Select manual parameter or auto parameter
0x4803	MIPI_CORE_3	0x00	RW	Bit[7]: test_en Bit[6:1]: Not used Bit[0]: dphy_test_escape_en
0x4804	MIPI_CORE_4	0xB6	RW	Bit[7:0]: mipi_phy_test_pattern[15:8]

table 6-30 MIPI_CORE registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x4805	MIPI_CORE_5	0x20	RW	Bit[7:6]: Not used Bit[5:4]: Option for pre-sleep Bit[3:0]: Retiming
0x4806	MIPI_CORE_6	0x40	RW	Bit[7:6]: clk_data_pattern Bit[5]: clk_trail_data Bit[4]: Enable power up mark Bit[3]: Remote reset Bit[2]: Suspend Bit[1]: Enable SMIA lane Bit[0]: Output TXLSB first
0x4807	MIPI_CORE_7	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Ultra low power mode state delay[3:0]
0x4808	MIPI_CORE_8	0x18	RW	Bit[7:0]: Wakeup delay[7:0]
0x4809	MIPI_CORE_9	0x4C	RW	Bit[7]: Manual control enable for lptx_pd_mode_sl Bit[6]: lptx_pd_mode_man Bit[5:0]: lptx_pd_ovlap
0x480A	MIPI_CORE_10	0x2A	RW	Bit[7]: pkt_bit14_opt Bit[6]: frame_blk_out_opt Bit[5]: pre_sleep_opt Bit[4:2]: Reserved Bit[1]: line_act_enable Bit[0]: wc_sel_opt
0x480B	MIPI_CORE_11	0x10	RW	Bit[7]: lane1_pn_swap Bit[6:4]: lane1_swap Bit[3]: lane0_pn_swap Bit[2:0]: lane0_swap
0x480C	MIPI_CORE_12	0x80	RW	Bit[7:5]: clk_lane_swap Bit[4]: lane_num_man_en Bit[3:0]: lane_num_man
0x480D	MIPI_CORE_13	0xB6	RW	Bit[7:0]: mipi_phy_test_pattern[7:0]
0x480E	MIPI_CORE_14	0x00	RW	Bit[7]: ring_cnt_err_opt_o Bit[6]: clk_lane_pn_swap Bit[5:4]: frm_end_time_opt Bit[3]: Not used Bit[2]: Enable img2 Bit[1:0]: Reserved
0x480F	MIPI_CORE_15	0x32	RW	Bit[7]: lane3_pn_swap Bit[6:4]: lane3_swap Bit[3]: lane2_pn_swap Bit[2:0]: lane2_swap
0x4810	MIPI_CORE_16	0xFF	RW	Bit[7:0]: Max frame count value[15:8]

table 6-30 MIPI_CORE registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x4811	MIPI_CORE_17	0xFF	RW	Bit[7:0]: Max frame count value[7:0]
0x4812	MIPI_CORE_18	0x12	RW	Bit[7:6]: Not used Bit[5:0]: emb_dt[5:0]
0x4813	MIPI_CORE_19	0x10	RW	Bit[7:4]: Virtual channel ID Bit[3:0]: Virtual channel ID
0x4814	MIPI_CORE_20	0x2A	RW	Bit[7]: Not used Bit[6]: Data type select Bit[5:0]: Data type[5:0]
0x4815	MIPI_CORE_21	0x2B	RW	Bit[7:6]: Not used Bit[5:0]: Data type[5:0]
0x4816	MIPI_CORE_22	0x2B	RW	Bit[7:6]: Not used Bit[5:0]: Data type[5:0]
0x4817	MIPI_CORE_23	0x00	RW	Bit[7:6]: fcnt_sel Bit[5:4]: lcnt_sel Bit[3:2]: frame_act_sel Bit[1:0]: last_sel
0x4818	MIPI_CORE_24	0x00	RW	Bit[7:2]: Not used Bit[1:0]: MIPI parameter value[9:8]
0x4819	MIPI_CORE_25	0x70	RW	Bit[7:0]: MIPI parameter value[7:0]
0x481A	MIPI_CORE_26	0x00	RW	Bit[7:2]: Not used Bit[1:0]: MIPI parameter value[9:8]
0x481B	MIPI_CORE_27	0x3C	RW	Bit[7:0]: MIPI parameter value[7:0]
0x481C	MIPI_CORE_28	0x01	RW	Bit[7:2]: Not used Bit[1:0]: MIPI parameter value[9:8]
0x481D	MIPI_CORE_29	0x2C	RW	Bit[7:0]: MIPI parameter value[7:0]
0x481E	MIPI_CORE_30	0x5F	RW	Bit[7:0]: MIPI parameter value[7:0]
0x481F	MIPI_CORE_31	0x26	RW	Bit[7:0]: MIPI parameter value[7:0]
0x4820	MIPI_CORE_32	0x00	RW	Bit[7:2]: Not used Bit[1:0]: MIPI parameter value[9:8]
0x4821	MIPI_CORE_33	0x3C	RW	Bit[7:0]: MIPI parameter value[7:0]
0x4822	MIPI_CORE_34	0x00	RW	Bit[7:2]: Not used Bit[1:0]: MIPI parameter value[9:8]
0x4823	MIPI_CORE_35	0x3C	RW	Bit[7:0]: MIPI parameter value[7:0]
0x4824	MIPI_CORE_36	0x00	RW	Bit[7:2]: Not used Bit[1:0]: MIPI parameter value[9:8]
0x4825	MIPI_CORE_37	0x32	RW	Bit[7:0]: MIPI parameter value[7:0]

table 6-30 MIPI_CORE registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x4826	MIPI_CORE_38	0x32	RW	Bit[7:0]: MIPI parameter value[7:0]
0x4827	MIPI_CORE_39	0x55	RW	Bit[7:0]: MIPI parameter value[7:0]
0x4828	MIPI_CORE_40	0x00	RW	Bit[7:2]: Not used Bit[1:0]: MIPI parameter value[9:8]
0x4829	MIPI_CORE_41	0x64	RW	Bit[7:0]: MIPI parameter value[7:0]
0x482A	MIPI_CORE_42	0x06	RW	Bit[7:6]: Not used Bit[5:0]: MIPI parameter value[5:0]
0x482B	MIPI_CORE_43	0x04	RW	Bit[7:6]: Reserved Bit[5:0]: MIPI parameter value[5:0]
0x482C	MIPI_CORE_44	0x00	RW	Bit[7:6]: Not used Bit[5:0]: MIPI parameter value[5:0]
0x482D	MIPI_CORE_45	0x00	RW	Bit[7:4]: MIPI parameter value[3:0] Bit[3:0]: MIPI parameter value[3:0]
0x482E	MIPI_CORE_46	0x34	RW	Bit[7:6]: Not used Bit[5:0]: MIPI parameter value[5:0]
0x482F	MIPI_CORE_47	0x00	RW	Bit[7:6]: Not used Bit[5:0]: MIPI parameter value[5:0]
0x4830	MIPI_CORE_48	0x00	RW	Bit[7:6]: Not used Bit[5:0]: MIPI parameter value
0x4831	MIPI_CORE_49	0x64	RW	Bit[7:4]: MIPI parameter value[3:0] Bit[3:0]: MIPI parameter value[3:0]
0x4832	MIPI_CORE_50	0x00	RW	Bit[7:6]: Not used Bit[5:0]: MIPI parameter value[5:0]
0x4833	MIPI_CORE_51	0x30	RW	Bit[7]: Not used Bit[6:0]: Packet FIFO ready mark[6:0]
0x4834	MIPI_CORE_52	0x01	RW	Bit[7]: Not used Bit[6]: dphy_preamble_en Bit[5:0]: t_dphy_preamble[5:0]
0x4835	MIPI_CORE_53	0x55	RW	Bit[7:0]: dphy_preamble_data
0x4836	MIPI_CORE_54	0x32	RW	Bit[7:4]: VC3 Bit[3:0]: VC2
0x4837	MIPI_CORE_55	0x0E	RW	Bit[7:0]: MIPI PCLK period[7:0] Should be changed when PCLK frequency changes

table 6-30 MIPI_CORE registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x4838	MIPI_CORE_56	0x00	RW	Bit[7]: Low power select for lane0 Bit[6]: Low power direction for lane0 Bit[5]: LP p0 for lane0 Bit[4]: LP n0 for lane0 Bit[3]: Low power select for lane1 Bit[2]: Low power direction for lane1 Bit[1]: LP p0 for lane1 Bit[0]: LP n0 for lane1
0x4839	MIPI_CORE_57	0x00	RW	Bit[7]: Low power select for lane2 Bit[6]: Low power direction for lane2 Bit[5]: LP p0 for lane2 Bit[4]: LP n0 for lane2 Bit[3]: Low power select for lane3 Bit[2]: Low power direction for lane3 Bit[1]: LP p0 for lane3 Bit[0]: LP n0 for lane0
0x483A~ 0x483B	NOT USED	–	–	Not Used
0x483C	MIPI_CORE_60	0x10	RW	Bit[7:0]: MIPI parameter value[7:0]
0x483D	MIPI_CORE_61	0x00	RW	Bit[7:4]: Not used Bit[3]: Low power select for clock lane Bit[2]: Not used Bit[1]: LP clock lane p Bit[0]: LP clock lane n
0x483E	MIPI_CORE_62	–	R	Bit[7:0]: Frame count value[15:8]
0x483F	MIPI_CORE_63	–	R	Bit[7:0]: Frame count value[7:0]
0x4840~ 0x4847	NOT USED	–	–	Not Used
0x4848	MIPI_CORE_72	0xB6	RW	Bit[7:0]: mipi_phy_test_pattern2[15:8]
0x4849	MIPI_CORE_73	0xB6	RW	Bit[7:0]: mipi_phy_test_pattern2[7:0]
0x484A	MIPI_CORE_74	0x3F	RW	Bit[7:6]: Not used Bit[5]: Sleep power down select Bit[4]: lp_pon data Bit[3]: lp_pon clock lane data Bit[2]: Manual sleep state Bit[1]: Clock lane sleep state Bit[0]: Data lane sleep state

table 6-30 MIPI_CORE registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x484B	MIPI_CORE_75	0x07	RW	Bit[7]: Not used Bit[6]: Line start select 0: Line start short packet from VFIFO non-empty 1: Line start short packet from VFIFO ready Bit[5]: EOF select Bit[4]: Virtual channel select Bit[3]: Data scramble enable Bit[2]: EOF busy select Bit[1]: Clock start select Bit[0]: SOF select
0x484C	MIPI_CORE_76	0x00	RW	Bit[7:1]: Not used Bit[0]: Disable frame count
0x484D	NOT USED	–	–	Not Used
0x484E	MIPI_CORE_78	0x10	RW	Bit[7:0]: Frame end delay
0x484F	MIPI_CORE_79	0x00	RW	Bit[7:4]: vc_height_sel Bit[3:1]: Not used Bit[0]: line_sleep_en
0x4850	MIPI_CORE_80	0x42	RW	Bit[7]: Not used Bit[6]: dphy12_frm_blk_opt Bit[5]: Deskew output enable Bit[4]: Deskew manual trigger Bit[3]: Initial deskew disable Bit[2]: Frame deskew disable Bit[1]: alt_cal_dis Bit[0]: DPHY1,2 enable
0x4851	MIPI_CORE_81	0xAA	RW	Bit[7:0]: Deskew data[7:0]
0x4852	MIPI_CORE_82	0xFF	RW	Bit[7:0]: Deskew sync data[7:0]
0x4853	MIPI_CORE_83	0x10	RW	Bit[7:0]: Deskew start delay[7:0]
0x4854	MIPI_CORE_84	0x05	RW	Bit[7:0]: Frame deskew width[7:0]
0x4855	MIPI_CORE_85	0x1C	RW	Bit[7:0]: Initial deskew width[7:0]
0x4856	MIPI_CORE_86	0x01	RW	Bit[7:0]: Frame deskew interval[7:0]
0x4857	MIPI_CORE_87	0x08	RW	Bit[7:4]: Not used Bit[3]: hs_same_time Bit[2:1]: Not used Bit[0]: deskew_en_man
0x4858	MIPI_CORE_88	0x1C	RW	Bit[7:0]: alt_deskew_interval[7:0]
0x4859~ 0x485F	NOT USED	–	–	Not Used

table 6-30 MIPI_CORE registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x4860	MIPI_CORE_96	0x00	RW	Bit[7:6]: C-PHY disable[1:0] Bit[5:4]: Not used Bit[3]: progseq_en Bit[2]: cphy_filler_dat Bit[1]: cphy_filler_en Bit[0]: C-PHY enable
0x4861	MIPI_CORE_97	0xEC	RW	Bit[7]: C-PHY escape flag Bit[6]: C-PHY escape flag Bit[5]: Not used Bit[4]: crc_sel_reg Bit[3]: cphy_pheader_order_sel Bit[2]: cphy_eot_same_time Bit[1]: cphy_trail_data_man Bit[0]: cphy_trail_man_en
0x4862	MIPI_CORE_98	0x04	RW	Bit[7:0]: C-PHY parameter[7:0]
0x4863~ 0x4864	NOT USED	–	–	Not Used
0x4865	MIPI_CORE_101	0x66	RW	Bit[7:0]: C-PHY programmable data1[7:0]
0x4866	MIPI_CORE_102	0x99	RW	Bit[7:0]: C-PHY programmable data2[7:0]
0x4867	MIPI_CORE_103	0x88	RW	Bit[7:0]: C-PHY programmable data3[7:0]
0x4868	MIPI_CORE_104	0xAA	RW	Bit[7:0]: C-PHY programmable data4[7:0]
0x4869	MIPI_CORE_105	0xFF	RW	Bit[7:0]: C-PHY preamble data1[7:0]
0x486A	MIPI_CORE_106	0x3F	RW	Bit[7:0]: C-PHY preamble data2[7:0]
0x486B	MIPI_CORE_107	0x84	RW	Bit[7:0]: C-PHY sync data1[7:0]
0x486C	MIPI_CORE_108	0x36	RW	Bit[7:0]: C-PHY sync data2[7:0]
0x486D	MIPI_CORE_109	0x00	RW	Bit[7:0]: Reverse data for C-PHY[7:0]
0x486E	MIPI_CORE_110	0x84	RW	Bit[7:0]: C-PHY escape data1[7:0]
0x486F	MIPI_CORE_111	0x36	RW	Bit[7:0]: C-PHY escape data2[7:0]
0x4870	MIPI_CORE_112	0x00	RW	Bit[7]: giic_ctrl_en Bit[6:0]: Not used

table 6-30 MIPI_CORE registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x4871	MIPI_CORE_113	0x10	RW	Bit[7]: prbs_seq_opt Bit[6:4]: prbs_deg_opt 000: prbs_disable 001: Deg9 010: Deg11 011: Deg16 100: Deg18 101: 4444 pattern 110: 20 pattern 111: 31 pattern Bit[3]: Not used Bit[2]: dphy_prbs9_opt Bit[1:0]: Output sequence option for PRBS
0x4872	MIPI_CORE_114	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: prbs_seed_lane0[17:16]
0x4873	MIPI_CORE_115	0x00	RW	Bit[7:0]: prbs_seed_lane0[15:8]
0x4874	MIPI_CORE_116	0xFF	RW	Bit[7:0]: prbs_seed_lane0[7:0]
0x4875	MIPI_CORE_117	0x00	RW	Bit[7:0]: prbs_seed_lane1[15:8]
0x4876	MIPI_CORE_118	0xFE	RW	Bit[7:0]: prbs_seed_lane1[7:0]
0x4877	MIPI_CORE_119	0x00	RW	Bit[7:0]: prbs_seed_lane2[15:8]
0x4878	MIPI_CORE_120	0xFD	RW	Bit[7:0]: prbs_seed_lane2[7:0]
0x4879	MIPI_CORE_121	0x00	RW	Bit[7:0]: prbs_seed_lane3[15:8]
0x487A	MIPI_CORE_122	0xFC	RW	Bit[7:0]: prbs_seed_lane3[7:0]
0x48C0	MIPI_CORE_192	0x00	RW	Bit[7:2]: Not used Bit[1]: color_bar_test_1frame Bit[0]: color_bar_test_en
0x48C1	MIPI_CORE_193	–	R	Bit[7:2]: Not used Bit[1]: color_bar_test_result Bit[0]: color_bar_test_done
0x48C2	MIPI_CORE_194	–	R	Bit[7:0]: color_bar_test_crc[15:8]
0x48C3	MIPI_CORE_195	–	R	Bit[7:0]: color_bar_test_crc[7:0]
0x48C4	MIPI_CORE_196	0x00	RW	Bit[7:0]: color_bar_test_golden[15:8]
0x48C5	MIPI_CORE_197	0x00	RW	Bit[7:0]: color_bar_test_golden[7:0]

6.31 MIPI_PHY [0x4880 - 0x488A]

table 6-31 MIPI_PHY registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4880	MIPI_PHY_0	0x00	RW	Bit[7]: Enable PLL2 debug output Bit[6]: Enable PCLK debug output Bit[5:3]: Clock lane skew adjustment Bit[2]: Disable clock lane Bit[1]: Test mode to force HS0 on clock/data lane Bit[0]: Enable PLL1 debug clock output
0x4881	MIPI_PHY_1	0x00	RW	Bit[7:5]: Data lane0 skew adjustment Bit[4]: Disable data lane0 Bit[3:1]: Data lane1 skew adjustment Bit[0]: Disable data lane1
0x4882	MIPI_PHY_2	0x00	RW	Bit[7:5]: Data lane2 skew adjustment Bit[4]: Disable data lane2 Bit[3:1]: Data lane3 skew adjustment Bit[0]: Disable data lane3
0x4883	MIPI_PHY_3	0x00	RW	Bit[7]: pll2_dac clock to MIPI PHY enable Bit[6]: Reserved Bit[5:4]: Coarse tuning register for high speed output voltage Bit[3]: Not used Bit[2:0]: Fine tuning register for high speed output voltage
0x4884	MIPI_PHY_4	0x09	RW	Bit[7]: ring_osc1_debug_o Bit[6]: ring_osc2_debug_o Bit[5]: Bypass HS TX enable retiming Bit[4:3]: LP TX driving strength adjustment Bit[2]: Select internal valid_2d delay 0: 2.5 HS clock delay 1: 3 HS clock delay Bit[1]: Not used Bit[0]: Enable MIPI self bias circuit
0x4885	MIPI_PHY_5	0x30	RW	Bit[7]: Not used Bit[6:4]: mipi_cphy_vcnt_set_o Bit[3:0]: MIPI HS TX driving strength adjustment
0x4886	MIPI_PHY_6	0x02	RW	Bit[7:6]: mipi_cphy_vcnt_set_o Bit[5:3]: Not used Bit[2]: n3_pin_swp Bit[1]: dis_data_wdg Bit[0]: dis_wdg

table 6-31 MIPI_PHY registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4887	MIPI_PHY_7	0x51	RW	Bit[7]: HS enable signal delay option Bit[6]: Select LPTX driver 0: Regulator mode 1: EVDD mode Bit[5]: MIPI D-PHY+ in-phase calibration 0: D-PHY 1.2 calibration mode 1: D-PHY+ in-phase calibration mode Bit[4]: De-emphasis mode selection 0: 7 dB 1: 3.5 dB Bit[3]: Enable de-emphasis function Bit[2:0]: D-emphasis amplitude adjustment
0x4888	MIPI_PHY_8	0x10	RW	Bit[7]: MIPI ring oscillator enable Bit[6]: MIPI LP data reset option 0: LP data reset to 1 1: LP data reset to 0 Bit[5]: Option of open termination output mode Bit[4]: PHY mode control 0: C-PHY mode 1: D-PHY mode Bit[3]: Not used Bit[2:0]: LP TX regulator output high voltage adjustment
0x4889	MIPI_PHY_9	0x00	RW	Bit[7]: Disable C-PHY trio0 Bit[6]: Disable C-PHY trio1 Bit[5]: Disable C-PHY trio2 Bit[4]: Disable C-PHY TX termination in idle mode Bit[3]: Enable C-PHY debug mode Bit[2:0]: Not used
0x488A	MIPI_PHY_10	0x00	RW	Bit[7:4]: mipi_bg_trim Bit[3]: MIPI BG bias selection Bit[2]: n3_hr_sel Bit[1:0]: MIPI HS TX slew rate control

6.32 TPM [0x4D00 - 0x4D23]

table 6-32 TPM registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4D00	R_TPM_SLOPE_H	0x05	RW	Bit[7:0]: r_tpm_slope[15:8]
0x4D01	R_TPM_SLOPE_L	0x19	RW	Bit[7:0]: r_tpm_slope[7:0]

table 6-32 TPM registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4D02	R_TPM_OFFSET_3	0xFD	RW	Bit[7:0]: r_tpm_offset[31:24]
0x4D03	R_TPM_OFFSET_2	0xD1	RW	Bit[7:0]: r_tpm_offset[23:16]
0x4D04	R_TPM_OFFSET_1	0xFF	RW	Bit[7:0]: r_tpm_offset[15:8]
0x4D05	R_TPM_OFFSET_0	0xFF	RW	Bit[7:0]: r_tpm_offset[7:0]
0x4D06	R_DIV	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: r_div[3:0]
0x4D07	R_CNT	0x07	RW	Bit[7:3]: Reserved Bit[2:0]: r_cnt_bit[2:0]
0x4D08	R_CLK_RE	1'b0	RW	Bit[7:1]: Reserved Bit[0]: r_clk_re[0]
0x4D09	R_STALL	1'b0	RW	Bit[7:1]: Reserved Bit[0]: r_stall[0]
0x4D0A	R_OTP_CTRL_EN	1'b0	RW	Bit[7:1]: Reserved Bit[0]: r_otp_ctrl_en[0]
0x4D0B	R_SOF_UPDATE_EN	1'b0	RW	Bit[7:1]: Reserved Bit[0]: r_sof_update_en[0]
0x4D0C	R_SHIFT	0x05	RW	Bit[7:5]: Reserved Bit[4:0]: r_shift_bit[4:0]
0x4D0D	R_PD_TPM_SNR	1'b0	RW	Bit[7:1]: Reserved Bit[0]: r_pd_tpm_snr[0]
0x4D0E	R_DIV_SEL	1'b0	RW	Bit[7:1]: Reserved Bit[0]: r_div_sel[0]
0x4D0F	R_MUL_DIV_SEL	1'b0	RW	Bit[7:1]: Reserved Bit[0]: r_mul_div_sel[0]
0x4D10	R_TPM_MIN	0x00	RW	Bit[7:0]: r_tpm_min[7:0]
0x4D11	R_TPM_MAX	0xFF	RW	Bit[7:0]: r_tpm_max[7:0]
0x4D12	TPM_CTRL_12	–	W	Writing register bit 0x4D12[0] to '1' will trigger temperature calculation, then registers 0x4D12 and 0x4D13 will be latched temperature value
0x4D13	TPM_CTRL_13	–	R	Latched Temperature Value, Integer Part
0x4D14	R_TPM_DEC_RDOUT	0x00	RW	Bit[7:0]: r_tpm_dec_rdout[7:0]
0x4D15	R_TPM_INT	0x00	RW	Bit[7:0]: r_tpm_int[7:0]
0x4D16	R_TPM_DEC	0x00	RW	Bit[7:0]: r_tpm_dec[7:0]
0x4D17	R_DB_NUM	0x00	RW	Bit[7:0]: r_db_num[7:0]

table 6-32 TPM registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4D18	R_DB_REAL_H	0x00	RW	Bit[7:0]: r_db_real[15:8]
0x4D19	R_DB_REAL_L	0x00	RW	Bit[7:0]: r_db_real[7:0]
0x4D1A	R_TPM_ABS_3	0x00	RW	Bit[7:0]: r_tpm_abs[31:24]
0x4D1B	R_TPM_ABS_2	0x00	RW	Bit[7:0]: r_tpm_abs[23:16]
0x4D1C	R_TPM_ABS_1	0x00	RW	Bit[7:0]: r_tpm_abs[15:8]
0x4D1D	R_TPM_ABS_0	0x00	RW	Bit[7:0]: r_tpm_abs[7:0]
0x4D1E	R_TPM_ADD_ABS_3	0x00	RW	Bit[7:0]: r_tpm_add_abs[31:24]
0x4D1F	R_TPM_ADD_ABS_2	0x00	RW	Bit[7:0]: r_tpm_add_abs[23:16]
0x4D20	R_TPM_ADD_ABS_1	0x00	RW	Bit[7:0]: r_tpm_add_abs[15:8]
0x4D21	R_TPM_ADD_ABS_0	0x00	RW	Bit[7:0]: r_tpm_add_abs[7:0]
0x4D22	R_TPM_ADD_H	0x00	RW	Bit[7:0]: r_tpm_add[15:8]
0x4D23	R_TPM_ADD_L	0x00	RW	Bit[7:0]: r_tpm_add[7:0]

6.33 ISP_TOP [0x5000 - 0x50B7]

table 6-33 ISP_top registers (sheet 1 of 16)

address	register name	default value	R/W	description
0x5000	ISP_TOP_0	0xF7	RW	Bit[7]: MF PD write back Range is [0:1] Bit[6]: DPC enable Range is [0:1] Bit[5]: MF enable Range is [0:1] Bit[4]: AWB gain enable Range is [0:1] Bit[3]: XTALK enable Range is [0:1] Bit[2]: OTP_DPC enable Range is [0:1] Bit[1]: PD compensation enable Range is [0:1] Bit[0]: ISP enable Range is [0:1]

table 6-33 ISP_top registers (sheet 2 of 16)

address	register name	default value	R/W	description
0x5001	ISP_TOP_1	0x1F	RW	Bit[7]: raw_bin_en Bit[6]: dpd_en Bit[5]: 4C to Bayer converter enable Bit[4]: raw_dns_en_l Range is [0:1] Bit[3]: raw_dns_en_m Range is [0:1] Bit[2]: raw_dns_en_s Range is [0:1] Bit[1]: binc_en Range is [0:1] Bit[0]: PD correction enable Range is [0:1]
0x5002	ISP_TOP_2	0x37	RW	Bit[7]: pre_bin_en Bit[6]: pre_bin_opt Bit[5]: para_latch_en Bit[4]: Latch module enable Range is [0:1] Bit[3]: Reserved Bit[2]: Black line HREF mask enable Range is [0:1] Bit[1]: re_timing_en Range is [0:1] Bit[0]: HREF before first VSYNC mask enable Range is [0:1]
0x5003	ISP_TOP_3	0x00	RW	Bit[7]: Reserved Bit[6]: Manual black ln number enable Range is [0:1] Bit[5]: Manual flip option enable Range is [0:1] Bit[4]: Manual mirror option enable Range is [0:1] Bit[3]: Manual BW mode enable Range is [0:1] Bit[2]: Manual XY bin enable Range is [0:1] Bit[1]: Manual XY even/odd step enable Range is [0:1] Bit[0]: Manual XY address start/end enable Range is [0:1]

table 6-33 ISP_top registers (sheet 3 of 16)

address	register name	default value	R/W	description
0x5004	ISP_TOP_4	0x80	RW	Bit[7]: mf_pdmap_sel Range is [0:1] Bit[6]: awbg_opt Bit[5]: Manual CFA pattern enable Range is [0:1] Bit[4]: Manual CFA array enable Range is [0:1] Bit[3]: Manual BLC enable Range is [0:1] Bit[2]: Manual exposure enable Range is [0:1] Bit[1]: Manual camera gain enable Range is [0:1] Bit[0]: Manual work mode enable Range is [0:1]
0x5005	ISP_TOP_5	0x40	RW	Bit[7:6]: raw_binning option Range is [0:3] Bit[5:4]: Manual exposure mode Range is [0:3] Bit[3]: Manual exposure mode enable Range is [0:1] Bit[2]: SRAM initial enable Range is [0:1] Bit[1]: Black line received by ISP Range is [0:1] Bit[0]: Gain iterate enable Range is [0:1]
0x5006	ISP_TOP_6	0x00	RW	Bit[7]: Reserved Bit[6]: Manual PD flip Range is [0:1] Bit[5]: Manual BW vbin2 Range is [0:1] Bit[4]: Manual BW hbin2 Range is [0:1] Bit[3]: xtc_flip Range is [0:1] Bit[2]: xtc_mirror Range is [0:1] Bit[1]: man_real_gain_en Range is [0:1] 0: Choose SOF of pre ISP 1: Choose VSYNC fall Bit[0]: Number of blank line to shift ahead[8] Range is [0:1]
0x5007	ISP_TOP_7	0x06	RW	Bit[7:0]: Number of blank line to shift ahead[7:0] Range is [0:255]

table 6-33 ISP_top registers (sheet 4 of 16)

address	register name	default value	R/W	description
0x5008	ISP_TOP_8	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Manual X address start[13:8] Range is [0:31]
0x5009	ISP_TOP_9	0x00	RW	Bit[7:0]: Manual X address start[7:0] Range is [0:255]
0x500A	ISP_TOP_A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y address start[12:8] Range is [0:31]
0x500B	ISP_TOP_B	0x00	RW	Bit[7:0]: Manual Y address start[7:0] Range is [0:255]
0x500C	ISP_TOP_C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Manual X address end[13:8] Range is [0:31]
0x500D	ISP_TOP_D	0x00	RW	Bit[7:0]: Manual X address end[7:0] Range is [0:255]
0x500E	ISP_TOP_E	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y address end[12:8] Range is [0:31]
0x500F	ISP_TOP_F	0x00	RW	Bit[7:0]: Manual Y address end[7:0] Range is [0:255]
0x5010	ISP_TOP_10	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual X even increment Range is [0:31]
0x5011	ISP_TOP_11	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual X odd increment Range is [0:31]
0x5012	ISP_TOP_12	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y even increment Range is [0:31]
0x5013	ISP_TOP_13	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y odd increment Range is [0:31]

table 6-33 ISP_top registers (sheet 5 of 16)

address	register name	default value	R/W	description
0x5014	ISP_TOP_14	0x00	RW	Bit[7]: Manual X bin2 Range is [0:1] Bit[6]: Manual Y bin2 Range is [0:1] Bit[5]: Manual X bin4 Range is [0:1] Bit[4]: Manual Y bin4 Range is [0:1] Bit[3:2]: Manual CFA pattern Range is [0:3] Bit[1]: Manual flip Range is [0:1] Bit[0]: Manual mirror Range is [0:1]
0x5015	ISP_TOP_15	0x20	RW	Bit[7:5]: Reserved Bit[4]: Manual X bin26 Range is [0:1] Bit[3]: Manual Y bin26 Range is [0:1] Bit[2:0]: Manual ISP mode Range is [0:7]
0x5016	ISP_TOP_16	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Manual real gain long[17:16] Range is [0:3]
0x5017	ISP_TOP_17	0x00	RW	Bit[7:0]: Manual real gain long[15:8] Range is [0:255]
0x5018	ISP_TOP_18	0x10	RW	Bit[7:0]: Manual real gain long[7:0] Range is [0:255]
0x5019	ISP_TOP_19	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Manual real gain medium[17:16] Range is [0:3]
0x501A	ISP_TOP_1A	0x00	RW	Bit[7:0]: Manual real gain medium[15:8] Range is [0:255]
0x501B	ISP_TOP_1B	0x10	RW	Bit[7:0]: Manual real gain medium[7:0] Range is [0:255]
0x501C	ISP_TOP_1C	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Manual real gain short[17:16] Range is [0:3]
0x501D	ISP_TOP_1D	0x00	RW	Bit[7:0]: Manual real gain short[15:8] Range is [0:255]
0x501E	ISP_TOP_1E	0x10	RW	Bit[7:0]: Manual real gain short[7:0] Range is [0:255]

table 6-33 ISP_top registers (sheet 6 of 16)

address	register name	default value	R/W	description
0x501F	ISP_TOP_1F	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual BLC long[11:8] Range is [0:15]
0x5020	ISP_TOP_20	0x10	RW	Bit[7:0]: Manual BLC long[7:0] Range is [0:255]
0x5021	ISP_TOP_21	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual BLC medium[11:8] Range is [0:15]
0x5022	ISP_TOP_22	0x10	RW	Bit[7:0]: Manual BLC medium[7:0] Range is [0:255]
0x5023	ISP_TOP_23	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: Manual BLC short[11:8] Range is [0:15]
0x5024	ISP_TOP_24	0x10	RW	Bit[7:0]: Manual BLC short[7:0] Range is [0:255]
0x5025	ISP_TOP_25	0x10	RW	Bit[7:0]: Manual expo medium channel[7:0] Range is [0:255]
0x5026	ISP_TOP_26	0x00	RW	Bit[7:0]: Manual expo short channel[15:8] Range is [0:255]
0x5027	RSVD	–	–	Reserved
0x5028	ISP_TOP_28	0x00	RW	Bit[7:0]: Manual extend expo L[31:24] Range is [0:255]
0x5029	ISP_TOP_29	0x00	RW	Bit[7:0]: Manual extend expo L[23:16] Range is [0:255]
0x502A	ISP_TOP_2A	0x04	RW	Bit[7:0]: Manual extend expo L[15:8] Range is [0:255]
0x502B	ISP_TOP_2B	0x00	RW	Bit[7:0]: Manual extend expo L[7:0] Range is [0:255]
0x502C	ISP_TOP_2C	0x00	RW	Bit[7:0]: Manual extend expo M[31:24] Range is [0:255]
0x502D	ISP_TOP_2D	0x00	RW	Bit[7:0]: Manual extend expo M[23:16] Range is [0:255]
0x502E	ISP_TOP_2E	0x04	RW	Bit[7:0]: Manual extend expo M[15:8] Range is [0:255]
0x502F	ISP_TOP_2F	0x00	RW	Bit[7:0]: Manual extend expo M[7:0] Range is [0:255]
0x5030	ISP_TOP_30	0x00	RW	Bit[7:0]: Manual extend expo S[31:24] Range is [0:255]

table 6-33 ISP_top registers (sheet 7 of 16)

address	register name	default value	R/W	description
0x5031	ISP_TOP_31	0x00	RW	Bit[7:0]: Manual extend expo S[23:16] Range is [0:255]
0x5032	ISP_TOP_32	0x04	RW	Bit[7:0]: Manual extend expo S[15:8] Range is [0:255]
0x5033	ISP_TOP_33	0x00	RW	Bit[7:0]: Manual extend expo S[7:0] Range is [0:255]
0x5034	ISP_TOP_34	0x00	RW	Bit[7:6]: Manual CFA array[0][0] Range is [0:3] Bit[5:4]: Manual CFA array[0][1] Range is [0:3] Bit[3:2]: Manual CFA array[0][2] Range is [0:3] Bit[1:0]: Manual CFA array[0][3] Range is [0:3]
0x5035	ISP_TOP_35	0x00	RW	Bit[7:6]: Manual CFA array[1][0] Range is [0:3] Bit[5:4]: Manual CFA array[1][1] Range is [0:3] Bit[3:2]: Manual CFA array[1][2] Range is [0:3] Bit[1:0]: Manual CFA array[1][3] Range is [0:3]
0x5036	ISP_TOP_36	0x00	RW	Bit[7:6]: Manual CFA array[2][0] Range is [0:3] Bit[5:4]: Manual CFA array[2][1] Range is [0:3] Bit[3:2]: Manual CFA array[2][2] Range is [0:3] Bit[1:0]: Manual CFA array[2][3] Range is [0:3]
0x5037	ISP_TOP_37	0x00	RW	Bit[7:6]: Manual CFA array[3][0] Range is [0:3] Bit[5:4]: Manual CFA array[3][1] Range is [0:3] Bit[3:2]: Manual CFA array[3][2] Range is [0:3] Bit[1:0]: Manual CFA array[3][3] Range is [0:3]
0x5038	ISP_TOP_38	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Focus window left[13:8] Range is [0:31]
0x5039	ISP_TOP_39	0x00	RW	Bit[7:0]: Focus window left[7:0] Range is [0:255]

table 6-33 ISP_top registers (sheet 8 of 16)

address	register name	default value	R/W	description
0x503A	ISP_TOP_3A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Focus window top[12:8] Range is [0:31]
0x503B	ISP_TOP_3B	0x00	RW	Bit[7:0]: Focus window top[7:0] Range is [0:255]
0x503C	ISP_TOP_3C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Focus window left[13:8] Range is [0:31]
0x503D	ISP_TOP_3D	0x00	RW	Bit[7:0]: Focus window left[7:0] Range is [0:255]
0x503E	ISP_TOP_3E	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Focus window top[12:8] Range is [0:31]
0x503F	ISP_TOP_3F	0x00	RW	Bit[7:0]: Focus window top[7:0] Range is [0:255]
0x5040	ISP_TOP_40	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: Manual black line number[9:8] Range is [0:3]
0x5041	ISP_TOP_41	0x00	RW	Bit[7:0]: Manual black line number[7:0] Range is [0:255]
0x5042	ISP_TOP_42	0x04	RW	Bit[7:6]: Reserved Bit[5]: Manual set VSYNC location in re-timing enable Range is [0:1] Bit[4:0]: Reserved
0x5043	RSVD	–	–	Reserved
0x5044	ISP_TOP_44	0x00	RW	Bit[7:2]: Reserved Bit[1]: man_dmy_disable Range is [0:1] Bit[0]: man_dummy_en Range is [0:1]
0x5045	ISP_TOP_45	0x00	RW	Bit[7:4]: man_valid_num Range is [0:15] Bit[3:0]: man_dmy_ratio Range is [0:15]
0x5046	ISP_TOP_46	0x00	RW	Bit[7:0]: man_nvalid_cnt[15:8] Range is [0:255]
0x5047	ISP_TOP_47	0x00	RW	Bit[7:0]: man_nvalid_cnt[7:0] Range is [0:255]

table 6-33 ISP_top registers (sheet 9 of 16)

address	register name	default value	R/W	description
0x5048	ISP_TOP_48	0x00	RW	Bit[7:0]: man_hblank_cnt[15:8] Range is [0:255]
0x5049	ISP_TOP_49	0x00	RW	Bit[7:0]: man_hblank_cnt[7:0] Range is [0:255]
0x504A	ISP_TOP_4A	0x00	RW	Bit[7]: dis_ck_gt_mf Range is [0:1] Bit[6]: dis_ck_gt_awb Range is [0:1] Bit[5]: dis_ck_gt_xtc Range is [0:1] Bit[4]: dis_ck_gt_otp_dpc Range is [0:1] Bit[3]: dis_ck_gt_pdc_vc Range is [0:1] Bit[2]: dis_ck_gt_pdc Range is [0:1] Bit[1]: dis_ck_gt_top Range is [0:1] Bit[0]: dis_ck_gt_all Range is [0:1]
0x504B	ISP_TOP_4B	0x00	RW	Bit[7]: dis_ck_gt_raw_bin Range is [0:1] Bit[6]: dis_ck_gt_regbus Range is [0:1] Bit[5]: dis_ck_gt_4cc Range is [0:1] Bit[4]: dis_ck_gt_raw_dns Range is [0:1] Bit[3]: dis_ck_gt_binc Range is [0:1] Bit[2]: dis_ck_gt_pdf Range is [0:1] Bit[1]: dis_ck_gt_dpc Range is [0:1] Bit[0]: dis_ck_gt_mf_back Range is [0:1]
0x504C	ISP_TOP_4C	0x00	RW	Bit[7]: dis_ck_gt_dpd Bit[6:4]: Reserved Bit[3]: sram_xtc_tm Range is [0:1] Bit[2]: sram_mem_tm Range is [0:1] Bit[1]: sram_mf_tm Range is [0:1] Bit[0]: sram_pdc_tm Range is [0:1]

table 6-33 ISP_top registers (sheet 10 of 16)

address	register name	default value	R/W	description
0x504D	ISP_TOP_4D	0x01	RW	Bit[7:6]: Reserved Bit[5]: XTALK SRAM cen Range is [0:1] Bit[4]: Shared MEM CTRL SRAM cen Range is [0:1] Bit[3]: MF PD WriteBack SRAM cen Range is [0:1] Bit[2]: Reserved Bit[1]: PDC SRAM cen Range is [0:1] Bit[0]: Cen global Range is [0:1]
0x504E	ISP_TOP_4E	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: pdc_sram_rtsel Bit[2:0]: pdc_sram_wtsel
0x504F	ISP_TOP_4F	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: mf_sram_rtsel Bit[2:0]: mf_sram_wtsel
0x5050	NOT USED	–	–	Not Used
0x5051	ISP_TOP_51	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: xtc_sram_rtsel Bit[2:0]: xtc_sram_wtsel
0x5052	ISP_TOP_52	0x00	RW	Bit[7:5]: Reserved Bit[4:3]: mem_sram_rtsel Bit[2:0]: mem_sram_wtsel
0x5053	ISP_TOP_53	0x04	RW	Bit[7:5]: Reserved Bit[4]: man_pd_density_en Bit[3:2]: man_pd_density_x Bit[1:0]: man_pd_density_y
0x5054	NOT USED	–	–	Not Used
0x5055	ISP_TOP_55	0x00	RW	Bit[7:0]: mem_pdbuf_en[23:16]
0x5056	ISP_TOP_56	0x00	RW	Bit[7:0]: mem_pdbuf_en[15:8]
0x5057	ISP_TOP_57	0x00	RW	Bit[7:0]: mem_pdbuf_en[7:0]

table 6-33 ISP_top registers (sheet 11 of 16)

address	register name	default value	R/W	description
0x5058	ISP_TOP_58	0x00	RW	Bit[7]: mf_back_bypass_en Range is [0:1] Bit[6]: dpc_bypass_en Range is [0:1] Bit[5]: mf_bypass_en Range is [0:1] Bit[4]: awbg_bypass_en Range is [0:1] Bit[3]: xtc_bypass_en Range is [0:1] Bit[2]: otp_bypass_en Range is [0:1] Bit[1]: pdc_bypass_en Range is [0:1] Bit[0]: isp_bypass_en Range is [0:1]
0x5059	ISP_TOP_59	0x00	RW	Bit[7]: inv_awb_bypass_en Bit[6]: combine_bypass_en Bit[5]: bayer_4c_bypass_en Bit[4]: raw_dns_bypass_en_l Range is [0:1] Bit[3]: raw_dns_bypass_en_m Range is [0:1] Bit[2]: raw_dns_bypass_en_s Range is [0:1] Bit[1]: binc_bypass_en Range is [0:1] Bit[0]: pdf_bypass_en Range is [0:1]
0x505A	ISP_TOP_5A	0x00	RW	Bit[7:0]: scale_gain_l[15:8] Range is [0:255]
0x505B	ISP_TOP_5B	0x10	RW	Bit[7:0]: scale_gain_l[7:0] Range is [0:255]
0x505C	ISP_TOP_5C	0x00	RW	Bit[7:0]: scale_gain_m[15:8] Range is [0:255]
0x505D	ISP_TOP_5D	0x10	RW	Bit[7:0]: scale_gain_m[7:0] Range is [0:255]
0x505E	ISP_TOP_5E	0x00	RW	Bit[7:0]: scale_gain_s[15:8] Range is [0:255]
0x505F	ISP_TOP_5F	0x10	RW	Bit[7:0]: scale_gain_s[7:0] Range is [0:255]
0x5060	ISP_TOP_60	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Winxstart[13:8] Range is [0:8191]

table 6-33 ISP_top registers (sheet 12 of 16)

address	register name	default value	R/W	description
0x5061	ISP_TOP_61	0x20	RW	Bit[7:0]: Winxstart[7:0] Range is [0:8191]
0x5062	ISP_TOP_62	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Winystart[12:8] Range is [0:8191]
0x5063	ISP_TOP_63	0x20	RW	Bit[7:0]: Winystart[7:0] Range is [0:8191]
0x5064	ISP_TOP_64	0x24	RW	Bit[7:6]: Not used Bit[5:0]: Winwidth[13:8] Range is [0:8191]
0x5065	ISP_TOP_65	0x00	RW	Bit[7:0]: Winwidth[7:0] Range is [0:8191]
0x5066	ISP_TOP_66	0x1B	RW	Bit[7:5]: Not used Bit[4:0]: Winheight[12:8] Range is [0:8191]
0x5067	ISP_TOP_67	0x00	RW	Bit[7:0]: Winheight[7:0] Range is [0:8191]
0x5068	ISP_TOP_68	0x01	RW	Bit[7:2]: Reserved Bit[1]: focus_win_en Bit[0]: ML2x2pattern Range is [0:1]
0x5069	ISP_TOP_69	0x10	RW	Bit[7:6]: Not used Bit[5:0]: PDcycleX Range is [1:32]
0x506A	ISP_TOP_6A	0x10	RW	Bit[7:6]: Not used Bit[5:0]: PDcycleY Range is [1:32]
0x506B	ISP_TOP_6B	0x04	RW	Bit[7:5]: Not used Bit[4:0]: PDX1 Range is [0:31]
0x506C	ISP_TOP_6C	0x04	RW	Bit[7:5]: Not used Bit[4:0]: PDX2 Range is [0:31]
0x506D	ISP_TOP_6D	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: PDX3 Range is [0:31]
0x506E	ISP_TOP_6E	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: PDX4 Range is [0:31]

table 6-33 ISP_top registers (sheet 13 of 16)

address	register name	default value	R/W	description
0x506F	ISP_TOP_6F	0x04	RW	Bit[7:5]: Not used Bit[4:0]: PDY1 Range is [0:31]
0x5070	ISP_TOP_70	0x04	RW	Bit[7:5]: Not used Bit[4:0]: PDY2 Range is [0:31]
0x5071	ISP_TOP_71	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: PDY3 Range is [0:31]
0x5072	ISP_TOP_72	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: PDY4 Range is [0:31]
0x5073	ISP_TOP_73	0x01	RW	Bit[7:5]: Not used Bit[4:0]: PDskipX Range is [0:31]
0x5074	ISP_TOP_74	0x01	RW	Bit[7:5]: Not used Bit[4:0]: PDskipY Range is [0:31]
0x5075	ISP_TOP_75	0xAA	RW	Bit[7:6]: PDCH1 Range is [0:3] Bit[5:4]: PDCH2 Range is [0:3] Bit[3:2]: PDCH3 Range is [0:3] Bit[1:0]: PDCH4 Range is [0:3]
0x5076	ISP_TOP_76	0x24	RW	Bit[7:6]: Not used Bit[5:0]: Arraywidth[13:8] Range is [0:8191]
0x5077	ISP_TOP_77	0x40	RW	Bit[7:0]: Arraywidth[7:0] Range is [0:8191]
0x5078	ISP_TOP_78	0x1B	RW	Bit[7:5]: Not used Bit[4:0]: Arrayheight[12:8] Range is [0:8191]
0x5079	ISP_TOP_79	0x40	RW	Bit[7:0]: Arrayheight[7:0] Range is [0:8191]
0x507A	ISP_TOP_7A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: manual_dmy_num0
0x507B	ISP_TOP_7B	0x00	RW	Bit[7:5]: Not used Bit[4:0]: manual_dmy_num1

table 6-33 ISP_top registers (sheet 14 of 16)

address	register name	default value	R/W	description
0x507C~ 0x5082	NOT USED	–	–	Not Used
0x5083	ISP_TOP_83	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: hdr_mode
0x5084	ISP_TOP_84	0x00	RW	Bit[7]: twopipe_offset_man_en Bit[6]: twopipe_focuswin_man_en Bit[5:0]: man_preisp_hsize[13:8]
0x5085	ISP_TOP_85	0x00	RW	Bit[7:0]: man_preisp_hsize[7:0]
0x5086	ISP_TOP_86	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_rp_xoffset[13:8]
0x5087	ISP_TOP_87	0x00	RW	Bit[7:0]: man_rp_xoffset[7:0]
0x5088	ISP_TOP_88	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_lp_xend[13:8]
0x5089	ISP_TOP_89	0x00	RW	Bit[7:0]: man_lp_xend[7:0]
0x508A	ISP_TOP_8A	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_rp_winleft[13:8]
0x508B	ISP_TOP_8B	0x00	RW	Bit[7:0]: man_rp_winleft[7:0]
0x508C	ISP_TOP_8C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_lp_winwidth[13:8]
0x508D	ISP_TOP_8D	0x00	RW	Bit[7:0]: man_lp_winwidth[7:0]
0x508E	ISP_TOP_8E	0x00	RW	Bit[7:6]: Not used Bit[5:0]: man_rp_winwidth[13:8]
0x508F	ISP_TOP_8F	0x00	RW	Bit[7:0]: man_rp_winwidth[7:0]
0x5090	ISP_TOP_90	0x20	RW	Bit[7:0]: overlap_num
0x5091~ 0x509F	NOT USED	–	–	Not Used
0x50A0	ISP_TOP_A0	–	R	Bit[7:4]: Not used Bit[3]: Flip Range is [0:1] Bit[2]: Mirror Range is [0:1] Bit[1]: X bin2 Range is [0:3] Bit[0]: Y bin2

table 6-33 ISP_top registers (sheet 15 of 16)

address	register name	default value	R/W	description
0x50A1	ISP_TOP_A1	–	R	Bit[7:6]: Not used Bit[5]: pd_writeback_fifo_full Range is [0:1] Bit[4:3]: CFA pattern Range is [0:3] Bit[2:0]: Work mode Range is [0:3]
0x50A2	ISP_TOP_A2	–	R	Bit[7:6]: Not used Bit[5:0]: Horizontal start point[13:8] Range is [0:31]
0x50A3	ISP_TOP_A3	–	R	Bit[7:0]: Horizontal start point[7:0] Range is [0:255]
0x50A4	ISP_TOP_A4	–	R	Bit[7:6]: Not used Bit[5:0]: Horizontal end point[13:8] Range is [0:31]
0x50A5	ISP_TOP_A5	–	R	Bit[7:0]: Horizontal end point[7:0] Range is [0:255]
0x50A6	ISP_TOP_A6	–	R	Bit[7:5]: Not used Bit[4:0]: Vertical start point[12:8] Range is [0:15]
0x50A7	ISP_TOP_A7	–	R	Bit[7:0]: Vertical start point[7:0] Range is [0:255]
0x50A8	ISP_TOP_A8	–	R	Bit[7:5]: Not used Bit[4:0]: Vertical end point[12:8] Range is [0:15]
0x50A9	ISP_TOP_A9	–	R	Bit[7:0]: Vertical end point[7:0] Range is [0:255]
0x50AA	ISP_TOP_AA	–	R	Bit[7:4]: X even increment Range is [0:15] Bit[3:0]: X odd increment Range is [0:15]
0x50AB	ISP_TOP_AB	–	R	Bit[7:4]: Y even increment Range is [0:15] Bit[3:0]: Y odd increment Range is [0:15]
0x50AC	ISP_TOP_AC	–	R	Bit[7:4]: Not used Bit[3:0]: Real gain long[11:8] Range is [0:15]
0x50AD	ISP_TOP_AD	–	R	Bit[7:0]: Real gain long[7:0] Range is [0:255]

table 6-33 ISP_top registers (sheet 16 of 16)

address	register name	default value	R/W	description
0x50AE	ISP_TOP_AE	–	R	Bit[7:4]: Not used Bit[3:0]: BLC long[11:8]
0x50AF	ISP_TOP_AF	–	R	Bit[7:0]: BLC long[7:0]
0x50B0	ISP_TOP_B0	–	R	Bit[7:4]: Not used Bit[3:0]: Real gain medium[11:8] Range is [0:3]
0x50B1	ISP_TOP_B1	–	R	Bit[7:0]: Real gain medium[7:0] Range is [0:255]
0x50B2	ISP_TOP_B2	–	R	Bit[7:4]: Not used Bit[3:0]: BLC medium[11:8] Range is [0:15]
0x50B3	ISP_TOP_B3	–	R	Bit[7:0]: BLC medium[7:0] Range is [0:255]
0x50B4	ISP_TOP_B4	–	R	Bit[7:4]: Not used Bit[3:0]: Real gain short[11:8]
0x50B5	ISP_TOP_B5	–	R	Bit[7:0]: Real gain short[7:0]
0x50B6	ISP_TOP_B6	–	R	Bit[7:4]: Not used Bit[3:0]: BLC short[11:8] Range is [0:3]
0x50B7	ISP_TOP_B7	–	R	Bit[7:0]: BLC short[7:0] Range is [0:255]

6.34 PRE_ISP_L [0x50C0 - 0x50E7]

table 6-34 PRE_ISP_L registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x50C0	PRE_ISP_2325_D2V2_TOP_0	0x00	RW	Bit[7:5]: Not used Bit[4]: Disable clock gating Range is [0:1] Bit[3]: Reserved Bit[2]: Manual size enable Range is [0:1] Bit[1]: Manual end address enable Range is [0:1] Bit[0]: Manual offset (start address) enable Range is [0:1]

table 6-34 PRE_ISP_L registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x50C1	PRE_ISP_2325_D2V2_TOP_1	0x00	RW	Bit[7]: Flip option Range is [0:1] Bit[6]: Mirror option Range is [0:1] Bit[5:4]: Color bar option Range is [0:3] Bit[3]: Transparent mode enable Range is [0:1] Bit[2]: Rolling mode enable Range is [0:1] Bit[1]: Clear last four bits enable Range is [0:1] Bit[0]: Test pattern enable Range is [0:1]
0x50C2	PRE_ISP_2325_D2V2_TOP_2	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Test pattern mode Range is [0:7]
0x50C3	RSVD	–	–	Reserved
0x50C4	PRE_ISP_2325_D2V2_TOP_4	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Manual width[13:8] Range is [0:4704]
0x50C5	PRE_ISP_2325_D2V2_TOP_5	0x80	RW	Bit[7:0]: Manual width[7:0] Range is [0:4704]
0x50C6	PRE_ISP_2325_D2V2_TOP_6	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual height[12:8] Range is [0:3536]
0x50C7	PRE_ISP_2325_D2V2_TOP_7	0xE0	RW	Bit[7:0]: Manual height[7:0] Range is [0:3536]
0x50C8	PRE_ISP_2325_D2V2_TOP_8	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Manual X offset[13:8] Range is [0:4704]
0x50C9	PRE_ISP_2325_D2V2_TOP_9	0x00	RW	Bit[7:0]: Manual X offset[7:0] Range is [0:4704]
0x50CA	PRE_ISP_2325_D2V2_TOP_A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y offset[12:8] Range is [0:3536]
0x50CB	PRE_ISP_2325_D2V2_TOP_B	0x00	RW	Bit[7:0]: Manual Y offset[7:0] Range is [0:3536]
0x50CC	PRE_ISP_2325_D2V2_TOP_C	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Manual X end[13:8] Range is [0:4704]

table 6-34 PRE_ISP_L registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x50CD	PRE_ISP_2325_D2V2_TOP_D	0x80	RW	Bit[7:0]: Manual X end[7:0] Range is [0:4704]
0x50CE	PRE_ISP_2325_D2V2_TOP_E	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y end[12:8] Range is [0:3536]
0x50CF	PRE_ISP_2325_D2V2_TOP_F	0xE0	RW	Bit[7:0]: Manual Y end[7:0] Range is [0:3536]
0x50D0~ 0x50D1	NOT USED	–	–	Not Used
0x50D2	PRE_ISP_2325_D2V2_TOP_12	0x01	RW	Bit[7:5]: Not used Bit[4:0]: In_number[12:8] Range is [0:3536]
0x50D3	PRE_ISP_2325_D2V2_TOP_13	0xE0	RW	Bit[7:0]: In_number[7:0] Range is [0:3536]
0x50D4~ 0x50D7	NOT USED	–	–	Not Used
0x50D8	PRE_ISP_2325_D2V2_TOP_18	–	R	Bit[7:6]: Reserved Bit[5:0]: Pixel count[13:8] Range is [0:3536]
0x50D9	PRE_ISP_2325_D2V2_TOP_19	–	R	Bit[7:0]: Pixel count[7:0] Range is [0:3536]
0x50DA	PRE_ISP_2325_D2V2_TOP_1A	–	R	Bit[7:5]: Reserved Bit[4:0]: Line count[12:8] Range is [0:255]
0x50DB	PRE_ISP_2325_D2V2_TOP_1B	–	R	Bit[7:0]: Line count[7:0] Range is [0:255]
0x50DC	PRE_ISP_2325_D2V2_TOP_1C	–	R	Bit[7:0]: dbg_0 Range is [0:255]
0x50DD	PRE_ISP_2325_D2V2_TOP_1D	–	R	Bit[7:0]: dbg_1 Range is [0:255]
0x50DE	PRE_ISP_2325_D2V2_TOP_1E	–	R	Bit[7:0]: dbg_2 Range is [0:1]
0x50DF	PRE_ISP_2325_D2V2_TOP_1F	–	R	Bit[7:0]: dbg_3 Range is [0:8191]
0x50E0	PRE_ISP_2325_D2V2_TOP_20	–	R	Bit[7:6]: Reserved Bit[5:0]: x_offset[13:8] Range is [0:8191]
0x50E1	PRE_ISP_2325_D2V2_TOP_21	–	R	Bit[7:0]: x_offset[7:0] Range is [0:8191]

table 6-34 PRE_ISP_L registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x50E2	PRE_ISP_2325_D2V2_TOP_22	–	R	Bit[7:5]: Reserved Bit[4:0]: y_offset[12:8] Range is [0:4095]
0x50E3	PRE_ISP_2325_D2V2_TOP_23	–	R	Bit[7:0]: y_offset[7:0] Range is [0:4095]
0x50E4~ 0x50E5	NOT USED	–	–	Not Used
0x50E6	PRE_ISP_2325_D2V2_TOP_26	–	R	Bit[7:0]: Software version[15:8] Range is [0:255]
0x50E7	PRE_ISP_2325_D2V2_TOP_27	–	R	Bit[7:0]: Hardware version[7:0] Range is [0:255]

6.35 AWBG_L [0x50F0 - 0x5107]

table 6-35 AWBG_L registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x50F0	AWBG_24_0	0xEE	RW	Bit[7:0]: CFAY[31:24]
0x50F1	AWBG_24_1	0x44	RW	Bit[7:0]: CFAY[23:16]
0x50F2	AWBG_24_2	0xEE	RW	Bit[7:0]: CFAY[15:8]
0x50F3	AWBG_24_3	0x44	RW	Bit[7:0]: CFAY[7:0]
0x50F4	AWBG_24_4	0x00	RW	Bit[7:0]: gain_lat_sel[7:0]
0x50F5	AWBG_24_5	0x02	RW	Bit[7:4]: Not used Bit[3]: cfay_man_en Bit[2]: blc_man_en Bit[1:0]: mne[9:8]
0x50F6	AWBG_24_6	0x00	RW	Bit[7:0]: MNE[7:0]
0x50F7	AWBG_24_7	0x00	RW	Bit[7:0]: BLC
0x50F8~ 0x50FF	RSVD	–	–	Reserved
0x5100	AWBG_24_8	0x04	RW	Bit[7:0]: cfa_gain0[15:8]
0x5101	AWBG_24_9	0x00	RW	Bit[7:0]: cfa_gain0[7:0]
0x5102	AWBG_24_A	0x04	RW	Bit[7:0]: cfa_gain1[15:8]

table 6-35 AWBG_L registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5103	AWBG_24_B	0x00	RW	Bit[7:0]: cfa_gain1[7:0]
0x5104	AWBG_24_C	0x04	RW	Bit[7:0]: cfa_gain2[15:8]
0x5105	AWBG_24_D	0x00	RW	Bit[7:0]: cfa_gain2[7:0]
0x5106	AWBG_24_E	0x04	RW	Bit[7:0]: cfa_gain3[15:8]
0x5107	AWBG_24_F	0x00	RW	Bit[7:0]: cfa_gain3[7:0]

6.36 OTP_L [0x5110 - 0x5141]

table 6-36 OTP_L registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5110	OTP_DPC_3615_D2V2_0	0x00	RW	Bit[7:0]: OTP eFUSE start address[15:8]
0x5111	OTP_DPC_3615_D2V2_1	0x00	RW	Bit[7:0]: OTP eFUSE start address[7:0]
0x5112	OTP_DPC_3615_D2V2_2	0xFF	RW	Bit[7:0]: OTP eFUSE end address[15:8]
0x5113	OTP_DPC_3615_D2V2_3	0xFF	RW	Bit[7:0]: OTP eFUSE end address[7:0]
0x5114	OTP_DPC_3615_D2V2_4	0x01	RW	Bit[7]: Manual size enable Bit[6]: Disable mirror and flip Range is [0:1] Bit[5]: Disable binning Range is [0:1] Bit[4]: Detection enable Range is [0:1] Bit[3]: Auto mode using exposure enable Range is [0:1] Bit[2]: Auto mode using gain enable Range is [0:1] Bit[1]: Flip option Range is [0:1] Bit[0]: Mirror option Range is [0:1]

table 6-36 OTP_L registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5115	OTP_DPC_3615_D2V2_5	0x0B	RW	Bit[7]: OTP eFUSE debug mode enable Read out data of debug address in eFUSE Range is [0:1] Bit[6]: Cluster data bypass enable Range is [0:1] Bit[5]: Manual increase step enable Range is [0:1] Bit[4]: Fixed pattern enable Range is [0:1] Bit[3]: Fixed pattern selection Range is [0:1] Bit[2:0]: Recovery method selection Range is [0:4]
0x5116	OTP_DPC_3615_D2V2_6	0x80	RW	Bit[7]: Gain-dependent OTP_DPC cluster enable Bit[6]: Disable detect and remove blocks' clock gating option Bit[5]: Disable get_cluster block's clock gating option Bit[4]: Disable start frame process logic clock gating option Bit[3]: Disable cluster_buf 1 of short exposure block's clock gating option Bit[2]: Disable cluster_buf 0 of short exposure block's clock gating option Bit[1]: Disable cluster_buf 1 of long exposure block's clock gating option Bit[0]: Disable cluster_buf 0 of long exposure block's clock gating option
0x5117	OTP_DPC_3615_D2V2_7	0x00	RW	Bit[7]: Manual Y direction binning enable Bit[6]: Manual Y direction bin4 enable Bit[5]: Manual Y direction bin3 enable Bit[4]: Manual Y direction bin2 enable Bit[3]: Manual X direction binning enable Bit[2]: Manual X direction bin4 enable Bit[1]: Manual X direction bin3 enable Bit[0]: Manual X direction bin2 enable

table 6-36 OTP_L registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5118	OTP_DPC_3615_D2V2_8	0x08	RW	Bit[7]: Manual offset enable Range is [0:1] Bit[6]: Manual offset enable Range is [0:1] Bit[5]: Manual Y direction BW binning enable Bit[4]: Manual X direction BW binning enable Bit[3:0]: Detection threshold for exposure 0 channel Range is [0:15]
0x5119	OTP_DPC_3615_D2V2_9	0x07	RW	Bit[7:0]: Gain threshold for exposure 0 channel Range is [0:255]
0x511A	OTP_DPC_3615_D2V2_A	0x00	RW	Bit[7]: Not used Bit[6:0]: Exposure threshold for exposure 0 channel[14:8] Range is [0:32767]
0x511B	OTP_DPC_3615_D2V2_B	0x00	RW	Bit[7:0]: Exposure threshold for exposure 0 channel[7:0] Range is [0:32767]
0x511C	OTP_DPC_3615_D2V2_C	0x01	RW	Bit[7]: Not used Bit[6]: y_bin26_man Bit[5]: x_bin26_man Bit[4:0]: Manual X direction increase step of even points Range is [0:31]
0x511D	OTP_DPC_3615_D2V2_D	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual X direction increase step of odd points Range is [0:31]
0x511E	OTP_DPC_3615_D2V2_E	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y direction increase step of even points Range is [0:31]
0x511F	OTP_DPC_3615_D2V2_F	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y direction increase step of odd points Range is [0:31]
0x5120	OTP_DPC_3615_D2V2_10	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[15:8] Range is [0:65535]

table 6-36 OTP_L registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x5121	OTP_DPC_3615_D2V2_11	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[7:0] Range is [0:65535]
0x5122	OTP_DPC_3615_D2V2_12	0x16	RW	Bit[7:0]: Manual X direction end in sensor array[15:8]
0x5123	OTP_DPC_3615_D2V2_13	0x3F	RW	Bit[7:0]: Manual X direction end in sensor array[7:0]
0x5124	OTP_DPC_3615_D2V2_14	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array[15:8] Range is [0:65535]
0x5125	OTP_DPC_3615_D2V2_15	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array[7:0] Range is [0:65535]
0x5126	OTP_DPC_3615_D2V2_16	0x00	RW	Bit[7:0]: OTP eFUSE debug address[15:8]
0x5127	OTP_DPC_3615_D2V2_17	0x00	RW	Bit[7:0]: OTP eFUSE debug address[7:0]
0x5128	NOT USED	–	–	Not Used
0x5129	OTP_DPC_3615_D2V2_19	0x01	RW	Bit[7:6]: Not used Bit[5]: Replace detected defect pixel with its position in sensor array Bit[4]: Position counter select 0: V counter 1: H counter Bit[3:0]: Gain-dependent threshold for exposure 0 channel Range is [0:15]
0x512A	OTP_DPC_3615_D2V2_1A	0x00	RW	Bit[7:0]: Manual hsize[15:8] Range is [0:65535]
0x512B	OTP_DPC_3615_D2V2_1B	0x00	RW	Bit[7:0]: Manual hsize[7:0] Range is [0:65535]
0x512C	OTP_DPC_3615_D2V2_1C	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[15:8] Range is [0:65535]
0x512D	OTP_DPC_3615_D2V2_1D	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[7:0] Range is [0:65535]
0x512E	OTP_DPC_3615_D2V2_1E	0x16	RW	Bit[7:0]: Manual X direction end in sensor array[15:8]
0x512F	OTP_DPC_3615_D2V2_1F	0x3F	RW	Bit[7:0]: Manual X direction end in sensor array[7:0]

table 6-36 OTP_L registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5130	OTP_DPC_3615_D2V2_20	–	R	Bit[7:0]: X direction offset in sensor array[15:8]
0x5131	OTP_DPC_3615_D2V2_21	–	R	Bit[7:0]: X direction offset in sensor array[7:0]
0x5132	OTP_DPC_3615_D2V2_22	–	R	Bit[7:0]: Y direction offset in sensor array[15:8]
0x5133	OTP_DPC_3615_D2V2_23	–	R	Bit[7:0]: Y direction offset in sensor array[7:0]
0x5134	OTP_DPC_3615_D2V2_24	–	R	Bit[7:0]: X direction end position in sensor array[15:8]
0x5135	OTP_DPC_3615_D2V2_25	–	R	Bit[7:0]: X direction end position in sensor array[7:0]
0x5136	OTP_DPC_3615_D2V2_26	–	R	Bit[7:5]: Reserved Bit[4:0]: X direction increase step of even points
0x5137	OTP_DPC_3615_D2V2_27	–	R	Bit[7:5]: Reserved Bit[4:0]: X direction increase step of odd points
0x5138	OTP_DPC_3615_D2V2_28	–	R	Bit[7:5]: Reserved Bit[4:0]: Y direction increase step of even points
0x5139	OTP_DPC_3615_D2V2_29	–	R	Bit[7:5]: Reserved Bit[4:0]: Y direction increase step of odd points
0x513A	OTP_DPC_3615_D2V2_2A	–	R	Bit[7]: Y direction BW binning Bit[6]: Y direction bin4 Bit[5]: Y direction bin3 Bit[4]: Y direction bin2 Bit[3]: X direction BW binning Bit[2]: X direction bin4 Bit[1]: X direction bin3 Bit[0]: X direction bin2
0x513B	OTP_DPC_3615_D2V2_2B	–	R	Bit[7:0]: Data of debug address in OTP eFUSE
0x513C	OTP_DPC_3615_D2V2_2C	–	R	Bit[7:0]: X direction offset in sensor array[15:8]
0x513D	OTP_DPC_3615_D2V2_2D	–	R	Bit[7:0]: X direction offset in sensor array[7:0]
0x513E	OTP_DPC_3615_D2V2_2E	–	R	Bit[7:0]: X direction end position in sensor array[15:8]
0x513F	OTP_DPC_3615_D2V2_2F	–	R	Bit[7:0]: X direction end position in sensor array[7:0]

table 6-36 OTP_L registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x5140	OTP_DPC_3615_D2V2_30	–	R	Bit[7:0]: Software version
0x5141	OTP_DPC_3615_D2V2_31	–	R	Bit[7:0]: Hardware version

6.37 DPC_L [0x5150 - 0x5177]

table 6-37 DPC_L registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5150~ 0x5151	NOT USED	–	–	Not Used
0x5152	DPC_1715_D2V2_2	0x03	RW	Bit[7:4]: Not used Bit[3]: Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x5153	DPC_1715_D2V2_3	0x0C	RW	Bit[7]: Not used Bit[6]: Line data select 0: Use dummy line data 1: Last two lines re-use bound data Bit[5]: HDR/SBS select 0: HDR 1: SBS Bit[4]: algorithm_opt Bit[3:2]: Edge filling option Bit[1:0]: RGB/G/BR select 00: RGB 01: G 10: Not used 11: BR
0x5154	DPC_1715_D2V2_4	0x04	RW	Bit[7:0]: White pixel threshold list[0]
0x5155	DPC_1715_D2V2_5	0x04	RW	Bit[7:0]: White pixel threshold list[1]
0x5156	DPC_1715_D2V2_6	0x04	RW	Bit[7:0]: White pixel threshold list[2]
0x5157	DPC_1715_D2V2_7	0x04	RW	Bit[7:0]: White pixel threshold list[3]
0x5158	DPC_1715_D2V2_8	0x04	RW	Bit[7:0]: Black pixel threshold list[0]
0x5159	DPC_1715_D2V2_9	0x04	RW	Bit[7:0]: Black pixel threshold list[1]
0x515A	DPC_1715_D2V2_A	0x04	RW	Bit[7:0]: Black pixel threshold list[2]
0x515B	DPC_1715_D2V2_B	0x04	RW	Bit[7:0]: Black pixel threshold list[3]

table 6-37 DPC_L registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x515C	NOT USED	–	–	Not Used
0x515D	DPC_1715_D2V2_D	0x03	RW	Bit[7:0]: Gain control point[0]
0x515E	DPC_1715_D2V2_E	0x08	RW	Bit[7:0]: Gain control point[1]
0x515F	DPC_1715_D2V2_F	0x0C	RW	Bit[7:0]: Gain control point[2]
0x5160	DPC_1715_D2V2_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[0]
0x5161	DPC_1715_D2V2_11	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[1]
0x5162	DPC_1715_D2V2_12	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[2]
0x5163	DPC_1715_D2V2_13	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[3]
0x5164	DPC_1715_D2V2_14	0x08	RW	Bit[7:0]: White couplet defect pixel correction gain threshold
0x5165	DPC_1715_D2V2_15	0x08	RW	Bit[7:4]: Not used Bit[3:0]: White couplet defect pixel correction gain threshold
0x5166	DPC_1715_D2V2_16	0x08	RW	Bit[7:0]: Black couplet defect pixel correction gain threshold
0x5167	DPC_1715_D2V2_17	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Black couplet defect pixel correction gain threshold
0x5168	NOT USED	–	–	Not Used
0x5169	DPC_1715_D2V2_19	0x08	RW	Bit[7:4]: Not used Bit[3:0]: White couplet threshold ratio
0x516A	DPC_1715_D2V2_1A	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Black couplet threshold ratio
0x516B	DPC_1715_D2V2_1B	0xFF	RW	Bit[7:0]: Saturation threshold
0x516C	DPC_1715_D2V2_1C	0x01	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[0]
0x516D	DPC_1715_D2V2_1D	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[1]
0x516E	DPC_1715_D2V2_1E	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[2]
0x516F	DPC_1715_D2V2_1F	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[3]

table 6-37 DPC_L registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5170	DPC_1715_D2V2_20	0x01	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[0]
0x5171	DPC_1715_D2V2_21	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[1]
0x5172	DPC_1715_D2V2_22	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[2]
0x5173	DPC_1715_D2V2_23	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[3]
0x5174~ 0x5175	NOT USED	–	–	Not Used
0x5176	DPC_1715_D2V2_26	–	R	Bit[7:0]: dpc_ver[15:8]
0x5177	DPC_1715_D2V2_27	–	R	Bit[7:0]: dpc_ver[7:0]

6.38 RAW_BIN_L [0x5180 - 0x518D]

table 6-38 RAW_BIN_L registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5180	RAW_BIN_1315_D2V2_TOP_0	0xC5	RW	Bit[7:3]: m_nVFilter[0] Vertical filter coefficients Bit[2]: m_bPDCheck_enable Enable PD check Bit[1]: m_bVBinningEnable Enable vertical binning Bit[0]: m_bHBinningEnable Enable horizontal binning
0x5181	RAW_BIN_1315_D2V2_TOP_1	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilter[1] Vertical filter coefficients
0x5182	RAW_BIN_1315_D2V2_TOP_2	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilter[2] Vertical filter coefficients
0x5183	RAW_BIN_1315_D2V2_TOP_3	0x18	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilter[3] Vertical filter coefficients

table 6-38 RAW_BIN_L registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5184	RAW_BIN_1315_D2V2_TOP_4	0x18	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[0] Horizontal filter coefficients
0x5185	RAW_BIN_1315_D2V2_TOP_5	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[1] Horizontal filter coefficients
0x5186	RAW_BIN_1315_D2V2_TOP_6	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[2] Horizontal filter coefficients
0x5187	RAW_BIN_1315_D2V2_TOP_7	0x18	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[3] Horizontal filter coefficients
0x5188	RAW_BIN_1315_D2V2_TOP_8	0x05	RW	Bit[7:6]: Not used Bit[5:0]: m_nVFilterShift Vertical filter shift
0x5189	RAW_BIN_1315_D2V2_TOP_9	0x05	RW	Bit[7:6]: Not used Bit[5:0]: m_nHFilterShift Horizontal filter shift
0x518A	RAW_BIN_1315_D2V2_TOP_A	0x00	RW	Bit[7:3]: Not used Bit[2]: m_bKeepBLC Keep BLC same for BWBin sum Bit[1]: BWBinSumEn BWBin sum enable option Bit[0]: m_bBWBin BW bin enable
0x518B	NOT USED	–	–	Not Used
0x518C	RAW_BIN_1315_D2V2_TOP_C	–	R	Bit[7:0]: RAW BIN version[15:8]
0x518D	RAW_BIN_1315_D2V2_TOP_D	–	R	Bit[7:0]: RAW BIN version[7:0]

6.39 BINC_L [0x51B0 - 0x51C7]

table 6-39 BINC_L registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x51B0	BINC_1215_D2V2_0	0x10	RW	Bit[7:6]: Not used Bit[5]: m_bEnableHCorrection Range is [0:1] Bit[4]: m_bEnableVCorrection Range is [0:1] Bit[3]: m_bHDRBin_RGBIr Range is [0:1] Bit[2]: m_bIndex_manual Range is [0:1] Bit[1]: m_nFlip_manual Range is [0:1] Bit[0]: m_nMirror_manual Range is [0:1]
0x51B1	BINC_1215_D2V2_1	0x0E	RW	Bit[7:6]: Not used Bit[5:4]: m_nVIndex[1:0] Bit[3:0]: m_nHIndex[3:0]
0x51B2	BINC_1215_D2V2_2	0x0E	RW	Bit[7:4]: m_nVIndex_manual[3:0] Bit[3:0]: m_nHIndex_manual[3:0]
0x51B3	BINC_1215_D2V2_3	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_pFilterV[0][4:0] Range is [0:31]
0x51B4	NOT USED	–	–	Not Used
0x51B5	BINC_1215_D2V2_5	0x02	RW	Bit[7:5]: Not used Bit[4:0]: m_pFilterV[1][4:0] Range is [0:31]
0x51B6	BINC_1215_D2V2_6	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[0][8] Range is [-256:255]
0x51B7	BINC_1215_D2V2_7	0x00	RW	Bit[7:0]: m_pFilterH[0][7:0] Range is [-256:255]
0x51B8	BINC_1215_D2V2_8	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[1][8] Range is [-256:255]
0x51B9	BINC_1215_D2V2_9	0x70	RW	Bit[7:0]: m_pFilterH[1][7:0] Range is [-256:255]
0x51BA	BINC_1215_D2V2_A	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[2][8] Range is [-256:255]

table 6-39 BINC_L registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x51BB	BINC_1215_D2V2_B	0x10	RW	Bit[7:0]: m_pFilterH[2][7:0] Range is [-256:255]
0x51BC	BINC_1215_D2V2_C	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[3][8] Range is [-256:255]
0x51BD	BINC_1215_D2V2_D	0x00	RW	Bit[7:0]: m_pFilterH[3][7:0] Range is [-256:255]
0x51BE~ 0x51C6	RSVD	–	–	Reserved
0x51C7	BINC_1215_D2V2_17	0x10	RW	Bit[7:5]: Reserved Bit[4]: snr_flip_sel Bit[3]: Reserved Bit[2]: clk_gate_disable_man for buffer Bit[1]: Reserved Bit[0]: clk_gate_disable_man for process[3:0]

6.40 PDF_L [0x51D0 - 0x521B]

table 6-40 PDF_L registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x51D0	PDF_3245_D2V2_TOP_0	0xC2	RW	Bit[7]: Use chromatic information enable Bit[6]: Enable PD correction or not Range is [0:1] Bit[5]: Enable single defect pixel removal Range is [0:1] Bit[4]: Rb adaptive correction enable Range is [0:1] Bit[3]: G adaptive correction enable Range is [0:1] Bit[2]: Use corner information enable Range is [0:1] Bit[1]: Use chromatic information enable Range is [0:1] Bit[0]: Is ML 2x2 pattern or not Range is [0:1]

table 6-40 PDF_L registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x51D1	PDF_3245_D2V2_TOP_1	0x08	RW	Bit[7]: Not used Bit[6]: Skip PD on B Bit[5]: Skip PD on G Bit[4:0]: Weight C Range is [0:16]
0x51D2	PDF_3245_D2V2_TOP_2	0x84	RW	Bit[7]: Control every PD and shadow Range is [0:1] Bit[6]: Control every PD and shadow Range is [0:1] Bit[5]: Control every PD and shadow Range is [0:1] Bit[4]: Control every PD and shadow Range is [0:1] Bit[3]: Control every PD and shadow Range is [0:1] Bit[2]: Control every PD and shadow Range is [0:1] Bit[1]: Control every PD and shadow Range is [0:1] Bit[0]: Control every PD and shadow Range is [0:1]
0x51D3	PDF_3245_D2V2_TOP_3	0x04	RW	Bit[7:5]: Not used Bit[4]: Control every PD and shadow Range is [0:1] Bit[3]: Control every PD and shadow Range is [0:1] Bit[2:1]: Direction based method PD correction method enable Range is [0:2] Bit[0]: m_bPDDebugMode_ Range is [0:1]
0x51D4	PDF_3245_D2V2_TOP_4	0x00	RW	Bit[7]: Enable PD/shadow ext or not Range is [0:1] Bit[6]: Enable PD/shadow ext or not Range is [0:1] Bit[5]: Enable PD/shadow ext or not Range is [0:1] Bit[4]: Enable PD/shadow ext or not Range is [0:1] Bit[3]: Enable PD/shadow ext or not Range is [0:1] Bit[2]: Enable PD/shadow ext or not Range is [0:1] Bit[1]: Enable PD/shadow ext or not Range is [0:1] Bit[0]: Enable PD/shadow ext or not Range is [0:1]

table 6-40 PDF_L registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x51D5	PDF_3245_D2V2_TOP_5	0x02	RW	Bit[7]: Enable PD/shadow ext or not Range is [0:1] Bit[6]: Enable PD/shadow ext or not Range is [0:1] Bit[5:4]: G diag option Range is [0:3] Bit[3]: Single defect pixel removal option Range is [0:1] Bit[2:0]: Single defect pixel removal shift bit Range is [0:7]
0x51D6	PDF_3245_D2V2_TOP_6	0x04	RW	Bit[7:0]: Single defect pixel threshold Range is [0:255]
0x51D7	PDF_3245_D2V2_TOP_7	0x11	RW	Bit[7:6]: m_ nDirWeightScaleBit Range is [0:3] Bit[5:4]: m_nDirWeightCurveNum Range is [0:3] Bit[3:2]: m_nBilWeightScaleBit Range is [0:3] Bit[1:0]: m_nBilWeightCurveNum Range is [0:3]
0x51D8	PDF_3245_D2V2_TOP_8	0x08	RW	Bit[7:6]: Not used Bit[5:0]: PD X cycle Range is [1:64]
0x51D9	PDF_3245_D2V2_TOP_9	0x10	RW	Bit[7:6]: Not used Bit[5:0]: PD Y cycle Range is [1:64]
0x51DA	PDF_3245_D2V2_TOP_A	0x02	RW	Bit[7:5]: Not used Bit[4:0]: PD X1 start Range is [0:31]
0x51DB	PDF_3245_D2V2_TOP_B	0x02	RW	Bit[7:5]: Not used Bit[4:0]: PD X2 start Range is [0:31]
0x51DC	PDF_3245_D2V2_TOP_C	0x06	RW	Bit[7:5]: Not used Bit[4:0]: PD X3 start Range is [0:31]
0x51DD	PDF_3245_D2V2_TOP_D	0x06	RW	Bit[7:5]: Not used Bit[4:0]: PD X4 start Range is [0:31]
0x51DE	PDF_3245_D2V2_TOP_E	0x02	RW	Bit[7:5]: Not used Bit[4:0]: PD Y1 start Range is [0:31]

table 6-40 PDF_L registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x51DF	PDF_3245_D2V2_TOP_F	0x06	RW	Bit[7:5]: Not used Bit[4:0]: PD Y2 start Range is [0:31]
0x51E0	PDF_3245_D2V2_TOP_10	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: PD Y3 start Range is [0:31]
0x51E1	PDF_3245_D2V2_TOP_11	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: PD Y4 start Range is [0:31]
0x51E2	PDF_3245_D2V2_TOP_12	0x00	RW	Bit[7:5]: Not used Bit[4:0]: PD X skip Range is [0:31]
0x51E3	PDF_3245_D2V2_TOP_13	0x00	RW	Bit[7:5]: Not used Bit[4:0]: PD Y skip Range is [0:31]
0x51E4	PDF_3245_D2V2_TOP_14	0xFF	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51E5	PDF_3245_D2V2_TOP_15	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51E6	PDF_3245_D2V2_TOP_16	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51E7	PDF_3245_D2V2_TOP_17	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51E8	PDF_3245_D2V2_TOP_18	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51E9	PDF_3245_D2V2_TOP_19	0xFF	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51EA	PDF_3245_D2V2_TOP_1A	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51EB	PDF_3245_D2V2_TOP_1B	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51EC	PDF_3245_D2V2_TOP_1C	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51ED	PDF_3245_D2V2_TOP_1D	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x51EE	PDF_3245_D2V2_TOP_1E	0x00	RW	Bit[7:0]: 1x noise level for PD correction Range is [0:255]
0x51EF	PDF_3245_D2V2_TOP_1F	0x00	RW	Bit[7:0]: 4x noise level for PD correction Range is [0:255]

table 6-40 PDF_L registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x51F0	PDF_3245_D2V2_TOP_20	0x00	RW	Bit[7:0]: 8x noise level for PD correction Range is [0:255]
0x51F1	PDF_3245_D2V2_TOP_21	0xAA	RW	Bit[7:6]: PD ch 1 Range is [0:3] Bit[5:4]: PD ch 2 Range is [0:3] Bit[3:2]: PD ch 3 Range is [0:3] Bit[1:0]: PD ch 4 Range is [0:3]
0x51F2	PDF_3245_D2V2_TOP_22	0x80	RW	Bit[7:0]: PD adaptive strength low threshold 1x Range is [0:255]
0x51F3	PDF_3245_D2V2_TOP_23	0x80	RW	Bit[7:0]: PD adaptive strength low threshold 4x Range is [0:255]
0x51F4	PDF_3245_D2V2_TOP_24	0x80	RW	Bit[7:0]: PD adaptive strength low threshold 8x Range is [0:255]
0x51F5	PDF_3245_D2V2_TOP_25	0xFF	RW	Bit[7:0]: PD adaptive strength high threshold 1x Range is [0:255]
0x51F6	PDF_3245_D2V2_TOP_26	0xFF	RW	Bit[7:0]: PD adaptive strength high threshold 8x Range is [0:255]
0x51F7	PDF_3245_D2V2_TOP_27	0xFF	RW	Bit[7:0]: PD adaptive strength high threshold 8x Range is [0:255]
0x51F8	PDF_3245_D2V2_TOP_28	0x0A	RW	Bit[7:0]: Shadow edge threshold low 1x Range is [0:255]
0x51F9	PDF_3245_D2V2_TOP_29	0x0A	RW	Bit[7:0]: Shadow edge threshold low 4x Range is [0:255]
0x51FA	PDF_3245_D2V2_TOP_2A	0x0A	RW	Bit[7:0]: Shadow edge threshold low 8x Range is [0:255]
0x51FB	PDF_3245_D2V2_TOP_2B	0x14	RW	Bit[7:0]: Shadow edge threshold high 1x Range is [0:255]
0x51FC	PDF_3245_D2V2_TOP_2C	0x14	RW	Bit[7:0]: Shadow edge threshold high 4x Range is [0:255]
0x51FD	PDF_3245_D2V2_TOP_2D	0x14	RW	Bit[7:0]: Shadow edge threshold high 8x Range is [0:255]
0x51FE	PDF_3245_D2V2_TOP_2E	0x00	RW	Bit[7:0]: Flat threshold Range is [0:255]
0x51FF	PDF_3245_D2V2_TOP_2F	0x00	RW	Bit[7:0]: Inte threshold Range is [0:255]

table 6-40 PDF_L registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x5200	PDF_3245_D2V2_TOP_30	0x12	RW	Bit[7:6]: Not used Bit[5:0]: Image width[13:8] Range is [0:16383]
0x5201	PDF_3245_D2V2_TOP_31	0x20	RW	Bit[7:0]: Image width[7:0] Range is [0:16383]
0x5202	PDF_3245_D2V2_TOP_32	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: Image height[12:8] Range is [0:8191]
0x5203	PDF_3245_D2V2_TOP_33	0xA0	RW	Bit[7:0]: Image height[7:0] Range is [0:8191]
0x5204	PDF_3245_D2V2_TOP_34	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Window start X[13:8] Range is [0:16383]
0x5205	PDF_3245_D2V2_TOP_35	0x10	RW	Bit[7:0]: Window start X[7:0] Range is [0:16383]
0x5206	PDF_3245_D2V2_TOP_36	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Window start Y[12:8] Range is [0:8191]
0x5207	PDF_3245_D2V2_TOP_37	0x10	RW	Bit[7:0]: Window start Y[7:0] Range is [0:8191]
0x5208	PDF_3245_D2V2_TOP_38	0x12	RW	Bit[7:6]: Not used Bit[5:0]: Window width[13:8] Range is [0:16383]
0x5209	PDF_3245_D2V2_TOP_39	0x00	RW	Bit[7:0]: Window width[7:0] Range is [0:16383]
0x520A	PDF_3245_D2V2_TOP_3A	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: Window height[12:8] Range is [0:8191]
0x520B	PDF_3245_D2V2_TOP_3B	0x80	RW	Bit[7:0]: Window height[7:0] Range is [0:8191]
0x520C	PDF_3245_D2V2_TOP_3C	0x00	RW	Bit[7:6]: Not used Bit[5]: vcnt_out_en Bit[4]: hcnt_out_en Bit[3]: cnt_output_en Bit[2]: engine2_off_en Bit[1]: fix_ptn_mode Bit[0]: fix_ptn_en

table 6-40 PDF_L registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x520D	PDF_3245_D2V2_TOP_3D	0x08	RW	Bit[7:4]: Not used Bit[3]: pd_cnt_clr_man_en Bit[2]: pd_win_man_en Bit[1]: xoffset_man_en Bit[0]: yoffset_man_en
0x520E	PDF_3245_D2V2_TOP_3E	0x00	RW	Bit[7:0]: r_gate_dis[7:0]
0x520F	PDF_3245_D2V2_TOP_3F	0x00	RW	Bit[7:0]: r_gate_dis[15:8]
0x5210	PDF_3245_D2V2_TOP_40	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Xoffset[13:8] Range is [0:16383]
0x5211	PDF_3245_D2V2_TOP_41	0x00	RW	Bit[7:0]: Xoffset[7:0] Range is [0:16383]
0x5212	PDF_3245_D2V2_TOP_42	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Yoffset[12:8] Range is [0:8191]
0x5213	PDF_3245_D2V2_TOP_43	0x00	RW	Bit[7:0]: Yoffset[7:0] Range is [0:8191]
0x5214	PDF_3245_D2V2_TOP_44	0x00	RW	Bit[7:4]: Not used Bit[3:0]: offset_c Range is [0:15]
0x5215	PDF_3245_D2V2_TOP_45	0x05	RW	Bit[7:5]: Not used Bit[4]: PDswitch Range is [0:1] Bit[3]: median_option Range is [0:1] Bit[2:0]: DirWeightCurveNumSquare Range is [0:3]
0x5216	PDF_3245_D2V2_TOP_46	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Xoffset1[13:8] Range is [0:16383]
0x5217	PDF_3245_D2V2_TOP_47	0x00	RW	Bit[7:0]: Xoffset1[7:0] Range is [0:16383]
0x5218~ 0x5219	NOT USED	–	–	Not Used
0x521A	PDF_3245_D2V2_TOP_4A	–	R	Bit[7:0]: Version[15:8]
0x521B	PDF_3245_D2V2_TOP_4B	–	R	Bit[7:0]: Version[7:0]

6.41 PDC_L [0x5250 - 0x534C]

table 6-41 PDC_L registers (sheet 1 of 11)

address	register name	default value	R/W	description
0x5250	PDC_3245_D2V2_TOP_0	0x6C	RW	Bit[7:6]: Not used Bit[5]: m_bML2x2HS Bit[4]: m_bByPassHighComp Bit[3]: m_nPDDOption Bit[2]: m_nEnablePreCompensate Bit[1]: m_nBypassPDCompensation Bit[0]: pdc_map_en
0x5251	PDC_3245_D2V2_TOP_1	0x00	RW	Bit[7:3]: Not used Bit[2]: m_bCurveFlip Bit[1]: m_bCurveMirror Bit[0]: m_nBinCurveEnable
0x5252	PDC_3245_D2V2_TOP_2	0x00	RW	Bit[7]: man_focuswin_en Bit[6]: win_man_en Bit[5]: yoffset_man_en Bit[4]: xoffset_man_en Bit[3]: man_ml2x2ptn_en Bit[2]: man_flip_en Bit[1]: man_mirror_en Bit[0]: man_bin_en
0x5253	PDC_3245_D2V2_TOP_3	0x00	RW	Bit[7:2]: Not used Bit[1]: man_scaler_en Bit[0]: man_pd_location_en
0x5254	PDC_3245_D2V2_TOP_4	0x00	RW	Bit[7]: Not used Bit[6]: man_ml2x2pattern Bit[5]: man_flip Bit[4]: man_mirror Bit[3:2]: Not used Bit[1]: man_vbin Bit[0]: man_hbin
0x5255	NOT USED	–	–	Not Used
0x5256	PDC_3245_D2V2_TOP_6	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nOffsetX>>8[13:8]
0x5257	PDC_3245_D2V2_TOP_7	0x10	RW	Bit[7:0]: m_nOffsetX[7:0]
0x5258	PDC_3245_D2V2_TOP_8	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nOffsetY>>8[13:8]
0x5259	PDC_3245_D2V2_TOP_9	0x00	RW	Bit[7:0]: m_nOffsetY[7:0]
0x525A	PDC_3245_D2V2_TOP_A	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinXStart>>8[13:8]

table 6-41 PDC_L registers (sheet 2 of 11)

address	register name	default value	R/W	description
0x525B	PDC_3245_D2V2_TOP_B	0x00	RW	Bit[7:0]: m_nWinXStart[7:0]
0x525C	PDC_3245_D2V2_TOP_C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinYStart>>8[13:8]
0x525D	PDC_3245_D2V2_TOP_D	0x00	RW	Bit[7:0]: m_nWinYStart[7:0]
0x525E	PDC_3245_D2V2_TOP_E	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinWidth>>8[13:8]
0x525F	PDC_3245_D2V2_TOP_F	0x80	RW	Bit[7:0]: m_nWinWidth[7:0]
0x5260	PDC_3245_D2V2_TOP_10	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinHeight>>8[13:8]
0x5261	PDC_3245_D2V2_TOP_11	0xA0	RW	Bit[7:0]: m_nWinHeight[7:0]
0x5262	PDC_3245_D2V2_TOP_12	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinLeft>>8[13:8]
0x5263	PDC_3245_D2V2_TOP_13	0x00	RW	Bit[7:0]: m_nFocusWinLeft[7:0]
0x5264	PDC_3245_D2V2_TOP_14	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinTop>>8[13:8]
0x5265	PDC_3245_D2V2_TOP_15	0x00	RW	Bit[7:0]: m_nFocusWinTop[7:0]
0x5266	PDC_3245_D2V2_TOP_16	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinWidth>>8[13:8]
0x5267	PDC_3245_D2V2_TOP_17	0x80	RW	Bit[7:0]: m_nFocusWinWidth[7:0]
0x5268	PDC_3245_D2V2_TOP_18	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinHeight>>8[13:8]
0x5269	PDC_3245_D2V2_TOP_19	0xA0	RW	Bit[7:0]: m_nFocusWinHeight[7:0]
0x526A	PDC_3245_D2V2_TOP_1A	0x10	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDCycleX[5:0]
0x526B	PDC_3245_D2V2_TOP_1B	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDCycleY[5:0]
0x526C	PDC_3245_D2V2_TOP_1C	0x01	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDSkipX[4:0]
0x526D	PDC_3245_D2V2_TOP_1D	0x01	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDSkipY[4:0]
0x526E	PDC_3245_D2V2_TOP_1E	0x04	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX1[4:0]
0x526F	PDC_3245_D2V2_TOP_1F	0x04	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX2[4:0]

table 6-41 PDC_L registers (sheet 3 of 11)

address	register name	default value	R/W	description
0x5270	PDC_3245_D2V2_TOP_20	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX3[4:0]
0x5271	PDC_3245_D2V2_TOP_21	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX4[4:0]
0x5272	PDC_3245_D2V2_TOP_22	0x04	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY1[4:0]
0x5273	PDC_3245_D2V2_TOP_23	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY2[4:0]
0x5274	PDC_3245_D2V2_TOP_24	0x14	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY3[4:0]
0x5275	PDC_3245_D2V2_TOP_25	0x1C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY4[4:0]
0x5276	PDC_3245_D2V2_TOP_26	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh1
0x5277	PDC_3245_D2V2_TOP_27	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh2
0x5278	PDC_3245_D2V2_TOP_28	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh3
0x5279	PDC_3245_D2V2_TOP_29	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh4
0x527A	PDC_3245_D2V2_TOP_2A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDFadingScalerH>>8[9:8]
0x527B	PDC_3245_D2V2_TOP_2B	0x40	RW	Bit[7:0]: m_nPDFadingScalerH[7:0]
0x527C	PDC_3245_D2V2_TOP_2C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDFadingScalerV>>8[9:8]
0x527D	PDC_3245_D2V2_TOP_2D	0x56	RW	Bit[7:0]: m_nPDFadingScalerV[7:0]
0x527E	PDC_3245_D2V2_TOP_2E	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nBinNumA[3:0]
0x527F	PDC_3245_D2V2_TOP_2F	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nBinNumB[3:0]
0x5280	PDC_3245_D2V2_TOP_30	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDWidth_ori>>8[13:8]
0x5281	PDC_3245_D2V2_TOP_31	0x80	RW	Bit[7:0]: m_nPDWidth_ori[7:0]
0x5282	PDC_3245_D2V2_TOP_32	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDHeight_ori>>8[13:8]
0x5283	PDC_3245_D2V2_TOP_33	0xA0	RW	Bit[7:0]: m_nPDHeight_ori[7:0]

table 6-41 PDC_L registers (sheet 4 of 11)

address	register name	default value	R/W	description
0x5284	PDC_3245_D2V2_TOP_34	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nArrayWidth>>8[13:8]
0x5285	PDC_3245_D2V2_TOP_35	0x80	RW	Bit[7:0]: m_nArrayWidth[7:0]
0x5286	PDC_3245_D2V2_TOP_36	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nArrayHeight>>8[13:8]
0x5287	PDC_3245_D2V2_TOP_37	0xA0	RW	Bit[7:0]: m_nArrayHeight[7:0]
0x5288	PDC_3245_D2V2_TOP_38	0x0F	RW	Bit[7:6]: Not used Bit[5:0]: m_nOffsetX>>8[13:8]
0x5289	PDC_3245_D2V2_TOP_39	0xB8	RW	Bit[7:0]: m_nOffsetX[7:0]
0x528A	PDC_3245_D2V2_TOP_3A	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinLeft>>8[13:8]
0x528B	PDC_3245_D2V2_TOP_3B	0x00	RW	Bit[7:0]: m_nFocusWinLeft[7:0]
0x528C	PDC_3245_D2V2_TOP_3C	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinWidth>>8[13:8]
0x528D	PDC_3245_D2V2_TOP_3D	0x80	RW	Bit[7:0]: m_nFocusWinWidth[7:0]
0x528E~ 0x528F	NOT USED	–	–	Not Used
0x5290	PDC_3245_D2V2_TOP_40	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[0]>>8[15:8]
0x5291	PDC_3245_D2V2_TOP_41	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[0][7:0]
0x5292	PDC_3245_D2V2_TOP_42	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[1]>>8[15:8]
0x5293	PDC_3245_D2V2_TOP_43	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[1][7:0]
0x5294	PDC_3245_D2V2_TOP_44	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[2]>>8[15:8]
0x5295	PDC_3245_D2V2_TOP_45	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[2][7:0]
0x5296	PDC_3245_D2V2_TOP_46	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[3]>>8[15:8]
0x5297	PDC_3245_D2V2_TOP_47	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[3][7:0]
0x5298	PDC_3245_D2V2_TOP_48	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[4]>>8[15:8]
0x5299	PDC_3245_D2V2_TOP_49	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[4][7:0]
0x529A	PDC_3245_D2V2_TOP_4A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[5]>>8[15:8]
0x529B	PDC_3245_D2V2_TOP_4B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[5][7:0]
0x529C	PDC_3245_D2V2_TOP_4C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[6]>>8[15:8]
0x529D	PDC_3245_D2V2_TOP_4D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[6][7:0]
0x529E	PDC_3245_D2V2_TOP_4E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[7]>>8[15:8]

table 6-41 PDC_L registers (sheet 5 of 11)

address	register name	default value	R/W	description
0x529F	PDC_3245_D2V2_TOP_4F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[7][7:0]
0x52A0	PDC_3245_D2V2_TOP_50	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[8]>>8[15:8]
0x52A1	PDC_3245_D2V2_TOP_51	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[8][7:0]
0x52A2	PDC_3245_D2V2_TOP_52	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[9]>>8[15:8]
0x52A3	PDC_3245_D2V2_TOP_53	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[9][7:0]
0x52A4	PDC_3245_D2V2_TOP_54	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[10]>>8[15:8]
0x52A5	PDC_3245_D2V2_TOP_55	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[10][7:0]
0x52A6	PDC_3245_D2V2_TOP_56	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[11]>>8[15:8]
0x52A7	PDC_3245_D2V2_TOP_57	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[11][7:0]
0x52A8	PDC_3245_D2V2_TOP_58	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[12]>>8[15:8]
0x52A9	PDC_3245_D2V2_TOP_59	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[12][7:0]
0x52AA	PDC_3245_D2V2_TOP_5A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[13]>>8[15:8]
0x52AB	PDC_3245_D2V2_TOP_5B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[13][7:0]
0x52AC	PDC_3245_D2V2_TOP_5C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[14]>>8[15:8]
0x52AD	PDC_3245_D2V2_TOP_5D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[14][7:0]
0x52AE	PDC_3245_D2V2_TOP_5E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[15]>>8[15:8]
0x52AF	PDC_3245_D2V2_TOP_5F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[15][7:0]
0x52B0	PDC_3245_D2V2_TOP_60	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[16]>>8[15:8]
0x52B1	PDC_3245_D2V2_TOP_61	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[16][7:0]
0x52B2	PDC_3245_D2V2_TOP_62	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[17]>>8[15:8]
0x52B3	PDC_3245_D2V2_TOP_63	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[17][7:0]
0x52B4	PDC_3245_D2V2_TOP_64	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[18]>>8[15:8]
0x52B5	PDC_3245_D2V2_TOP_65	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[18][7:0]
0x52B6	PDC_3245_D2V2_TOP_66	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[19]>>8[15:8]
0x52B7	PDC_3245_D2V2_TOP_67	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[19][7:0]
0x52B8	PDC_3245_D2V2_TOP_68	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[20]>>8[15:8]
0x52B9	PDC_3245_D2V2_TOP_69	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[20][7:0]
0x52BA	PDC_3245_D2V2_TOP_6A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[21]>>8[15:8]
0x52BB	PDC_3245_D2V2_TOP_6B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[21][7:0]
0x52BC	PDC_3245_D2V2_TOP_6C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[22]>>8[15:8]

table 6-41 PDC_L registers (sheet 6 of 11)

address	register name	default value	R/W	description
0x52BD	PDC_3245_D2V2_TOP_6D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[22][7:0]
0x52BE	PDC_3245_D2V2_TOP_6E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[23]>>8[15:8]
0x52BF	PDC_3245_D2V2_TOP_6F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[23][7:0]
0x52C0	PDC_3245_D2V2_TOP_70	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[24]>>8[15:8]
0x52C1	PDC_3245_D2V2_TOP_71	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[24][7:0]
0x52C2	PDC_3245_D2V2_TOP_72	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[25]>>8[15:8]
0x52C3	PDC_3245_D2V2_TOP_73	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[25][7:0]
0x52C4	PDC_3245_D2V2_TOP_74	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[26]>>8[15:8]
0x52C5	PDC_3245_D2V2_TOP_75	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[26][7:0]
0x52C6	PDC_3245_D2V2_TOP_76	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[27]>>8[15:8]
0x52C7	PDC_3245_D2V2_TOP_77	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[27][7:0]
0x52C8	PDC_3245_D2V2_TOP_78	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[28]>>8[15:8]
0x52C9	PDC_3245_D2V2_TOP_79	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[28][7:0]
0x52CA	PDC_3245_D2V2_TOP_7A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[29]>>8[15:8]
0x52CB	PDC_3245_D2V2_TOP_7B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[29][7:0]
0x52CC	PDC_3245_D2V2_TOP_7C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[30]>>8[15:8]
0x52CD	PDC_3245_D2V2_TOP_7D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[30][7:0]
0x52CE	PDC_3245_D2V2_TOP_7E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[31]>>8[15:8]
0x52CF	PDC_3245_D2V2_TOP_7F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[31][7:0]
0x52D0	PDC_3245_D2V2_TOP_80	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[0][5:0]
0x52D1	PDC_3245_D2V2_TOP_81	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[1][5:0]
0x52D2	PDC_3245_D2V2_TOP_82	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[2][5:0]
0x52D3	PDC_3245_D2V2_TOP_83	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[3][5:0]
0x52D4	PDC_3245_D2V2_TOP_84	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[4][5:0]
0x52D5	PDC_3245_D2V2_TOP_85	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[5][5:0]
0x52D6	PDC_3245_D2V2_TOP_86	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[6][5:0]

table 6-41 PDC_L registers (sheet 7 of 11)

address	register name	default value	R/W	description
0x52D7	PDC_3245_D2V2_TOP_87	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[7][5:0]
0x52D8	PDC_3245_D2V2_TOP_88	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[8][5:0]
0x52D9	PDC_3245_D2V2_TOP_89	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[9][5:0]
0x52DA	PDC_3245_D2V2_TOP_8A	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[10][5:0]
0x52DB	PDC_3245_D2V2_TOP_8B	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[11][5:0]
0x52DC	PDC_3245_D2V2_TOP_8C	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[12][5:0]
0x52DD	PDC_3245_D2V2_TOP_8D	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[13][5:0]
0x52DE	PDC_3245_D2V2_TOP_8E	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[14][5:0]
0x52DF	PDC_3245_D2V2_TOP_8F	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[15][5:0]
0x52E0	PDC_3245_D2V2_TOP_90	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[16][5:0]
0x52E1	PDC_3245_D2V2_TOP_91	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[17][5:0]
0x52E2	PDC_3245_D2V2_TOP_92	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[18][5:0]
0x52E3	PDC_3245_D2V2_TOP_93	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[19][5:0]
0x52E4	PDC_3245_D2V2_TOP_94	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[20][5:0]
0x52E5	PDC_3245_D2V2_TOP_95	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[21][5:0]
0x52E6	PDC_3245_D2V2_TOP_96	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[22][5:0]
0x52E7	PDC_3245_D2V2_TOP_97	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[23][5:0]
0x52E8	PDC_3245_D2V2_TOP_98	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[24][5:0]
0x52E9	PDC_3245_D2V2_TOP_99	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[25][5:0]

table 6-41 PDC_L registers (sheet 8 of 11)

address	register name	default value	R/W	description
0x52EA	PDC_3245_D2V2_TOP_9A	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[26][5:0]
0x52EB	PDC_3245_D2V2_TOP_9B	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[27][5:0]
0x52EC	PDC_3245_D2V2_TOP_9C	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[28][5:0]
0x52ED	PDC_3245_D2V2_TOP_9D	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[29][5:0]
0x52EE	PDC_3245_D2V2_TOP_9E	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[30][5:0]
0x52EF	PDC_3245_D2V2_TOP_9F	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[31][5:0]
0x52F0	PDC_3245_D2V2_TOP_A0	0x01	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[0][5:0]
0x52F1	PDC_3245_D2V2_TOP_A1	0x02	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[1][5:0]
0x52F2	PDC_3245_D2V2_TOP_A2	0x03	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[2][5:0]
0x52F3	PDC_3245_D2V2_TOP_A3	0x04	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[3][5:0]
0x52F4	PDC_3245_D2V2_TOP_A4	0x05	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[4][5:0]
0x52F5	PDC_3245_D2V2_TOP_A5	0x06	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[5][5:0]
0x52F6	PDC_3245_D2V2_TOP_A6	0x07	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[6][5:0]
0x52F7	PDC_3245_D2V2_TOP_A7	0x08	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[7][5:0]
0x52F8	PDC_3245_D2V2_TOP_A8	0x09	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[8][5:0]
0x52F9	PDC_3245_D2V2_TOP_A9	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[9][5:0]
0x52FA	PDC_3245_D2V2_TOP_AA	0x0B	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[10][5:0]
0x52FB	PDC_3245_D2V2_TOP_AB	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[11][5:0]
0x52FC	PDC_3245_D2V2_TOP_AC	0x0D	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[12][5:0]

table 6-41 PDC_L registers (sheet 9 of 11)

address	register name	default value	R/W	description
0x52FD	PDC_3245_D2V2_TOP_AD	0x0E	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[13][5:0]
0x52FE	PDC_3245_D2V2_TOP_AE	0x0F	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[14][5:0]
0x52FF	PDC_3245_D2V2_TOP_AF	0x10	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[15][5:0]
0x5300	PDC_3245_D2V2_TOP_B0	0x11	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[16][5:0]
0x5301	PDC_3245_D2V2_TOP_B1	0x12	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[17][5:0]
0x5302	PDC_3245_D2V2_TOP_B2	0x13	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[18][5:0]
0x5303	PDC_3245_D2V2_TOP_B3	0x14	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[19][5:0]
0x5304	PDC_3245_D2V2_TOP_B4	0x15	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[20][5:0]
0x5305	PDC_3245_D2V2_TOP_B5	0x16	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[21][5:0]
0x5306	PDC_3245_D2V2_TOP_B6	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[22][5:0]
0x5307	PDC_3245_D2V2_TOP_B7	0x18	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[23][5:0]
0x5308	PDC_3245_D2V2_TOP_B8	0x19	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[24][5:0]
0x5309	PDC_3245_D2V2_TOP_B9	0x1A	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[25][5:0]
0x530A	PDC_3245_D2V2_TOP_BA	0x1B	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[26][5:0]
0x530B	PDC_3245_D2V2_TOP_BB	0x1C	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[27][5:0]
0x530C	PDC_3245_D2V2_TOP_BC	0x1D	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[28][5:0]
0x530D	PDC_3245_D2V2_TOP_BD	0x1E	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[29][5:0]
0x530E	PDC_3245_D2V2_TOP_BE	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[30][5:0]
0x530F	PDC_3245_D2V2_TOP_BF	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[31][5:0]

table 6-41 PDC_L registers (sheet 10 of 11)

address	register name	default value	R/W	description
0x5310	PDC_3245_D2V2_TOP_C0	0x03	RW	Bit[7:4]: Not used Bit[3:0]: m_nOverExpoThre>>8[11:8]
0x5311	PDC_3245_D2V2_TOP_C1	0xFF	RW	Bit[7:0]: m_nOverExpoThre[7:0]
0x5312	PDC_3245_D2V2_TOP_C2	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Calculate start select Bit[3:0]: Replace PD by column/row count in debug mode
0x5313	PDC_3245_D2V2_TOP_C3	0x01	RW	Bit[7:5]: Not used Bit[4]: Firmware write SRAM enable Bit[3:2]: Not used Bit[1:0]: Firmware read SRAM select 00: None 01: L 10: M 11: S
0x5314~ 0x532F	NOT USED	–	–	Not Used
0x5330	PDC_3245_D2V2_TOP_E0	0x00	RW	Bit[7:0]: PD restore control
0x5331	PDC_3245_D2V2_TOP_E1	0x02	RW	Bit[7:4]: Not used Bit[3]: m_bFourCell2PD Bit[2]: m_nPDOption Bit[1:0]: m_bMedianFilterOption
0x5332	PDC_3245_D2V2_TOP_E2	0x42	RW	Bit[7:4]: m_nMedianFilterPixel[0][3:0] Bit[3:0]: m_nMedianFilterPixel[1][3:0]
0x5333	PDC_3245_D2V2_TOP_E3	0x24	RW	Bit[7:4]: m_nMedianFilterPixel[2][3:0] Bit[3:0]: m_nMedianFilterPixel[3][3:0]
0x5334	PDC_3245_D2V2_TOP_E4	0x00	RW	Bit[7:5]: Not used Bit[4:2]: PD restore dbg_cnt_sel Bit[1:0]: PD restore dbg_byt_sel
0x5335	PDC_3245_D2V2_TOP_E5	0x01	RW	Bit[7:1]: Not used Bit[0]: BLC option enable
0x5336	PDC_3245_D2V2_TOP_E6	0x00	RW	Bit[7:0]: BLC reserved from 0~128
0x5337~ 0x533F	NOT USED	–	–	Not Used
0x5340	PDC_3245_D2V2_TOP_F0	–	R	Bit[7:0]: PDC version[15:8]
0x5341	PDC_3245_D2V2_TOP_F1	–	R	Bit[7:0]: PDC version[7:0]
0x5342~ 0x5344	NOT USED	–	–	Not Used
0x5345	PDC_3245_D2V2_TOP_F5	–	R	Bit[7:0]: PD counter[23:16]

table 6-41 PDC_L registers (sheet 11 of 11)

address	register name	default value	R/W	description
0x5346	PDC_3245_D2V2_TOP_F6	–	R	Bit[7:0]: PD counter[15:8]
0x5347	PDC_3245_D2V2_TOP_F7	–	R	Bit[7:0]: PD counter[7:0]
0x5349	PDC_3245_D2V2_TOP_F9	–	R	Bit[7:0]: PD counter[23:16]
0x534A	PDC_3245_D2V2_TOP_FA	–	R	Bit[7:0]: PD counter[15:8]
0x534B	PDC_3245_D2V2_TOP_FB	–	R	Bit[7:0]: PD counter[7:0]
0x534C	PDC_3245_D2V2_TOP_FC	–	R	Bit[7:0]: PD restore PD VC counter

6.42 RAW_DNS_L [0x5350 - 0x535F]

table 6-42 RAW_DNS_L registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5350~ 0x5352	NOT USED	–	–	Not Used
0x5353	RAW_DNS_1055_3	0x05	RW	Bit[7:5]: Reserved Bit[4]: dns_para_man_en Bit[3]: dns_mode Bit[2]: avg_dis_1 Range is [0:1] Bit[1]: avg_dis_0 Range is [0:1] Bit[0]: g_dns_en Range is [0:1]
0x5354	RAW_DNS_1055_4	0x04	RW	Bit[7:0]: dns_noise_list_0 Range is [0:7]
0x5355	RAW_DNS_1055_5	0x08	RW	Bit[7:0]: dns_noise_list_1 Range is [8:15]
0x5356	RAW_DNS_1055_6	0x10	RW	Bit[7:0]: dns_noise_list_2 Range is [16:31]
0x5357	RAW_DNS_1055_7	0x18	RW	Bit[7:0]: dns_noise_list_3 Range is [32:63]
0x5358	RAW_DNS_1055_8	0x20	RW	Bit[7:0]: dns_noise_list_4 Range is [64:95]
0x5359	RAW_DNS_1055_9	0x30	RW	Bit[7:0]: dns_noise_list_5 Range is [96:127]

table 6-42 RAW_DNS_L registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x535A	RAW_DNS_1055_A	0x40	RW	Bit[7:0]: dns_noise_list_6 Range is [128:191]
0x535B	RAW_DNS_1055_B	0x40	RW	Bit[7:0]: dns_noise_list_7 Range is [192:255]
0x535C~ 0x535E	RSVD	–	–	Reserved
0x535F	RAW_DNS_1055_F	0x08	RW	Bit[7:0]: dns_noise_man

6.43 PRE_ISP_M [0x53C0 - 0x53E7]

table 6-43 PRE_ISP_M registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x53C0	PRE_ISP_2325_D2V2_TOP_0	0x00	RW	Bit[7:5]: Not used Bit[4]: Disable clock gating Range is [0:1] Bit[3]: Reserved Bit[2]: Manual size enable Range is [0:1] Bit[1]: Manual end address enable Range is [0:1] Bit[0]: Manual offset (start address) enable Range is [0:1]
0x53C1	PRE_ISP_2325_D2V2_TOP_1	0x00	RW	Bit[7]: Flip option Range is [0:1] Bit[6]: Mirror option Range is [0:1] Bit[5:4]: Color bar option Range is [0:3] Bit[3]: Transparent mode enable Range is [0:1] Bit[2]: Rolling mode enable Range is [0:1] Bit[1]: Clear last four bits enable Range is [0:1] Bit[0]: Test pattern enable Range is [0:1]
0x53C2	PRE_ISP_2325_D2V2_TOP_2	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Test pattern mode Range is [0:7]

table 6-43 PRE_ISP_M registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x53C3	RSVD	–	–	Reserved
0x53C4	PRE_ISP_2325_D2V2_TOP_4	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Manual width[13:8] Range is [0:4704]
0x53C5	PRE_ISP_2325_D2V2_TOP_5	0x80	RW	Bit[7:0]: Manual width[7:0] Range is [0:4704]
0x53C6	PRE_ISP_2325_D2V2_TOP_6	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual height[12:8] Range is [0:3536]
0x53C7	PRE_ISP_2325_D2V2_TOP_7	0xE0	RW	Bit[7:0]: Manual height[7:0] Range is [0:3536]
0x53C8	PRE_ISP_2325_D2V2_TOP_8	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Manual X offset[13:8] Range is [0:4704]
0x53C9	PRE_ISP_2325_D2V2_TOP_9	0x00	RW	Bit[7:0]: Manual X offset[7:0] Range is [0:4704]
0x53CA	PRE_ISP_2325_D2V2_TOP_A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y offset[12:8] Range is [0:3536]
0x53CB	PRE_ISP_2325_D2V2_TOP_B	0x00	RW	Bit[7:0]: Manual Y offset[7:0] Range is [0:3536]
0x53CC	PRE_ISP_2325_D2V2_TOP_C	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Manual X end[13:8] Range is [0:4704]
0x53CD	PRE_ISP_2325_D2V2_TOP_D	0x80	RW	Bit[7:0]: Manual X end[7:0] Range is [0:4704]
0x53CE	PRE_ISP_2325_D2V2_TOP_E	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y end[12:8] Range is [0:3536]
0x53CF	PRE_ISP_2325_D2V2_TOP_F	0xE0	RW	Bit[7:0]: Manual Y end[7:0] Range is [0:3536]
0x53D0~ 0x53D1	NOT USED	–	–	Not Used
0x53D2	PRE_ISP_2325_D2V2_TOP_12	0x01	RW	Bit[7:5]: Not used Bit[4:0]: In_number[12:8] Range is [0:3536]
0x53D3	PRE_ISP_2325_D2V2_TOP_13	0xE0	RW	Bit[7:0]: In_number[7:0] Range is [0:3536]

table 6-43 PRE_ISP_M registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x53D4~ 0x53D7	NOT USED	–	–	Not Used
0x53D8	PRE_ISP_2325_D2V2_TOP_18	–	R	Bit[7:6]: Reserved Bit[5:0]: Pixel count[13:8] Range is [0:3536]
0x53D9	PRE_ISP_2325_D2V2_TOP_19	–	R	Bit[7:0]: Pixel count[7:0] Range is [0:3536]
0x53DA	PRE_ISP_2325_D2V2_TOP_1A	–	R	Bit[7:5]: Reserved Bit[4:0]: Line count[12:8] Range is [0:255]
0x53DB	PRE_ISP_2325_D2V2_TOP_1B	–	R	Bit[7:0]: Line count[7:0] Range is [0:255]
0x53DC	PRE_ISP_2325_D2V2_TOP_1C	–	R	Bit[7:0]: dbg_0 Range is [0:255]
0x53DD	PRE_ISP_2325_D2V2_TOP_1D	–	R	Bit[7:0]: dbg_1 Range is [0:255]
0x53DE	PRE_ISP_2325_D2V2_TOP_1E	–	R	Bit[7:0]: dbg_2 Range is [0:1]
0x53DF	PRE_ISP_2325_D2V2_TOP_1F	–	R	Bit[7:0]: dbg_3 Range is [0:8191]
0x53E0	PRE_ISP_2325_D2V2_TOP_20	–	R	Bit[7:6]: Reserved Bit[5:0]: x_offset[13:8] Range is [0:8191]
0x53E1	PRE_ISP_2325_D2V2_TOP_21	–	R	Bit[7:0]: x_offset[7:0] Range is [0:8191]
0x53E2	PRE_ISP_2325_D2V2_TOP_22	–	R	Bit[7:5]: Reserved Bit[4:0]: y_offset[12:8] Range is [0:4095]
0x53E3	PRE_ISP_2325_D2V2_TOP_23	–	R	Bit[7:0]: y_offset[7:0] Range is [0:4095]
0x53E4~ 0x53E5	NOT USED	–	–	Not Used
0x53E6	PRE_ISP_2325_D2V2_TOP_26	–	R	Bit[7:0]: Software version[15:8] Range is [0:255]
0x53E7	PRE_ISP_2325_D2V2_TOP_27	–	R	Bit[7:0]: Hardware version[7:0] Range is [0:255]

6.44 AWBG_M [0x53F0 - 0x5407]

table 6-44 AWBG_M registers

address	register name	default value	R/W	description
0x53F0	AWBG_24_0	0xEE	RW	Bit[7:0]: CFAY[31:24]
0x53F1	AWBG_24_1	0x44	RW	Bit[7:0]: CFAY[23:16]
0x53F2	AWBG_24_2	0xEE	RW	Bit[7:0]: CFAY[15:8]
0x53F3	AWBG_24_3	0x44	RW	Bit[7:0]: CFAY[7:0]
0x53F4	AWBG_24_4	0x00	RW	Bit[7:0]: gain_lat_sel[7:0]
0x53F5	AWBG_24_5	0x02	RW	Bit[7:4]: Not used Bit[3]: cfay_man_en Bit[2]: blc_man_en Bit[1:0]: mne[9:8]
0x53F6	AWBG_24_6	0x00	RW	Bit[7:0]: MNE[7:0]
0x53F7	AWBG_24_7	0x00	RW	Bit[7:0]: BLC
0x53F8~ 0x53FF	RSVD	–	–	Reserved
0x5400	AWBG_24_8	0x04	RW	Bit[7:0]: cfa_gain0[15:8]
0x5401	AWBG_24_9	0x00	RW	Bit[7:0]: cfa_gain0[7:0]
0x5402	AWBG_24_A	0x04	RW	Bit[7:0]: cfa_gain1[15:8]
0x5403	AWBG_24_B	0x00	RW	Bit[7:0]: cfa_gain1[7:0]
0x5404	AWBG_24_C	0x04	RW	Bit[7:0]: cfa_gain2[15:8]
0x5405	AWBG_24_D	0x00	RW	Bit[7:0]: cfa_gain2[7:0]
0x5406	AWBG_24_E	0x04	RW	Bit[7:0]: cfa_gain3[15:8]
0x5407	AWBG_24_F	0x00	RW	Bit[7:0]: cfa_gain3[7:0]

6.45 OTP_M [0x5410 - 0x5441]

table 6-45 OTP_M registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x5410	OTP_DPC_3615_D2V2_0	0x00	RW	Bit[7:0]: OTP eFUSE start address[15:8]
0x5411	OTP_DPC_3615_D2V2_1	0x00	RW	Bit[7:0]: OTP eFUSE start address[7:0]
0x5412	OTP_DPC_3615_D2V2_2	0xFF	RW	Bit[7:0]: OTP eFUSE end address[15:8]
0x5413	OTP_DPC_3615_D2V2_3	0xFF	RW	Bit[7:0]: OTP eFUSE end address[7:0]
0x5414	OTP_DPC_3615_D2V2_4	0x01	RW	Bit[7]: Manual size enable Bit[6]: Disable mirror and flip Range is [0:1] Bit[5]: Disable binning Range is [0:1] Bit[4]: Detection enable Range is [0:1] Bit[3]: Auto mode using exposure enable Range is [0:1] Bit[2]: Auto mode using gain enable Range is [0:1] Bit[1]: Flip option Range is [0:1] Bit[0]: Mirror option Range is [0:1]
0x5415	OTP_DPC_3615_D2V2_5	0x0B	RW	Bit[7]: OTP eFUSE debug mode enable Read out data of debug address in eFUSE Range is [0:1] Bit[6]: Cluster data bypass enable Range is [0:1] Bit[5]: Manual increase step enable Range is [0:1] Bit[4]: Fixed pattern enable Range is [0:1] Bit[3]: Fixed pattern selection Range is [0:1] Bit[2:0]: Recovery method selection Range is [0:4]

table 6-45 OTP_M registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x5416	OTP_DPC_3615_D2V2_6	0x80	RW	Bit[7]: Gain-dependent OTP_DPC cluster enable Bit[6]: Disable detect and remove blocks' clock gating option Bit[5]: Disable get_cluster block's clock gating option Bit[4]: Disable start frame process logic clock gating option Bit[3]: Disable cluster_buf 1 of short exposure block's clock gating option Bit[2]: Disable cluster_buf 0 of short exposure block's clock gating option Bit[1]: Disable cluster_buf 1 of long exposure block's clock gating option Bit[0]: Disable cluster_buf 0 of long exposure block's clock gating option
0x5417	OTP_DPC_3615_D2V2_7	0x00	RW	Bit[7]: Manual Y direction binning enable Bit[6]: Manual Y direction bin4 enable Bit[5]: Manual Y direction bin3 enable Bit[4]: Manual Y direction bin2 enable Bit[3]: Manual X direction binning enable Bit[2]: Manual X direction bin4 enable Bit[1]: Manual X direction bin3 enable Bit[0]: Manual X direction bin2 enable
0x5418	OTP_DPC_3615_D2V2_8	0x08	RW	Bit[7]: Manual offset enable Range is [0:1] Bit[6]: Manual offset enable Range is [0:1] Bit[5]: Manual Y direction BW binning enable Bit[4]: Manual X direction BW binning enable Bit[3:0]: Detection threshold for exposure 0 channel Range is [0:15]
0x5419	OTP_DPC_3615_D2V2_9	0x07	RW	Bit[7:0]: Gain threshold for exposure 0 channel Range is [0:255]
0x541A	OTP_DPC_3615_D2V2_A	0x00	RW	Bit[7]: Not used Bit[6:0]: Exposure threshold for exposure 0 channel[14:8] Range is [0:32767]
0x541B	OTP_DPC_3615_D2V2_B	0x00	RW	Bit[7:0]: Exposure threshold for exposure 0 channel[7:0] Range is [0:32767]

table 6-45 OTP_M registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x541C	OTP_DPC_3615_D2V2_C	0x01	RW	Bit[7]: Not used Bit[6]: y_bin26_man Bit[5]: x_bin26_man Bit[4:0]: Manual X direction increase step of even points Range is [0:31]
0x541D	OTP_DPC_3615_D2V2_D	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual X direction increase step of odd points Range is [0:31]
0x541E	OTP_DPC_3615_D2V2_E	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y direction increase step of even points Range is [0:31]
0x541F	OTP_DPC_3615_D2V2_F	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y direction increase step of odd points Range is [0:31]
0x5420	OTP_DPC_3615_D2V2_10	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[15:8] Range is [0:65535]
0x5421	OTP_DPC_3615_D2V2_11	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[7:0] Range is [0:65535]
0x5422	OTP_DPC_3615_D2V2_12	0x16	RW	Bit[7:0]: Manual X direction end in sensor array[15:8]
0x5423	OTP_DPC_3615_D2V2_13	0x3F	RW	Bit[7:0]: Manual X direction end in sensor array[7:0]
0x5424	OTP_DPC_3615_D2V2_14	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array[15:8] Range is [0:65535]
0x5425	OTP_DPC_3615_D2V2_15	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array[7:0] Range is [0:65535]
0x5426	OTP_DPC_3615_D2V2_16	0x00	RW	Bit[7:0]: OTP eFUSE debug address[15:8]
0x5427	OTP_DPC_3615_D2V2_17	0x00	RW	Bit[7:0]: OTP eFUSE debug address[7:0]
0x5428	NOT USED	–	–	Not Used

table 6-45 OTP_M registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x5429	OTP_DPC_3615_D2V2_19	0x01	RW	Bit[7:6]: Not used Bit[5]: Replace detected defect pixel with its position in sensor array Bit[4]: Position counter select 0: V counter 1: H counter Bit[3:0]: Gain-dependent threshold for exposure 0 channel Range is [0:15]
0x542A	OTP_DPC_3615_D2V2_1A	0x00	RW	Bit[7:0]: Manual hsize[15:8] Range is [0:65535]
0x542B	OTP_DPC_3615_D2V2_1B	0x00	RW	Bit[7:0]: Manual hsize[7:0] Range is [0:65535]
0x542C	OTP_DPC_3615_D2V2_1C	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[15:8] Range is [0:65535]
0x542D	OTP_DPC_3615_D2V2_1D	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[7:0] Range is [0:65535]
0x542E	OTP_DPC_3615_D2V2_1E	0x16	RW	Bit[7:0]: Manual X direction end in sensor array[15:8]
0x542F	OTP_DPC_3615_D2V2_1F	0x3F	RW	Bit[7:0]: Manual X direction end in sensor array[7:0]
0x5430	OTP_DPC_3615_D2V2_20	–	R	Bit[7:0]: X direction offset in sensor array[15:8]
0x5431	OTP_DPC_3615_D2V2_21	–	R	Bit[7:0]: X direction offset in sensor array[7:0]
0x5432	OTP_DPC_3615_D2V2_22	–	R	Bit[7:0]: Y direction offset in sensor array[15:8]
0x5433	OTP_DPC_3615_D2V2_23	–	R	Bit[7:0]: Y direction offset in sensor array[7:0]
0x5434	OTP_DPC_3615_D2V2_24	–	R	Bit[7:0]: X direction end position in sensor array[15:8]
0x5435	OTP_DPC_3615_D2V2_25	–	R	Bit[7:0]: X direction end position in sensor array[7:0]
0x5436	OTP_DPC_3615_D2V2_26	–	R	Bit[7:5]: Reserved Bit[4:0]: X direction increase step of even points
0x5437	OTP_DPC_3615_D2V2_27	–	R	Bit[7:5]: Reserved Bit[4:0]: X direction increase step of odd points

table 6-45 OTP_M registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x5438	OTP_DPC_3615_D2V2_28	–	R	Bit[7:5]: Reserved Bit[4:0]: Y direction increase step of even points
0x5439	OTP_DPC_3615_D2V2_29	–	R	Bit[7:5]: Reserved Bit[4:0]: Y direction increase step of odd points
0x543A	OTP_DPC_3615_D2V2_2A	–	R	Bit[7]: Y direction BW binning Bit[6]: Y direction bin4 Bit[5]: Y direction bin3 Bit[4]: Y direction bin2 Bit[3]: X direction BW binning Bit[2]: X direction bin4 Bit[1]: X direction bin3 Bit[0]: X direction bin2
0x543B	OTP_DPC_3615_D2V2_2B	–	R	Bit[7:0]: Data of debug address in OTP eFUSE
0x543C	OTP_DPC_3615_D2V2_2C	–	R	Bit[7:0]: X direction offset in sensor array[15:8]
0x543D	OTP_DPC_3615_D2V2_2D	–	R	Bit[7:0]: X direction offset in sensor array[7:0]
0x543E	OTP_DPC_3615_D2V2_2E	–	R	Bit[7:0]: X direction end position in sensor array[15:8]
0x543F	OTP_DPC_3615_D2V2_2F	–	R	Bit[7:0]: X direction end position in sensor array[7:0]
0x5440	OTP_DPC_3615_D2V2_30	–	R	Bit[7:0]: Software version
0x5441	OTP_DPC_3615_D2V2_31	–	R	Bit[7:0]: Hardware version

6.46 DPC_M [0x5450 - 0x5477]

table 6-46 DPC_M registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5450~ 0x5451	NOT USED	–	–	Not Used
0x5452	DPC_1715_D2V2_2	0x03	RW	Bit[7:4]: Not used Bit[3]: Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x5453	DPC_1715_D2V2_3	0x0C	RW	Bit[7]: Not used Bit[6]: Line data select 0: Use dummy line data 1: Last two lines re-use bound data Bit[5]: HDR/SBS select 0: HDR 1: SBS Bit[4]: algorithm_opt Bit[3:2]: Edge filling option Bit[1:0]: RGB/G/BR select 00: RGB 01: G 10: Not used 11: BR
0x5454	DPC_1715_D2V2_4	0x04	RW	Bit[7:0]: White pixel threshold list[0]
0x5455	DPC_1715_D2V2_5	0x04	RW	Bit[7:0]: White pixel threshold list[1]
0x5456	DPC_1715_D2V2_6	0x04	RW	Bit[7:0]: White pixel threshold list[2]
0x5457	DPC_1715_D2V2_7	0x04	RW	Bit[7:0]: White pixel threshold list[3]
0x5458	DPC_1715_D2V2_8	0x04	RW	Bit[7:0]: Black pixel threshold list[0]
0x5459	DPC_1715_D2V2_9	0x04	RW	Bit[7:0]: Black pixel threshold list[1]
0x545A	DPC_1715_D2V2_A	0x04	RW	Bit[7:0]: Black pixel threshold list[2]
0x545B	DPC_1715_D2V2_B	0x04	RW	Bit[7:0]: Black pixel threshold list[3]
0x545C	NOT USED	–	–	Not Used
0x545D	DPC_1715_D2V2_D	0x03	RW	Bit[7:0]: Gain control point[0]
0x545E	DPC_1715_D2V2_E	0x08	RW	Bit[7:0]: Gain control point[1]
0x545F	DPC_1715_D2V2_F	0x0C	RW	Bit[7:0]: Gain control point[2]
0x5460	DPC_1715_D2V2_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[0]

table 6-46 DPC_M registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5461	DPC_1715_D2V2_11	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[1]
0x5462	DPC_1715_D2V2_12	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[2]
0x5463	DPC_1715_D2V2_13	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[3]
0x5464	DPC_1715_D2V2_14	0x08	RW	Bit[7:0]: White couplet defect pixel correction gain threshold
0x5465	DPC_1715_D2V2_15	0x08	RW	Bit[7:4]: Not used Bit[3:0]: White couplet defect pixel correction gain threshold
0x5466	DPC_1715_D2V2_16	0x08	RW	Bit[7:0]: Black couplet defect pixel correction gain threshold
0x5467	DPC_1715_D2V2_17	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Black couplet defect pixel correction gain threshold
0x5468	NOT USED	–	–	Not Used
0x5469	DPC_1715_D2V2_19	0x08	RW	Bit[7:4]: Not used Bit[3:0]: White couplet threshold ratio
0x546A	DPC_1715_D2V2_1A	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Black couplet threshold ratio
0x546B	DPC_1715_D2V2_1B	0xFF	RW	Bit[7:0]: Saturation threshold
0x546C	DPC_1715_D2V2_1C	0x01	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[0]
0x546D	DPC_1715_D2V2_1D	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[1]
0x546E	DPC_1715_D2V2_1E	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[2]
0x546F	DPC_1715_D2V2_1F	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[3]
0x5470	DPC_1715_D2V2_20	0x01	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[0]
0x5471	DPC_1715_D2V2_21	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[1]
0x5472	DPC_1715_D2V2_22	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[2]
0x5473	DPC_1715_D2V2_23	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[3]

table 6-46 DPC_M registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5474~ 0x5475	NOT USED	–	–	Not Used
0x5476	DPC_1715_D2V2_26	–	R	Bit[7:0]: dpc_ver[15:8]
0x5477	DPC_1715_D2V2_27	–	R	Bit[7:0]: dpc_ver[7:0]

6.47 RAW_BIN_M [0x5480 - 0x548D]

table 6-47 RAW_BIN_M registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5480	RAW_BIN_1315_D2V2_TOP_0	0xC5	RW	Bit[7:3]: m_nVFilter[0] Vertical filter coefficients Bit[2]: m_bPDCheck_enable Enable PD check Bit[1]: m_bVBinningEnable Enable vertical binning Bit[0]: m_bHBinningEnable Enable horizontal binning
0x5481	RAW_BIN_1315_D2V2_TOP_1	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilter[1] Vertical filter coefficients
0x5482	RAW_BIN_1315_D2V2_TOP_2	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilter[2] Vertical filter coefficients
0x5483	RAW_BIN_1315_D2V2_TOP_3	0x18	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilter[3] Vertical filter coefficients
0x5484	RAW_BIN_1315_D2V2_TOP_4	0x18	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[0] Horizontal filter coefficients
0x5485	RAW_BIN_1315_D2V2_TOP_5	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[1] Horizontal filter coefficients
0x5486	RAW_BIN_1315_D2V2_TOP_6	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[2] Horizontal filter coefficients

table 6-47 RAW_BIN_M registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5487	RAW_BIN_1315_D2V2_TOP_7	0x18	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[3] Horizontal filter coefficients
0x5488	RAW_BIN_1315_D2V2_TOP_8	0x05	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilterShift Vertical filter shift
0x5489	RAW_BIN_1315_D2V2_TOP_9	0x05	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilterShift Horizontal filter shift
0x548A	RAW_BIN_1315_D2V2_TOP_A	0x00	RW	Bit[7:3]: Not used Bit[2]: m_bKeepBLC Keep BLC same for BWBinSum Bit[1]: BWBinSumEn BWBin sum enable option Bit[0]: m_bBWBin BW bin enable
0x548B	NOT USED	–	–	Not Used
0x548C	RAW_BIN_1315_D2V2_TOP_C	–	R	Bit[7:0]: RAW BIN version[15:8]
0x548D	RAW_BIN_1315_D2V2_TOP_D	–	R	Bit[7:0]: RAW BIN version[7:0]

6.48 BINC_M [0x54B0 - 0x54C7]

table 6-48 BINC_M registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x54B0	BINC_1215_D2V2_0	0x10	RW	Bit[7:6]: Not used Bit[5]: m_bEnableHCorrection Range is [0:1] Bit[4]: m_bEnableVCorrection Range is [0:1] Bit[3]: m_bHDRBin_RGBIr Range is [0:1] Bit[2]: m_bIndex_manual Range is [0:1] Bit[1]: m_nFlip_manual Range is [0:1] Bit[0]: m_nMirror_manual Range is [0:1]

table 6-48 BINC_M registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x54B1	BINC_1215_D2V2_1	0x0E	RW	Bit[7:6]: Not used Bit[5:4]: m_nVIndex[1:0] Bit[3:0]: m_nHIndex[3:0]
0x54B2	BINC_1215_D2V2_2	0x0E	RW	Bit[7:4]: m_nVIndex_manual[3:0] Bit[3:0]: m_nHIndex_manual[3:0]
0x54B3	BINC_1215_D2V2_3	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_pFilterV[0][4:0] Range is [0:31]
0x54B4	NOT USED	–	–	Not Used
0x54B5	BINC_1215_D2V2_5	0x02	RW	Bit[7:5]: Not used Bit[4:0]: m_pFilterV[1][4:0] Range is [0:31]
0x54B6	BINC_1215_D2V2_6	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[0][8] Range is [-256:255]
0x54B7	BINC_1215_D2V2_7	0x00	RW	Bit[7:0]: m_pFilterH[0][7:0] Range is [-256:255]
0x54B8	BINC_1215_D2V2_8	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[1][8] Range is [-256:255]
0x54B9	BINC_1215_D2V2_9	0x70	RW	Bit[7:0]: m_pFilterH[1][7:0] Range is [-256:255]
0x54BA	BINC_1215_D2V2_A	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[2][8] Range is [-256:255]
0x54BB	BINC_1215_D2V2_B	0x10	RW	Bit[7:0]: m_pFilterH[2][7:0] Range is [-256:255]
0x54BC	BINC_1215_D2V2_C	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[3][8] Range is [-256:255]
0x54BD	BINC_1215_D2V2_D	0x00	RW	Bit[7:0]: m_pFilterH[3][7:0] Range is [-256:255]
0x54BE~ 0x54C6	RSVD	–	–	Reserved

table 6-48 BINC_M registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x54C7	BINC_1215_D2V2_17	0x10	RW	Bit[7:5]: Reserved Bit[4]: snr_flip_sel Bit[3]: Reserved Bit[2]: clk_gate_disable_man for buffer Bit[1]: Reserved Bit[0]: clk_gate_disable_man for process[3:0]

6.49 PDF_M [0x54D0 - 0x551B]

table 6-49 PDF_M registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x54D0	PDF_3245_D2V2_TOP_0	0xC2	RW	Bit[7]: Use chromatic information enable Bit[6]: Enable PD correction or not Range is [0:1] Bit[5]: Enable single defect pixel removal Range is [0:1] Bit[4]: Rb adaptive correction enable Range is [0:1] Bit[3]: G adaptive correction enable Range is [0:1] Bit[2]: Use corner information enable Range is [0:1] Bit[1]: Use chromatic information enable Range is [0:1] Bit[0]: Is ML 2x2 pattern or not Range is [0:1]
0x54D1	PDF_3245_D2V2_TOP_1	0x08	RW	Bit[7]: Not used Bit[6]: Skip PD on B Bit[5]: Skip PD on G Bit[4:0]: Weight C Range is [0:16]

table 6-49 PDF_M registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x54D2	PDF_3245_D2V2_TOP_2	0x84	RW	Bit[7]: Control every PD and shadow Range is [0:1] Bit[6]: Control every PD and shadow Range is [0:1] Bit[5]: Control every PD and shadow Range is [0:1] Bit[4]: Control every PD and shadow Range is [0:1] Bit[3]: Control every PD and shadow Range is [0:1] Bit[2]: Control every PD and shadow Range is [0:1] Bit[1]: Control every PD and shadow Range is [0:1] Bit[0]: Control every PD and shadow Range is [0:1]
0x54D3	PDF_3245_D2V2_TOP_3	0x04	RW	Bit[7:5]: Not used Bit[4]: Control every PD and shadow Range is [0:1] Bit[3]: Control every PD and shadow Range is [0:1] Bit[2:1]: Direction based method PD correction method enable Range is [0:2] Bit[0]: m_bPDDebugMode_ Range is [0:1]
0x54D4	PDF_3245_D2V2_TOP_4	0x00	RW	Bit[7]: Enable PD/shadow ext or not Range is [0:1] Bit[6]: Enable PD/shadow ext or not Range is [0:1] Bit[5]: Enable PD/shadow ext or not Range is [0:1] Bit[4]: Enable PD/shadow ext or not Range is [0:1] Bit[3]: Enable PD/shadow ext or not Range is [0:1] Bit[2]: Enable PD/shadow ext or not Range is [0:1] Bit[1]: Enable PD/shadow ext or not Range is [0:1] Bit[0]: Enable PD/shadow ext or not Range is [0:1]

table 6-49 PDF_M registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x54D5	PDF_3245_D2V2_TOP_5	0x02	RW	Bit[7]: Enable PD/shadow ext or not Range is [0:1] Bit[6]: Enable PD/shadow ext or not Range is [0:1] Bit[5:4]: G diag option Range is [0:3] Bit[3]: Single defect pixel removal option Range is [0:1] Bit[2:0]: Single defect pixel removal shift bit Range is [0:7]
0x54D6	PDF_3245_D2V2_TOP_6	0x04	RW	Bit[7:0]: Single defect pixel threshold Range is [0:255]
0x54D7	PDF_3245_D2V2_TOP_7	0x11	RW	Bit[7:6]: m_ nDirWeightScaleBit Range is [0:3] Bit[5:4]: m_nDirWeightCurveNum Range is [0:3] Bit[3:2]: m_nBilWeightScaleBit Range is [0:3] Bit[1:0]: m_nBilWeightCurveNum Range is [0:3]
0x54D8	PDF_3245_D2V2_TOP_8	0x08	RW	Bit[7:6]: Not used Bit[5:0]: PD X cycle Range is [1:64]
0x54D9	PDF_3245_D2V2_TOP_9	0x10	RW	Bit[7:6]: Not used Bit[5:0]: PD Y cycle Range is [1:64]
0x54DA	PDF_3245_D2V2_TOP_A	0x02	RW	Bit[7:5]: Not used Bit[4:0]: PD X1 start Range is [0:31]
0x54DB	PDF_3245_D2V2_TOP_B	0x02	RW	Bit[7:5]: Not used Bit[4:0]: PD X2 start Range is [0:31]
0x54DC	PDF_3245_D2V2_TOP_C	0x06	RW	Bit[7:5]: Not used Bit[4:0]: PD X3 start Range is [0:31]
0x54DD	PDF_3245_D2V2_TOP_D	0x06	RW	Bit[7:5]: Not used Bit[4:0]: PD X4 start Range is [0:31]
0x54DE	PDF_3245_D2V2_TOP_E	0x02	RW	Bit[7:5]: Not used Bit[4:0]: PD Y1 start Range is [0:31]

table 6-49 PDF_M registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x54DF	PDF_3245_D2V2_TOP_F	0x06	RW	Bit[7:5]: Not used Bit[4:0]: PD Y2 start Range is [0:31]
0x54E0	PDF_3245_D2V2_TOP_10	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: PD Y3 start Range is [0:31]
0x54E1	PDF_3245_D2V2_TOP_11	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: PD Y4 start Range is [0:31]
0x54E2	PDF_3245_D2V2_TOP_12	0x00	RW	Bit[7:5]: Not used Bit[4:0]: PD X skip Range is [0:31]
0x54E3	PDF_3245_D2V2_TOP_13	0x00	RW	Bit[7:5]: Not used Bit[4:0]: PD Y skip Range is [0:31]
0x54E4	PDF_3245_D2V2_TOP_14	0xFF	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54E5	PDF_3245_D2V2_TOP_15	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54E6	PDF_3245_D2V2_TOP_16	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54E7	PDF_3245_D2V2_TOP_17	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54E8	PDF_3245_D2V2_TOP_18	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54E9	PDF_3245_D2V2_TOP_19	0xFF	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54EA	PDF_3245_D2V2_TOP_1A	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54EB	PDF_3245_D2V2_TOP_1B	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54EC	PDF_3245_D2V2_TOP_1C	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54ED	PDF_3245_D2V2_TOP_1D	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x54EE	PDF_3245_D2V2_TOP_1E	0x00	RW	Bit[7:0]: 1x noise level for PD correction Range is [0:255]
0x54EF	PDF_3245_D2V2_TOP_1F	0x00	RW	Bit[7:0]: 4x noise level for PD correction Range is [0:255]

table 6-49 PDF_M registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x54F0	PDF_3245_D2V2_TOP_20	0x00	RW	Bit[7:0]: 8x noise level for PD correction Range is [0:255]
0x54F1	PDF_3245_D2V2_TOP_21	0xAA	RW	Bit[7:6]: PD ch 1 Range is [0:3] Bit[5:4]: PD ch 2 Range is [0:3] Bit[3:2]: PD ch 3 Range is [0:3] Bit[1:0]: PD ch 4 Range is [0:3]
0x54F2	PDF_3245_D2V2_TOP_22	0x80	RW	Bit[7:0]: PD adaptive strength low threshold 1x Range is [0:255]
0x54F3	PDF_3245_D2V2_TOP_23	0x80	RW	Bit[7:0]: PD adaptive strength low threshold 4x Range is [0:255]
0x54F4	PDF_3245_D2V2_TOP_24	0x80	RW	Bit[7:0]: PD adaptive strength low threshold 8x Range is [0:255]
0x54F5	PDF_3245_D2V2_TOP_25	0xFF	RW	Bit[7:0]: PD adaptive strength high threshold 1x Range is [0:255]
0x54F6	PDF_3245_D2V2_TOP_26	0xFF	RW	Bit[7:0]: PD adaptive strength high threshold 8x Range is [0:255]
0x54F7	PDF_3245_D2V2_TOP_27	0xFF	RW	Bit[7:0]: PD adaptive strength high threshold 8x Range is [0:255]
0x54F8	PDF_3245_D2V2_TOP_28	0x0A	RW	Bit[7:0]: Shadow edge threshold low 1x Range is [0:255]
0x54F9	PDF_3245_D2V2_TOP_29	0x0A	RW	Bit[7:0]: Shadow edge threshold low 4x Range is [0:255]
0x54FA	PDF_3245_D2V2_TOP_2A	0x0A	RW	Bit[7:0]: Shadow edge threshold low 8x Range is [0:255]
0x54FB	PDF_3245_D2V2_TOP_2B	0x14	RW	Bit[7:0]: Shadow edge threshold high 1x Range is [0:255]
0x54FC	PDF_3245_D2V2_TOP_2C	0x14	RW	Bit[7:0]: Shadow edge threshold high 4x Range is [0:255]
0x54FD	PDF_3245_D2V2_TOP_2D	0x14	RW	Bit[7:0]: Shadow edge threshold high 8x Range is [0:255]
0x54FE	PDF_3245_D2V2_TOP_2E	0x00	RW	Bit[7:0]: Flat threshold Range is [0:255]
0x54FF	PDF_3245_D2V2_TOP_2F	0x00	RW	Bit[7:0]: Inte threshold Range is [0:255]

table 6-49 PDF_M registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x5500	PDF_3245_D2V2_TOP_30	0x12	RW	Bit[7:6]: Not used Bit[5:0]: Image width[13:8] Range is [0:16383]
0x5501	PDF_3245_D2V2_TOP_31	0x20	RW	Bit[7:0]: Image width[7:0] Range is [0:16383]
0x5502	PDF_3245_D2V2_TOP_32	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: Image height[12:8] Range is [0:8191]
0x5503	PDF_3245_D2V2_TOP_33	0xA0	RW	Bit[7:0]: Image height[7:0] Range is [0:8191]
0x5504	PDF_3245_D2V2_TOP_34	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Window start X[13:8] Range is [0:16383]
0x5505	PDF_3245_D2V2_TOP_35	0x10	RW	Bit[7:0]: Window start X[7:0] Range is [0:16383]
0x5506	PDF_3245_D2V2_TOP_36	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Window start Y[12:8] Range is [0:8191]
0x5507	PDF_3245_D2V2_TOP_37	0x10	RW	Bit[7:0]: Window start Y[7:0] Range is [0:8191]
0x5508	PDF_3245_D2V2_TOP_38	0x12	RW	Bit[7:6]: Not used Bit[5:0]: Window width[13:8] Range is [0:16383]
0x5509	PDF_3245_D2V2_TOP_39	0x00	RW	Bit[7:0]: Window width[7:0] Range is [0:16383]
0x550A	PDF_3245_D2V2_TOP_3A	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: Window height[12:8] Range is [0:8191]
0x550B	PDF_3245_D2V2_TOP_3B	0x80	RW	Bit[7:0]: Window height[7:0] Range is [0:8191]
0x550C	PDF_3245_D2V2_TOP_3C	0x00	RW	Bit[7:6]: Not used Bit[5]: vcnt_out_en Bit[4]: hcnt_out_en Bit[3]: cnt_output_en Bit[2]: engine2_off_en Bit[1]: fix_ptn_mode Bit[0]: fix_ptn_en

table 6-49 PDF_M registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x550D	PDF_3245_D2V2_TOP_3D	0x08	RW	Bit[7:4]: Not used Bit[3]: pd_cnt_clr_man_en Bit[2]: pd_win_man_en Bit[1]: xoffset_man_en Bit[0]: yoffset_man_en
0x550E	PDF_3245_D2V2_TOP_3E	0x00	RW	Bit[7:0]: r_gate_dis[7:0]
0x550F	PDF_3245_D2V2_TOP_3F	0x00	RW	Bit[7:0]: r_gate_dis[15:8]
0x5510	PDF_3245_D2V2_TOP_40	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Xoffset[13:8] Range is [0:16383]
0x5511	PDF_3245_D2V2_TOP_41	0x00	RW	Bit[7:0]: Xoffset[7:0] Range is [0:16383]
0x5512	PDF_3245_D2V2_TOP_42	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Yoffset[12:8] Range is [0:8191]
0x5513	PDF_3245_D2V2_TOP_43	0x00	RW	Bit[7:0]: Yoffset[7:0] Range is [0:8191]
0x5514	PDF_3245_D2V2_TOP_44	0x00	RW	Bit[7:4]: Not used Bit[3:0]: offset_c Range is [0:15]
0x5515	PDF_3245_D2V2_TOP_45	0x05	RW	Bit[7:5]: Not used Bit[4]: PDswitch Range is [0:1] Bit[3]: median_option Range is [0:1] Bit[2:0]: DirWeightCurveNumSquare Range is [0:3]
0x5516	PDF_3245_D2V2_TOP_46	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Xoffset1[13:8] Range is [0:16383]
0x5517	PDF_3245_D2V2_TOP_47	0x00	RW	Bit[7:0]: Xoffset1[7:0] Range is [0:16383]
0x5518~ 0x5519	NOT USED	–	–	Not Used
0x551A	PDF_3245_D2V2_TOP_4A	–	R	Bit[7:0]: Version[15:8]
0x551B	PDF_3245_D2V2_TOP_4B	–	R	Bit[7:0]: Version[7:0]

6.50 PDC_M [0x5550 - 0x564C]

table 6-50 PDC_M registers (sheet 1 of 11)

address	register name	default value	R/W	description
0x5550	PDC_3245_D2V2_TOP_0	0x6C	RW	Bit[7:6]: Not used Bit[5]: m_bML2x2HS Bit[4]: m_bByPassHighComp Bit[3]: m_nPDDOption Bit[2]: m_nEnablePreCompensate Bit[1]: m_nBypassPDCompensation Bit[0]: pdc_map_en
0x5551	PDC_3245_D2V2_TOP_1	0x00	RW	Bit[7:3]: Not used Bit[2]: m_bCurveFlip Bit[1]: m_bCurveMirror Bit[0]: m_nBinCurveEnable
0x5552	PDC_3245_D2V2_TOP_2	0x00	RW	Bit[7]: man_focuswin_en Bit[6]: win_man_en Bit[5]: yoffset_man_en Bit[4]: xoffset_man_en Bit[3]: man_ml2x2ptn_en Bit[2]: man_flip_en Bit[1]: man_mirror_en Bit[0]: man_bin_en
0x5553	PDC_3245_D2V2_TOP_3	0x00	RW	Bit[7:2]: Not used Bit[1]: man_scaler_en Bit[0]: man_pd_en
0x5554	PDC_3245_D2V2_TOP_4	0x00	RW	Bit[7]: Not used Bit[6]: man_ml2x2pattern Bit[5]: man_flip Bit[4]: man_mirror Bit[3:2]: Not used Bit[1]: man_vbin Bit[0]: man_hbin
0x5555	NOT USED	–	–	Not Used
0x5556	PDC_3245_D2V2_TOP_6	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nOffsetX>>8[13:8]
0x5557	PDC_3245_D2V2_TOP_7	0x10	RW	Bit[7:0]: m_nOffsetX[7:0]
0x5558	PDC_3245_D2V2_TOP_8	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nOffsetY>>8[13:8]
0x5559	PDC_3245_D2V2_TOP_9	0x00	RW	Bit[7:0]: m_nOffsetY[7:0]
0x555A	PDC_3245_D2V2_TOP_A	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinXStart>>8[13:8]

table 6-50 PDC_M registers (sheet 2 of 11)

address	register name	default value	R/W	description
0x555B	PDC_3245_D2V2_TOP_B	0x00	RW	Bit[7:0]: m_nWinXStart[7:0]
0x555C	PDC_3245_D2V2_TOP_C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinYStart>>8[13:8]
0x555D	PDC_3245_D2V2_TOP_D	0x00	RW	Bit[7:0]: m_nWinYStart[7:0]
0x555E	PDC_3245_D2V2_TOP_E	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinWidth>>8[13:8]
0x555F	PDC_3245_D2V2_TOP_F	0x80	RW	Bit[7:0]: m_nWinWidth[7:0]
0x5560	PDC_3245_D2V2_TOP_10	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinHeight>>8[13:8]
0x5561	PDC_3245_D2V2_TOP_11	0xA0	RW	Bit[7:0]: m_nWinHeight[7:0]
0x5562	PDC_3245_D2V2_TOP_12	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinLeft>>8[13:8]
0x5563	PDC_3245_D2V2_TOP_13	0x00	RW	Bit[7:0]: m_nFocusWinLeft[7:0]
0x5564	PDC_3245_D2V2_TOP_14	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinTop>>8[13:8]
0x5565	PDC_3245_D2V2_TOP_15	0x00	RW	Bit[7:0]: m_nFocusWinTop[7:0]
0x5566	PDC_3245_D2V2_TOP_16	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinWidth>>8[13:8]
0x5567	PDC_3245_D2V2_TOP_17	0x80	RW	Bit[7:0]: m_nFocusWinWidth[7:0]
0x5568	PDC_3245_D2V2_TOP_18	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinHeight>>8[13:8]
0x5569	PDC_3245_D2V2_TOP_19	0xA0	RW	Bit[7:0]: m_nFocusWinHeight[7:0]
0x556A	PDC_3245_D2V2_TOP_1A	0x10	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDCycleX[5:0]
0x556B	PDC_3245_D2V2_TOP_1B	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDCycleY[5:0]
0x556C	PDC_3245_D2V2_TOP_1C	0x01	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDSkipX[4:0]
0x556D	PDC_3245_D2V2_TOP_1D	0x01	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDSkipY[4:0]
0x556E	PDC_3245_D2V2_TOP_1E	0x04	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX1[4:0]
0x556F	PDC_3245_D2V2_TOP_1F	0x04	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX2[4:0]

table 6-50 PDC_M registers (sheet 3 of 11)

address	register name	default value	R/W	description
0x5570	PDC_3245_D2V2_TOP_20	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX3[4:0]
0x5571	PDC_3245_D2V2_TOP_21	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX4[4:0]
0x5572	PDC_3245_D2V2_TOP_22	0x04	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY1[4:0]
0x5573	PDC_3245_D2V2_TOP_23	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY2[4:0]
0x5574	PDC_3245_D2V2_TOP_24	0x14	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY3[4:0]
0x5575	PDC_3245_D2V2_TOP_25	0x1C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY4[4:0]
0x5576	PDC_3245_D2V2_TOP_26	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh1
0x5577	PDC_3245_D2V2_TOP_27	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh2
0x5578	PDC_3245_D2V2_TOP_28	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh3
0x5579	PDC_3245_D2V2_TOP_29	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh4
0x557A	PDC_3245_D2V2_TOP_2A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDFadingScalerH>>8[9:8]
0x557B	PDC_3245_D2V2_TOP_2B	0x40	RW	Bit[7:0]: m_nPDFadingScalerH[7:0]
0x557C	PDC_3245_D2V2_TOP_2C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDFadingScalerV>>8[9:8]
0x557D	PDC_3245_D2V2_TOP_2D	0x56	RW	Bit[7:0]: m_nPDFadingScalerV[7:0]
0x557E	PDC_3245_D2V2_TOP_2E	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nBinNumA[3:0]
0x557F	PDC_3245_D2V2_TOP_2F	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nBinNumB[3:0]
0x5580	PDC_3245_D2V2_TOP_30	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDWidth_ori>>8[13:8]
0x5581	PDC_3245_D2V2_TOP_31	0x80	RW	Bit[7:0]: m_nPDWidth_ori[7:0]
0x5582	PDC_3245_D2V2_TOP_32	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDHeight_ori>>8[13:8]
0x5583	PDC_3245_D2V2_TOP_33	0xA0	RW	Bit[7:0]: m_nPDHeight_ori[7:0]

table 6-50 PDC_M registers (sheet 4 of 11)

address	register name	default value	R/W	description
0x5584	PDC_3245_D2V2_TOP_34	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nArrayWidth>>8[13:8]
0x5585	PDC_3245_D2V2_TOP_35	0x80	RW	Bit[7:0]: m_nArrayWidth[7:0]
0x5586	PDC_3245_D2V2_TOP_36	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nArrayHeight>>8[13:8]
0x5587	PDC_3245_D2V2_TOP_37	0xA0	RW	Bit[7:0]: m_nArrayHeight[7:0]
0x5588	PDC_3245_D2V2_TOP_38	0x0F	RW	Bit[7:6]: Not used Bit[5:0]: m_nOffsetX>>8[13:8]
0x5589	PDC_3245_D2V2_TOP_39	0xB8	RW	Bit[7:0]: m_nOffsetX[7:0]
0x558A	PDC_3245_D2V2_TOP_3A	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinLeft>>8[13:8]
0x558B	PDC_3245_D2V2_TOP_3B	0x00	RW	Bit[7:0]: m_nFocusWinLeft[7:0]
0x558C	PDC_3245_D2V2_TOP_3C	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinWidth>>8[13:8]
0x558D	PDC_3245_D2V2_TOP_3D	0x80	RW	Bit[7:0]: m_nFocusWinWidth[7:0]
0x558E~ 0x558F	NOT USED	–	–	Not Used
0x5590	PDC_3245_D2V2_TOP_40	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[0]>>8[15:8]
0x5591	PDC_3245_D2V2_TOP_41	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[0][7:0]
0x5592	PDC_3245_D2V2_TOP_42	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[1]>>8[15:8]
0x5593	PDC_3245_D2V2_TOP_43	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[1][7:0]
0x5594	PDC_3245_D2V2_TOP_44	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[2]>>8[15:8]
0x5595	PDC_3245_D2V2_TOP_45	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[2][7:0]
0x5596	PDC_3245_D2V2_TOP_46	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[3]>>8[15:8]
0x5597	PDC_3245_D2V2_TOP_47	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[3][7:0]
0x5598	PDC_3245_D2V2_TOP_48	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[4]>>8[15:8]
0x5599	PDC_3245_D2V2_TOP_49	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[4][7:0]
0x559A	PDC_3245_D2V2_TOP_4A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[5]>>8[15:8]
0x559B	PDC_3245_D2V2_TOP_4B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[5][7:0]
0x559C	PDC_3245_D2V2_TOP_4C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[6]>>8[15:8]
0x559D	PDC_3245_D2V2_TOP_4D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[6][7:0]
0x559E	PDC_3245_D2V2_TOP_4E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[7]>>8[15:8]

table 6-50 PDC_M registers (sheet 5 of 11)

address	register name	default value	R/W	description
0x559F	PDC_3245_D2V2_TOP_4F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[7][7:0]
0x55A0	PDC_3245_D2V2_TOP_50	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[8]>>8[15:8]
0x55A1	PDC_3245_D2V2_TOP_51	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[8][7:0]
0x55A2	PDC_3245_D2V2_TOP_52	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[9]>>8[15:8]
0x55A3	PDC_3245_D2V2_TOP_53	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[9][7:0]
0x55A4	PDC_3245_D2V2_TOP_54	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[10]>>8[15:8]
0x55A5	PDC_3245_D2V2_TOP_55	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[10][7:0]
0x55A6	PDC_3245_D2V2_TOP_56	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[11]>>8[15:8]
0x55A7	PDC_3245_D2V2_TOP_57	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[11][7:0]
0x55A8	PDC_3245_D2V2_TOP_58	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[12]>>8[15:8]
0x55A9	PDC_3245_D2V2_TOP_59	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[12][7:0]
0x55AA	PDC_3245_D2V2_TOP_5A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[13]>>8[15:8]
0x55AB	PDC_3245_D2V2_TOP_5B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[13][7:0]
0x55AC	PDC_3245_D2V2_TOP_5C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[14]>>8[15:8]
0x55AD	PDC_3245_D2V2_TOP_5D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[14][7:0]
0x55AE	PDC_3245_D2V2_TOP_5E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[15]>>8[15:8]
0x55AF	PDC_3245_D2V2_TOP_5F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[15][7:0]
0x55B0	PDC_3245_D2V2_TOP_60	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[16]>>8[15:8]
0x55B1	PDC_3245_D2V2_TOP_61	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[16][7:0]
0x55B2	PDC_3245_D2V2_TOP_62	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[17]>>8[15:8]
0x55B3	PDC_3245_D2V2_TOP_63	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[17][7:0]
0x55B4	PDC_3245_D2V2_TOP_64	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[18]>>8[15:8]
0x55B5	PDC_3245_D2V2_TOP_65	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[18][7:0]
0x55B6	PDC_3245_D2V2_TOP_66	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[19]>>8[15:8]
0x55B7	PDC_3245_D2V2_TOP_67	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[19][7:0]
0x55B8	PDC_3245_D2V2_TOP_68	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[20]>>8[15:8]
0x55B9	PDC_3245_D2V2_TOP_69	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[20][7:0]
0x55BA	PDC_3245_D2V2_TOP_6A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[21]>>8[15:8]
0x55BB	PDC_3245_D2V2_TOP_6B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[21][7:0]
0x55BC	PDC_3245_D2V2_TOP_6C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[22]>>8[15:8]

table 6-50 PDC_M registers (sheet 6 of 11)

address	register name	default value	R/W	description
0x55BD	PDC_3245_D2V2_TOP_6D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[22][7:0]
0x55BE	PDC_3245_D2V2_TOP_6E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[23]>>8[15:8]
0x55BF	PDC_3245_D2V2_TOP_6F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[23][7:0]
0x55C0	PDC_3245_D2V2_TOP_70	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[24]>>8[15:8]
0x55C1	PDC_3245_D2V2_TOP_71	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[24][7:0]
0x55C2	PDC_3245_D2V2_TOP_72	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[25]>>8[15:8]
0x55C3	PDC_3245_D2V2_TOP_73	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[25][7:0]
0x55C4	PDC_3245_D2V2_TOP_74	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[26]>>8[15:8]
0x55C5	PDC_3245_D2V2_TOP_75	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[26][7:0]
0x55C6	PDC_3245_D2V2_TOP_76	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[27]>>8[15:8]
0x55C7	PDC_3245_D2V2_TOP_77	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[27][7:0]
0x55C8	PDC_3245_D2V2_TOP_78	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[28]>>8[15:8]
0x55C9	PDC_3245_D2V2_TOP_79	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[28][7:0]
0x55CA	PDC_3245_D2V2_TOP_7A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[29]>>8[15:8]
0x55CB	PDC_3245_D2V2_TOP_7B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[29][7:0]
0x55CC	PDC_3245_D2V2_TOP_7C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[30]>>8[15:8]
0x55CD	PDC_3245_D2V2_TOP_7D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[30][7:0]
0x55CE	PDC_3245_D2V2_TOP_7E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[31]>>8[15:8]
0x55CF	PDC_3245_D2V2_TOP_7F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[31][7:0]
0x55D0	PDC_3245_D2V2_TOP_80	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[0][5:0]
0x55D1	PDC_3245_D2V2_TOP_81	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[1][5:0]
0x55D2	PDC_3245_D2V2_TOP_82	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[2][5:0]
0x55D3	PDC_3245_D2V2_TOP_83	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[3][5:0]
0x55D4	PDC_3245_D2V2_TOP_84	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[4][5:0]
0x55D5	PDC_3245_D2V2_TOP_85	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[5][5:0]
0x55D6	PDC_3245_D2V2_TOP_86	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[6][5:0]

table 6-50 PDC_M registers (sheet 7 of 11)

address	register name	default value	R/W	description
0x55D7	PDC_3245_D2V2_TOP_87	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[7][5:0]
0x55D8	PDC_3245_D2V2_TOP_88	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[8][5:0]
0x55D9	PDC_3245_D2V2_TOP_89	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[9][5:0]
0x55DA	PDC_3245_D2V2_TOP_8A	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[10][5:0]
0x55DB	PDC_3245_D2V2_TOP_8B	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[11][5:0]
0x55DC	PDC_3245_D2V2_TOP_8C	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[12][5:0]
0x55DD	PDC_3245_D2V2_TOP_8D	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[13][5:0]
0x55DE	PDC_3245_D2V2_TOP_8E	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[14][5:0]
0x55DF	PDC_3245_D2V2_TOP_8F	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[15][5:0]
0x55E0	PDC_3245_D2V2_TOP_90	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[16][5:0]
0x55E1	PDC_3245_D2V2_TOP_91	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[17][5:0]
0x55E2	PDC_3245_D2V2_TOP_92	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[18][5:0]
0x55E3	PDC_3245_D2V2_TOP_93	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[19][5:0]
0x55E4	PDC_3245_D2V2_TOP_94	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[20][5:0]
0x55E5	PDC_3245_D2V2_TOP_95	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[21][5:0]
0x55E6	PDC_3245_D2V2_TOP_96	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[22][5:0]
0x55E7	PDC_3245_D2V2_TOP_97	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[23][5:0]
0x55E8	PDC_3245_D2V2_TOP_98	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[24][5:0]
0x55E9	PDC_3245_D2V2_TOP_99	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[25][5:0]

table 6-50 PDC_M registers (sheet 8 of 11)

address	register name	default value	R/W	description
0x55EA	PDC_3245_D2V2_TOP_9A	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[26][5:0]
0x55EB	PDC_3245_D2V2_TOP_9B	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[27][5:0]
0x55EC	PDC_3245_D2V2_TOP_9C	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[28][5:0]
0x55ED	PDC_3245_D2V2_TOP_9D	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[29][5:0]
0x55EE	PDC_3245_D2V2_TOP_9E	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[30][5:0]
0x55EF	PDC_3245_D2V2_TOP_9F	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[31][5:0]
0x55F0	PDC_3245_D2V2_TOP_A0	0x01	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[0][5:0]
0x55F1	PDC_3245_D2V2_TOP_A1	0x02	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[1][5:0]
0x55F2	PDC_3245_D2V2_TOP_A2	0x03	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[2][5:0]
0x55F3	PDC_3245_D2V2_TOP_A3	0x04	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[3][5:0]
0x55F4	PDC_3245_D2V2_TOP_A4	0x05	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[4][5:0]
0x55F5	PDC_3245_D2V2_TOP_A5	0x06	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[5][5:0]
0x55F6	PDC_3245_D2V2_TOP_A6	0x07	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[6][5:0]
0x55F7	PDC_3245_D2V2_TOP_A7	0x08	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[7][5:0]
0x55F8	PDC_3245_D2V2_TOP_A8	0x09	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[8][5:0]
0x55F9	PDC_3245_D2V2_TOP_A9	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[9][5:0]
0x55FA	PDC_3245_D2V2_TOP_AA	0x0B	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[10][5:0]
0x55FB	PDC_3245_D2V2_TOP_AB	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[11][5:0]
0x55FC	PDC_3245_D2V2_TOP_AC	0x0D	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[12][5:0]

table 6-50 PDC_M registers (sheet 9 of 11)

address	register name	default value	R/W	description
0x55FD	PDC_3245_D2V2_TOP_AD	0x0E	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[13][5:0]
0x55FE	PDC_3245_D2V2_TOP_AE	0x0F	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[14][5:0]
0x55FF	PDC_3245_D2V2_TOP_AF	0x10	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[15][5:0]
0x5600	PDC_3245_D2V2_TOP_B0	0x11	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[16][5:0]
0x5601	PDC_3245_D2V2_TOP_B1	0x12	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[17][5:0]
0x5602	PDC_3245_D2V2_TOP_B2	0x13	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[18][5:0]
0x5603	PDC_3245_D2V2_TOP_B3	0x14	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[19][5:0]
0x5604	PDC_3245_D2V2_TOP_B4	0x15	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[20][5:0]
0x5605	PDC_3245_D2V2_TOP_B5	0x16	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[21][5:0]
0x5606	PDC_3245_D2V2_TOP_B6	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[22][5:0]
0x5607	PDC_3245_D2V2_TOP_B7	0x18	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[23][5:0]
0x5608	PDC_3245_D2V2_TOP_B8	0x19	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[24][5:0]
0x5609	PDC_3245_D2V2_TOP_B9	0x1A	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[25][5:0]
0x560A	PDC_3245_D2V2_TOP_BA	0x1B	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[26][5:0]
0x560B	PDC_3245_D2V2_TOP_BB	0x1C	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[27][5:0]
0x560C	PDC_3245_D2V2_TOP_BC	0x1D	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[28][5:0]
0x560D	PDC_3245_D2V2_TOP_BD	0x1E	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[29][5:0]
0x560E	PDC_3245_D2V2_TOP_BE	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[30][5:0]
0x560F	PDC_3245_D2V2_TOP_BF	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[31][5:0]

table 6-50 PDC_M registers (sheet 10 of 11)

address	register name	default value	R/W	description
0x5610	PDC_3245_D2V2_TOP_C0	0x03	RW	Bit[7:4]: Not used Bit[3:0]: m_nOverExpoThre>>8[11:8]
0x5611	PDC_3245_D2V2_TOP_C1	0xFF	RW	Bit[7:0]: m_nOverExpoThre[7:0]
0x5612	PDC_3245_D2V2_TOP_C2	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Calculate start select Bit[3:0]: Replace PD by column/row count in debug mode
0x5613	PDC_3245_D2V2_TOP_C3	0x01	RW	Bit[7:5]: Not used Bit[4]: Firmware write SRAM enable Bit[3:2]: Not used Bit[1:0]: Firmware read SRAM select 00: None 01: L 10: M 11: S
0x5614~ 0x562F	NOT USED	–	–	Not Used
0x5630	PDC_3245_D2V2_TOP_E0	0x00	RW	Bit[7:0]: PD restore control
0x5631	PDC_3245_D2V2_TOP_E1	0x02	RW	Bit[7:4]: Not used Bit[3]: m_bFourCell2PD Bit[2]: m_nPDOption Bit[1:0]: m_bMedianFilterOption
0x5632	PDC_3245_D2V2_TOP_E2	0x42	RW	Bit[7:4]: m_nMedianFilterPixel[0][3:0] Bit[3:0]: m_nMedianFilterPixel[1][3:0]
0x5633	PDC_3245_D2V2_TOP_E3	0x24	RW	Bit[7:4]: m_nMedianFilterPixel[2][3:0] Bit[3:0]: m_nMedianFilterPixel[3][3:0]
0x5634	PDC_3245_D2V2_TOP_E4	0x00	RW	Bit[7:5]: Not used Bit[4:2]: PD restore dbg_cnt_sel Bit[1:0]: PD restore dbg_byt_sel
0x5635~ 0x563F	NOT USED	–	–	Not Used
0x5640	PDC_3245_D2V2_TOP_F0	–	R	Bit[7:0]: PDC version[15:8]
0x5641	PDC_3245_D2V2_TOP_F1	–	R	Bit[7:0]: PDC version[7:0]
0x5642~ 0x5644	NOT USED	–	–	Not Used
0x5645	PDC_3245_D2V2_TOP_F5	–	R	Bit[7:0]: PD counter[23:16]
0x5646	PDC_3245_D2V2_TOP_F6	–	R	Bit[7:0]: PD counter[15:8]
0x5647	PDC_3245_D2V2_TOP_F7	–	R	Bit[7:0]: PD counter[7:0]

table 6-50 PDC_M registers (sheet 11 of 11)

address	register name	default value	R/W	description
0x5648	NOT USED	–	–	Not Used
0x5649	PDC_3245_D2V2_TOP_F9	–	R	Bit[7:0]: PD counter[23:16]
0x564A	PDC_3245_D2V2_TOP_FA	–	R	Bit[7:0]: PD counter[15:8]
0x564B	PDC_3245_D2V2_TOP_FB	–	R	Bit[7:0]: PD counter[7:0]
0x564C	PDC_3245_D2V2_TOP_FC	–	R	Bit[7:0]: PD restore PD VC counter

6.51 RAW_DNS_M [0x5650 - 0x565F]

table 6-51 RAW_DNS_M registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5650~ 0x5652	NOT USED	–	–	Not Used
0x5653	RAW_DNS_1055_3	0x05	RW	Bit[7:5]: Reserved Bit[4]: dns_para_man_en Bit[3]: dns_mode Bit[2]: avg_dis_1 Range is [0:1] Bit[1]: avg_dis_0 Range is [0:1] Bit[0]: g_dns_en Range is [0:1]
0x5654	RAW_DNS_1055_4	0x04	RW	Bit[7:0]: dns_noise_list_0 Range is [0:7]
0x5655	RAW_DNS_1055_5	0x08	RW	Bit[7:0]: dns_noise_list_1 Range is [8:15]
0x5656	RAW_DNS_1055_6	0x10	RW	Bit[7:0]: dns_noise_list_2 Range is [16:31]
0x5657	RAW_DNS_1055_7	0x18	RW	Bit[7:0]: dns_noise_list_3 Range is [32:63]
0x5658	RAW_DNS_1055_8	0x20	RW	Bit[7:0]: dns_noise_list_4 Range is [64:95]
0x5659	RAW_DNS_1055_9	0x30	RW	Bit[7:0]: dns_noise_list_5 Range is [96:127]
0x565A	RAW_DNS_1055_A	0x40	RW	Bit[7:0]: dns_noise_list_6 Range is [128:191]

table 6-51 RAW_DNS_M registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x565B	RAW_DNS_1055_B	0x40	RW	Bit[7:0]: dns_noise_list_7 Range is [192:255]
0x565C~ 0x565E	RSVD	–	–	Reserved
0x565F	RAW_DNS_1055_F	0x08	RW	Bit[7:0]: dns_noise_man

6.52 PRE_ISP_S [0x56C0 - 0x56E7]

table 6-52 PRE_ISP_S registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x56C0	PRE_ISP_2325_D2V2_TOP_0	0x00	RW	Bit[7:5]: Not used Bit[4]: Disable clock gating Range is [0:1] Bit[3]: Reserved Bit[2]: Manual size enable Range is [0:1] Bit[1]: Manual end address enable Range is [0:1] Bit[0]: Manual offset (start address) enable Range is [0:1]
0x56C1	PRE_ISP_2325_D2V2_TOP_1	0x00	RW	Bit[7]: Flip option Range is [0:1] Bit[6]: Mirror option Range is [0:1] Bit[5:4]: Color bar option Range is [0:3] Bit[3]: Transparent mode enable Range is [0:1] Bit[2]: Rolling mode enable Range is [0:1] Bit[1]: Clear last four bits enable Range is [0:1] Bit[0]: Test pattern enable Range is [0:1]
0x56C2	PRE_ISP_2325_D2V2_TOP_2	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Test pattern mode Range is [0:7]
0x56C3	RSVD	–	–	Reserved

table 6-52 PRE_ISP_S registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x56C4	PRE_ISP_2325_D2V2_TOP_4	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Manual width[13:8] Range is [0:4704]
0x56C5	PRE_ISP_2325_D2V2_TOP_5	0x80	RW	Bit[7:0]: Manual width[7:0] Range is [0:4704]
0x56C6	PRE_ISP_2325_D2V2_TOP_6	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual height[12:8] Range is [0:3536]
0x56C7	PRE_ISP_2325_D2V2_TOP_7	0xE0	RW	Bit[7:0]: Manual height[7:0] Range is [0:3536]
0x56C8	PRE_ISP_2325_D2V2_TOP_8	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Manual X offset[13:8] Range is [0:4704]
0x56C9	PRE_ISP_2325_D2V2_TOP_9	0x00	RW	Bit[7:0]: Manual X offset[7:0] Range is [0:4704]
0x56CA	PRE_ISP_2325_D2V2_TOP_A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y offset[12:8] Range is [0:3536]
0x56CB	PRE_ISP_2325_D2V2_TOP_B	0x00	RW	Bit[7:0]: Manual Y offset[7:0] Range is [0:3536]
0x56CC	PRE_ISP_2325_D2V2_TOP_C	0x02	RW	Bit[7:6]: Not used Bit[5:0]: Manual X end[13:8] Range is [0:4704]
0x56CD	PRE_ISP_2325_D2V2_TOP_D	0x80	RW	Bit[7:0]: Manual X end[7:0] Range is [0:4704]
0x56CE	PRE_ISP_2325_D2V2_TOP_E	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y end[12:8] Range is [0:3536]
0x56CF	PRE_ISP_2325_D2V2_TOP_F	0xE0	RW	Bit[7:0]: Manual Y end[7:0] Range is [0:3536]
0x56D0~ 0x56D1	NOT USED	–	–	Not Used
0x56D2	PRE_ISP_2325_D2V2_TOP_12	0x01	RW	Bit[7:5]: Not used Bit[4:0]: In_number[12:8] Range is [0:3536]
0x56D3	PRE_ISP_2325_D2V2_TOP_13	0xE0	RW	Bit[7:0]: In_number[7:0] Range is [0:3536]
0x56D4~ 0x56D7	NOT USED	–	–	Not Used

table 6-52 PRE_ISP_S registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x56D8	PRE_ISP_2325_D2V2_TOP_18	–	R	Bit[7:6]: Reserved Bit[5:0]: Pixel count[13:8] Range is [0:3536]
0x56D9	PRE_ISP_2325_D2V2_TOP_19	–	R	Bit[7:0]: Pixel count[7:0] Range is [0:3536]
0x56DA	PRE_ISP_2325_D2V2_TOP_1A	–	R	Bit[7:5]: Reserved Bit[4:0]: Line count[12:8] Range is [0:255]
0x56DB	PRE_ISP_2325_D2V2_TOP_1B	–	R	Bit[7:0]: Line count[7:0] Range is [0:255]
0x56DC	PRE_ISP_2325_D2V2_TOP_1C	–	R	Bit[7:0]: dbg_0 Range is [0:255]
0x56DD	PRE_ISP_2325_D2V2_TOP_1D	–	R	Bit[7:0]: dbg_1 Range is [0:255]
0x56DE	PRE_ISP_2325_D2V2_TOP_1E	–	R	Bit[7:0]: dbg_2 Range is [0:1]
0x56DF	PRE_ISP_2325_D2V2_TOP_1F	–	R	Bit[7:0]: dbg_3 Range is [0:8191]
0x56E0	PRE_ISP_2325_D2V2_TOP_20	–	R	Bit[7:6]: Reserved Bit[5:0]: x_offset[13:8] Range is [0:8191]
0x56E1	PRE_ISP_2325_D2V2_TOP_21	–	R	Bit[7:0]: x_offset[7:0] Range is [0:8191]
0x56E2	PRE_ISP_2325_D2V2_TOP_22	–	R	Bit[7:5]: Reserved Bit[4:0]: y_offset[12:8] Range is [0:4095]
0x56E3	PRE_ISP_2325_D2V2_TOP_23	–	R	Bit[7:0]: y_offset[7:0] Range is [0:4095]
0x56E4~ 0x56E5	NOT USED	–	–	Not Used
0x56E6	PRE_ISP_2325_D2V2_TOP_26	–	R	Bit[7:0]: Software version[15:8] Range is [0:255]
0x56E7	PRE_ISP_2325_D2V2_TOP_27	–	R	Bit[7:0]: Hardware version[7:0] Range is [0:255]

6.53 AWBG_S [0x56F0 - 0x5707]

table 6-53 AWBG_S registers

address	register name	default value	R/W	description
0x56F0	AWBG_24_0	0xEE	RW	Bit[7:0]: CFAY[31:24]
0x56F1	AWBG_24_1	0x44	RW	Bit[7:0]: CFAY[23:16]
0x56F2	AWBG_24_2	0xEE	RW	Bit[7:0]: CFAY[15:8]
0x56F3	AWBG_24_3	0x44	RW	Bit[7:0]: CFAY[7:0]
0x56F4	AWBG_24_4	0x00	RW	Bit[7:0]: gain_lat_sel[7:0]
0x56F5	AWBG_24_5	0x02	RW	Bit[7:4]: Not used Bit[3]: cfay_man_en Bit[2]: blc_man_en Bit[1:0]: mne[9:8]
0x56F6	AWBG_24_6	0x00	RW	Bit[7:0]: MNE[7:0]
0x56F7	AWBG_24_7	0x00	RW	Bit[7:0]: BLC
0x56F8~ 0x56FF	RSVD	–	–	Reserved
0x5700	AWBG_24_8	0x04	RW	Bit[7:0]: cfa_gain0[15:8]
0x5701	AWBG_24_9	0x00	RW	Bit[7:0]: cfa_gain0[7:0]
0x5702	AWBG_24_A	0x04	RW	Bit[7:0]: cfa_gain1[15:8]
0x5703	AWBG_24_B	0x00	RW	Bit[7:0]: cfa_gain1[7:0]
0x5704	AWBG_24_C	0x04	RW	Bit[7:0]: cfa_gain2[15:8]
0x5705	AWBG_24_D	0x00	RW	Bit[7:0]: cfa_gain2[7:0]
0x5706	AWBG_24_E	0x04	RW	Bit[7:0]: cfa_gain3[15:8]
0x5707	AWBG_24_F	0x00	RW	Bit[7:0]: cfa_gain3[7:0]

6.54 OTP_S [0x5710 - 0x5741]

table 6-54 OTP_S registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x5710	OTP_DPC_3615_D2V2_0	0x00	RW	Bit[7:0]: OTP eFUSE start address[15:8]
0x5711	OTP_DPC_3615_D2V2_1	0x00	RW	Bit[7:0]: OTP eFUSE start address[7:0]
0x5712	OTP_DPC_3615_D2V2_2	0xFF	RW	Bit[7:0]: OTP eFUSE end address[15:8]
0x5713	OTP_DPC_3615_D2V2_3	0xFF	RW	Bit[7:0]: OTP eFUSE end address[7:0]
0x5714	OTP_DPC_3615_D2V2_4	0x01	RW	Bit[7]: Manual size enable Bit[6]: Disable mirror and flip Range is [0:1] Bit[5]: Disable binning Range is [0:1] Bit[4]: Detection enable Range is [0:1] Bit[3]: Auto mode using exposure enable Range is [0:1] Bit[2]: Auto mode using gain enable Range is [0:1] Bit[1]: Flip option Range is [0:1] Bit[0]: Mirror option Range is [0:1]
0x5715	OTP_DPC_3615_D2V2_5	0x0B	RW	Bit[7]: OTP eFUSE debug mode enable Read out data of debug address in eFUSE Range is [0:1] Bit[6]: Cluster data bypass enable Range is [0:1] Bit[5]: Manual increase step enable Range is [0:1] Bit[4]: Fixed pattern enable Range is [0:1] Bit[3]: Fixed pattern selection Range is [0:1] Bit[2:0]: Recovery method selection Range is [0:4]

table 6-54 OTP_S registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x5716	OTP_DPC_3615_D2V2_6	0x80	RW	Bit[7]: Gain-dependent OTP_DPC cluster enable Bit[6]: Disable detect and remove blocks' clock gating option Bit[5]: Disable get_cluster block's clock gating option Bit[4]: Disable start frame process logic clock gating option Bit[3]: Disable cluster_buf 1 of short exposure block's clock gating option Bit[2]: Disable cluster_buf 0 of short exposure block's clock gating option Bit[1]: Disable cluster_buf 1 of long exposure block's clock gating option Bit[0]: Disable cluster_buf 0 of long exposure block's clock gating option
0x5717	OTP_DPC_3615_D2V2_7	0x00	RW	Bit[7]: Manual Y direction binning enable Bit[6]: Manual Y direction bin4 enable Bit[5]: Manual Y direction bin3 enable Bit[4]: Manual Y direction bin2 enable Bit[3]: Manual X direction binning enable Bit[2]: Manual X direction bin4 enable Bit[1]: Manual X direction bin3 enable Bit[0]: Manual X direction bin2 enable
0x5718	OTP_DPC_3615_D2V2_8	0x08	RW	Bit[7]: Manual offset enable Range is [0:1] Bit[6]: Manual offset enable Range is [0:1] Bit[5]: Manual Y direction BW binning enable Bit[4]: Manual X direction BW binning enable Bit[3:0]: Detection threshold for exposure 0 channel Range is [0:15]
0x5719	OTP_DPC_3615_D2V2_9	0x07	RW	Bit[7:0]: Gain threshold for exposure 0 channel Range is [0:255]
0x571A	OTP_DPC_3615_D2V2_A	0x00	RW	Bit[7]: Not used Bit[6:0]: Exposure threshold for exposure 0 channel[14:8] Range is [0:32767]
0x571B	OTP_DPC_3615_D2V2_B	0x00	RW	Bit[7:0]: Exposure threshold for exposure 0 channel[7:0] Range is [0:32767]

table 6-54 OTP_S registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x571C	OTP_DPC_3615_D2V2_C	0x01	RW	Bit[7]: Not used Bit[6]: y_bin26_man Bit[5]: x_bin26_man Bit[4:0]: Manual X direction increase step of even points Range is [0:31]
0x571D	OTP_DPC_3615_D2V2_D	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual X direction increase step of odd points Range is [0:31]
0x571E	OTP_DPC_3615_D2V2_E	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y direction increase step of even points Range is [0:31]
0x571F	OTP_DPC_3615_D2V2_F	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Manual Y direction increase step of odd points Range is [0:31]
0x5720	OTP_DPC_3615_D2V2_10	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[15:8] Range is [0:65535]
0x5721	OTP_DPC_3615_D2V2_11	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[7:0] Range is [0:65535]
0x5722	OTP_DPC_3615_D2V2_12	0x16	RW	Bit[7:0]: Manual X direction end in sensor array[15:8]
0x5723	OTP_DPC_3615_D2V2_13	0x3F	RW	Bit[7:0]: Manual X direction end in sensor array[7:0]
0x5724	OTP_DPC_3615_D2V2_14	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array[15:8] Range is [0:65535]
0x5725	OTP_DPC_3615_D2V2_15	0x00	RW	Bit[7:0]: Manual Y direction offset in sensor array[7:0] Range is [0:65535]
0x5726	OTP_DPC_3615_D2V2_16	0x00	RW	Bit[7:0]: OTP eFUSE debug address[15:8]
0x5727	OTP_DPC_3615_D2V2_17	0x00	RW	Bit[7:0]: OTP eFUSE debug address[7:0]
0x5728	NOT USED	–	–	Not Used

table 6-54 OTP_S registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x5729	OTP_DPC_3615_D2V2_19	0x01	RW	Bit[7:6]: Not used Bit[5]: Replace detected defect pixel with its position in sensor array Bit[4]: Position counter select 0: V counter 1: H counter Bit[3:0]: Gain-dependent threshold for exposure 0 channel Range is [0:15]
0x572A	OTP_DPC_3615_D2V2_1A	0x00	RW	Bit[7:0]: Manual hsize[15:8] Range is [0:65535]
0x572B	OTP_DPC_3615_D2V2_1B	0x00	RW	Bit[7:0]: Manual hsize[7:0] Range is [0:65535]
0x572C	OTP_DPC_3615_D2V2_1C	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[15:8] Range is [0:65535]
0x572D	OTP_DPC_3615_D2V2_1D	0x00	RW	Bit[7:0]: Manual X direction offset in sensor array[7:0] Range is [0:65535]
0x572E	OTP_DPC_3615_D2V2_1E	0x16	RW	Bit[7:0]: Manual X direction end in sensor array[15:8]
0x572F	OTP_DPC_3615_D2V2_1F	0x3F	RW	Bit[7:0]: Manual X direction end in sensor array[7:0]
0x5730	OTP_DPC_3615_D2V2_20	–	R	Bit[7:0]: X direction offset in sensor array[15:8]
0x5731	OTP_DPC_3615_D2V2_21	–	R	Bit[7:0]: X direction offset in sensor array[7:0]
0x5732	OTP_DPC_3615_D2V2_22	–	R	Bit[7:0]: Y direction offset in sensor array[15:8]
0x5733	OTP_DPC_3615_D2V2_23	–	R	Bit[7:0]: Y direction offset in sensor array[7:0]
0x5734	OTP_DPC_3615_D2V2_24	–	R	Bit[7:0]: X direction end position in sensor array[15:8]
0x5735	OTP_DPC_3615_D2V2_25	–	R	Bit[7:0]: X direction end position in sensor array[7:0]
0x5736	OTP_DPC_3615_D2V2_26	–	R	Bit[7:5]: Reserved Bit[4:0]: X direction increase step of even points
0x5737	OTP_DPC_3615_D2V2_27	–	R	Bit[7:5]: Reserved Bit[4:0]: X direction increase step of odd points

table 6-54 OTP_S registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x5738	OTP_DPC_3615_D2V2_28	–	R	Bit[7:5]: Reserved Bit[4:0]: Y direction increase step of even points
0x5739	OTP_DPC_3615_D2V2_29	–	R	Bit[7:5]: Reserved Bit[4:0]: Y direction increase step of odd points
0x573A	OTP_DPC_3615_D2V2_2A	–	R	Bit[7]: Y direction BW binning Bit[6]: Y direction bin4 Bit[5]: Y direction bin3 Bit[4]: Y direction bin2 Bit[3]: X direction BW binning Bit[2]: X direction bin4 Bit[1]: X direction bin3 Bit[0]: X direction bin2
0x573B	OTP_DPC_3615_D2V2_2B	–	R	Bit[7:0]: Data of debug address in OTP eFUSE
0x573C	OTP_DPC_3615_D2V2_2C	–	R	Bit[7:0]: X direction offset in sensor array[15:8]
0x573D	OTP_DPC_3615_D2V2_2D	–	R	Bit[7:0]: X direction offset in sensor array[7:0]
0x573E	OTP_DPC_3615_D2V2_2E	–	R	Bit[7:0]: X direction end position in sensor array[15:8]
0x543F	OTP_DPC_3615_D2V2_2F	–	R	Bit[7:0]: X direction end position in sensor array[7:0]
0x5740	OTP_DPC_3615_D2V2_30	–	R	Bit[7:0]: Software version
0x5741	OTP_DPC_3615_D2V2_31	–	R	Bit[7:0]: Hardware version

6.55 DPC_S [0x5750 - 0x5777]

table 6-55 DPC_S registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5750~ 0x5751	NOT USED	–	–	Not Used
0x5752	DPC_1715_D2V2_2	0x03	RW	Bit[7:4]: Not used Bit[3]: Enable manual mode Bit[2]: Enable cross cluster correction Bit[1]: Enable black pixel correction Bit[0]: Enable white pixel correction
0x5753	DPC_1715_D2V2_3	0x0C	RW	Bit[7]: Not used Bit[6]: Line data select 0: Use dummy line data 1: Last two lines re-use bound data Bit[5]: HDR/SBS select 0: HDR 1: SBS Bit[4]: algorithm_opt Bit[3:2]: Edge filling option Bit[1:0]: RGB/G/BR select 00: RGB 01: G 10: Not used 11: BR
0x5754	DPC_1715_D2V2_4	0x04	RW	Bit[7:0]: White pixel threshold list[0]
0x5755	DPC_1715_D2V2_5	0x04	RW	Bit[7:0]: White pixel threshold list[1]
0x5756	DPC_1715_D2V2_6	0x04	RW	Bit[7:0]: White pixel threshold list[2]
0x5757	DPC_1715_D2V2_7	0x04	RW	Bit[7:0]: White pixel threshold list[3]
0x5758	DPC_1715_D2V2_8	0x04	RW	Bit[7:0]: Black pixel threshold list[0]
0x5759	DPC_1715_D2V2_9	0x04	RW	Bit[7:0]: Black pixel threshold list[1]
0x575A	DPC_1715_D2V2_A	0x04	RW	Bit[7:0]: Black pixel threshold list[2]
0x575B	DPC_1715_D2V2_B	0x04	RW	Bit[7:0]: Black pixel threshold list[3]
0x575C	NOT USED	–	–	Not Used
0x575D	DPC_1715_D2V2_D	0x03	RW	Bit[7:0]: Gain control point[0]
0x575E	DPC_1715_D2V2_E	0x08	RW	Bit[7:0]: Gain control point[1]
0x575F	DPC_1715_D2V2_F	0x0C	RW	Bit[7:0]: Gain control point[2]
0x5760	DPC_1715_D2V2_10	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[0]

table 6-55 DPC_S registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5761	DPC_1715_D2V2_11	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[1]
0x5762	DPC_1715_D2V2_12	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[2]
0x5763	DPC_1715_D2V2_13	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Max allowed defect pixel list[3]
0x5764	DPC_1715_D2V2_14	0x08	RW	Bit[7:0]: White couplet defect pixel correction gain threshold
0x5765	DPC_1715_D2V2_15	0x08	RW	Bit[7:4]: Not used Bit[3:0]: White couplet defect pixel correction gain threshold
0x5766	DPC_1715_D2V2_16	0x08	RW	Bit[7:0]: Black couplet defect pixel correction gain threshold
0x5767	DPC_1715_D2V2_17	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Black couplet defect pixel correction gain threshold
0x5768	NOT USED	–	–	Not Used
0x5769	DPC_1715_D2V2_19	0x08	RW	Bit[7:4]: Not used Bit[3:0]: White couplet threshold ratio
0x576A	DPC_1715_D2V2_1A	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Black couplet threshold ratio
0x576B	DPC_1715_D2V2_1B	0xFF	RW	Bit[7:0]: Saturation threshold
0x576C	DPC_1715_D2V2_1C	0x01	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[0]
0x576D	DPC_1715_D2V2_1D	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[1]
0x576E	DPC_1715_D2V2_1E	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[2]
0x576F	DPC_1715_D2V2_1F	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of WP to be corrected[3]
0x5770	DPC_1715_D2V2_20	0x01	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[0]
0x5771	DPC_1715_D2V2_21	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[1]
0x5772	DPC_1715_D2V2_22	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[2]
0x5773	DPC_1715_D2V2_23	0x04	RW	Bit[7:3]: Not used Bit[2:0]: Max number of BP to be corrected[3]

table 6-55 DPC_S registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5774~ 0x5775	NOT USED	–	–	Not Used
0x5776	DPC_1715_D2V2_26	–	R	Bit[7:0]: dpc_ver[15:8]
0x5777	DPC_1715_D2V2_27	–	R	Bit[7:0]: dpc_ver[7:0]

6.56 RAW_BIN_S [0x5780 - 0x578C]

table 6-56 RAW_BIN_S registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5780	RAW_BIN_1315_D2V2_TOP_0	0xC5	RW	Bit[7:3]: m_nVFilter[0] Vertical filter coefficients Bit[2]: m_bPDCheck_enable Enable PD check Bit[1]: m_bVBinningEnable Enable Vertical Binning Bit[0]: m_bHBinningEnable Enable Horizontal Binning
0x5781	RAW_BIN_1315_D2V2_TOP_1	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilter[1] Vertical filter coefficients
0x5782	RAW_BIN_1315_D2V2_TOP_2	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilter[2] Vertical filter coefficients
0x5783	RAW_BIN_1315_D2V2_TOP_3	0x18	RW	Bit[7:5]: Not used Bit[4:0]: m_nVFilter[3] Vertical filter coefficients
0x5784	RAW_BIN_1315_D2V2_TOP_4	0x18	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[0] Horizontal filter coefficients
0x5785	RAW_BIN_1315_D2V2_TOP_5	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[1] Horizontal filter coefficients
0x5786	RAW_BIN_1315_D2V2_TOP_6	0x08	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[2] Horizontal filter coefficients

table 6-56 RAW_BIN_S registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5787	RAW_BIN_1315_D2V2_TOP_7	0x18	RW	Bit[7:5]: Not used Bit[4:0]: m_nHFilter[3] Horizontal filter coefficients
0x5788	RAW_BIN_1315_D2V2_TOP_8	0x05	RW	Bit[7:6]: Not used Bit[5:0]: m_nVFilterShift Vertical filter shift
0x5789	RAW_BIN_1315_D2V2_TOP_9	0x05	RW	Bit[7:6]: Not used Bit[5:0]: m_nHFilterShift Horizontal filter shift
0x578A	RAW_BIN_1315_D2V2_TOP_A	0x00	RW	Bit[7:3]: Not used Bit[2]: m_bKeepBLC Keep BLC same for BWBinSum Bit[1]: BWBinSumEn BWBin sum enable option Bit[0]: m_bBWBin BW bin enable
0x578B	RAW_BIN_1315_D2V2_TOP_C	–	R	Bit[7:0]: RAW BIN version[15:8]
0x578C	RAW_BIN_1315_D2V2_TOP_D	–	R	Bit[7:0]: RAW BIN version[7:0]

6.57 BINC_S [0x57B0 - 0x57C7]

table 6-57 BINC_S registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x57B0	BINC_1215_D2V2_0	0x10	RW	Bit[7:6]: Not used Bit[5]: m_bEnableHCorrection Range is [0:1] Bit[4]: m_bEnableVCorrection Range is [0:1] Bit[3]: m_bHDRBin_RGBIr Range is [0:1] Bit[2]: m_bIndex_manual Range is [0:1] Bit[1]: m_nFlip_manual Range is [0:1] Bit[0]: m_nMirror_manual Range is [0:1]
0x57B1	BINC_1215_D2V2_1	0x0E	RW	Bit[7:6]: Not used Bit[5:4]: m_nVIndex[1:0] Bit[3:0]: m_nHIndex[3:0]

table 6-57 BINC_S registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x57B2	BINC_1215_D2V2_2	0x0E	RW	Bit[7:4]: m_nVIndex_manual[3:0] Bit[3:0]: m_nHIndex_manual[3:0]
0x57B3	BINC_1215_D2V2_3	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: m_pFilterV[0][4:0] Range is [0:31]
0x57B4	NOT USED	–	–	Not Used
0x57B5	BINC_1215_D2V2_5	0x02	RW	Bit[7:5]: Not used Bit[4:0]: m_pFilterV[1][4:0] Range is [0:31]
0x57B6	BINC_1215_D2V2_6	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[0][8] Range is [-256:255]
0x57B7	BINC_1215_D2V2_7	0x00	RW	Bit[7:0]: m_pFilterH[0][7:0] Range is [-256:255]
0x57B8	BINC_1215_D2V2_8	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[1][8] Range is [-256:255]
0x57B9	BINC_1215_D2V2_9	0x70	RW	Bit[7:0]: m_pFilterH[1][7:0] Range is [-256:255]
0x57BA	BINC_1215_D2V2_A	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[2][8] Range is [-256:255]
0x57BB	BINC_1215_D2V2_B	0x10	RW	Bit[7:0]: m_pFilterH[2][7:0] Range is [-256:255]
0x57BC	BINC_1215_D2V2_C	0x00	RW	Bit[7:1]: Not used Bit[0]: m_pFilterH[3][8] Range is [-256:255]
0x57BD	BINC_1215_D2V2_D	0x00	RW	Bit[7:0]: m_pFilterH[3][7:0] Range is [-256:255]
0x57BE~ 0x57C6	RSVD	–	–	Reserved
0x57C7	BINC_1215_D2V2_17	0x10	RW	Bit[7:5]: Reserved Bit[4]: snr_flip_sel Bit[3]: Reserved Bit[2]: clk_gate_disable_man for buffer Bit[1]: Reserved Bit[0]: clk_gate_disable_man for process[3:0]

6.58 PDF_S [0x57D0 - 0x581B]

table 6-58 PDF_S registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x57D0	PDF_3245_D2V2_TOP_0	0xC2	RW	Bit[7]: Use chromatic information enable Bit[6]: Enable PD correction or not Range is [0:1] Bit[5]: Enable single defect pixel removal Range is [0:1] Bit[4]: Rb adaptive correction enable Range is [0:1] Bit[3]: G adaptive correction enable Range is [0:1] Bit[2]: Use corner information enable Range is [0:1] Bit[1]: Use chromatic information enable Range is [0:1] Bit[0]: Is ML 2x2 pattern or not Range is [0:1]
0x57D1	PDF_3245_D2V2_TOP_1	0x08	RW	Bit[7]: Not used Bit[6]: Skip PD on B Bit[5]: Skip PD on G Bit[4:0]: Weight C Range is [0:16]
0x57D2	PDF_3245_D2V2_TOP_2	0x84	RW	Bit[7]: Control every PD and shadow Range is [0:1] Bit[6]: Control every PD and shadow Range is [0:1] Bit[5]: Control every PD and shadow Range is [0:1] Bit[4]: Control every PD and shadow Range is [0:1] Bit[3]: Control every PD and shadow Range is [0:1] Bit[2]: Control every PD and shadow Range is [0:1] Bit[1]: Control every PD and shadow Range is [0:1] Bit[0]: Control every PD and shadow Range is [0:1]

table 6-58 PDF_S registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x57D3	PDF_3245_D2V2_TOP_3	0x04	RW	Bit[7:5]: Not used Bit[4]: Control every PD and shadow Range is [0:1] Bit[3]: Control every PD and shadow Range is [0:1] Bit[2:1]: Direction based method PD correction method enable Range is [0:2] Bit[0]: m_bPDDebugMode_ Range is [0:1]
0x57D4	PDF_3245_D2V2_TOP_4	0x00	RW	Bit[7]: Enable PD/shadow ext or not Range is [0:1] Bit[6]: Enable PD/shadow ext or not Range is [0:1] Bit[5]: Enable PD/shadow ext or not Range is [0:1] Bit[4]: Enable PD/shadow ext or not Range is [0:1] Bit[3]: Enable PD/shadow ext or not Range is [0:1] Bit[2]: Enable PD/shadow ext or not Range is [0:1] Bit[1]: Enable PD/shadow ext or not Range is [0:1] Bit[0]: Enable PD/shadow ext or not Range is [0:1]
0x57D5	PDF_3245_D2V2_TOP_5	0x02	RW	Bit[7]: Enable PD/shadow ext or not Range is [0:1] Bit[6]: Enable PD/shadow ext or not Range is [0:1] Bit[5:4]: G diag option Range is [0:3] Bit[3]: Single defect pixel removal option Range is [0:1] Bit[2:0]: Single defect pixel removal shift bit Range is [0:7]
0x57D6	PDF_3245_D2V2_TOP_6	0x04	RW	Bit[7:0]: Single defect pixel threshold Range is [0:255]
0x57D7	PDF_3245_D2V2_TOP_7	0x11	RW	Bit[7:6]: m_ nDirWeightScaleBit Range is [0:3] Bit[5:4]: m_nDirWeightCurveNum Range is [0:3] Bit[3:2]: m_nBilWeightScaleBit Range is [0:3] Bit[1:0]: m_nBilWeightCurveNum Range is [0:3]

table 6-58 PDF_S registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x57D8	PDF_3245_D2V2_TOP_8	0x08	RW	Bit[7:6]: Not used Bit[5:0]: PD X cycle Range is [1:64]
0x57D9	PDF_3245_D2V2_TOP_9	0x10	RW	Bit[7:6]: Not used Bit[5:0]: PD Y cycle Range is [1:64]
0x57DA	PDF_3245_D2V2_TOP_A	0x02	RW	Bit[7:5]: Not used Bit[4:0]: PD X1 start Range is [0:31]
0x57DB	PDF_3245_D2V2_TOP_B	0x02	RW	Bit[7:5]: Not used Bit[4:0]: PD X2 start Range is [0:31]
0x57DC	PDF_3245_D2V2_TOP_C	0x06	RW	Bit[7:5]: Not used Bit[4:0]: PD X3 start Range is [0:31]
0x57DD	PDF_3245_D2V2_TOP_D	0x06	RW	Bit[7:5]: Not used Bit[4:0]: PD X4 start Range is [0:31]
0x57DE	PDF_3245_D2V2_TOP_E	0x02	RW	Bit[7:5]: Not used Bit[4:0]: PD Y1 start Range is [0:31]
0x57DF	PDF_3245_D2V2_TOP_F	0x06	RW	Bit[7:5]: Not used Bit[4:0]: PD Y2 start Range is [0:31]
0x57E0	PDF_3245_D2V2_TOP_10	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: PD Y3 start Range is [0:31]
0x57E1	PDF_3245_D2V2_TOP_11	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: PD Y4 start Range is [0:31]
0x57E2	PDF_3245_D2V2_TOP_12	0x00	RW	Bit[7:5]: Not used Bit[4:0]: PD X skip Range is [0:31]
0x57E3	PDF_3245_D2V2_TOP_13	0x00	RW	Bit[7:5]: Not used Bit[4:0]: PD Y skip Range is [0:31]
0x57E4	PDF_3245_D2V2_TOP_14	0xFF	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x57E5	PDF_3245_D2V2_TOP_15	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]

table 6-58 PDF_S registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x57E6	PDF_3245_D2V2_TOP_16	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x57E7	PDF_3245_D2V2_TOP_17	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x57E8	PDF_3245_D2V2_TOP_18	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x57E9	PDF_3245_D2V2_TOP_19	0xFF	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x57EA	PDF_3245_D2V2_TOP_1A	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x57EB	PDF_3245_D2V2_TOP_1B	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x57EC	PDF_3245_D2V2_TOP_1C	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x57ED	PDF_3245_D2V2_TOP_1D	0x10	RW	Bit[7:0]: PD/shadow threshold ratio Range is [0:255]
0x57EE	PDF_3245_D2V2_TOP_1E	0x00	RW	Bit[7:0]: 1x noise level for PD correction Range is [0:255]
0x57EF	PDF_3245_D2V2_TOP_1F	0x00	RW	Bit[7:0]: 4x noise level for PD correction Range is [0:255]
0x57F0	PDF_3245_D2V2_TOP_20	0x00	RW	Bit[7:0]: 8x noise level for PD correction Range is [0:255]
0x57F1	PDF_3245_D2V2_TOP_21	0xAA	RW	Bit[7:6]: PD ch 1 Range is [0:3] Bit[5:4]: PD ch 2 Range is [0:3] Bit[3:2]: PD ch 3 Range is [0:3] Bit[1:0]: PD ch 4 Range is [0:3]
0x57F2	PDF_3245_D2V2_TOP_22	0x80	RW	Bit[7:0]: PD adaptive strength low threshold 1x Range is [0:255]
0x57F3	PDF_3245_D2V2_TOP_23	0x80	RW	Bit[7:0]: PD adaptive strength low threshold 4x Range is [0:255]
0x57F4	PDF_3245_D2V2_TOP_24	0x80	RW	Bit[7:0]: PD adaptive strength low threshold 8x Range is [0:255]
0x57F5	PDF_3245_D2V2_TOP_25	0xFF	RW	Bit[7:0]: PD adaptive strength high threshold 1x Range is [0:255]

table 6-58 PDF_S registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x57F6	PDF_3245_D2V2_TOP_26	0xFF	RW	Bit[7:0]: PD adaptive strength high threshold 8x Range is [0:255]
0x57F7	PDF_3245_D2V2_TOP_27	0xFF	RW	Bit[7:0]: PD adaptive strength high threshold 8x Range is [0:255]
0x57F8	PDF_3245_D2V2_TOP_28	0x0A	RW	Bit[7:0]: Shadow edge threshold low 1x Range is [0:255]
0x57F9	PDF_3245_D2V2_TOP_29	0x0A	RW	Bit[7:0]: Shadow edge threshold low 4x Range is [0:255]
0x57FA	PDF_3245_D2V2_TOP_2A	0x0A	RW	Bit[7:0]: Shadow edge threshold low 8x Range is [0:255]
0x57FB	PDF_3245_D2V2_TOP_2B	0x14	RW	Bit[7:0]: Shadow edge threshold high 1x Range is [0:255]
0x57FC	PDF_3245_D2V2_TOP_2C	0x14	RW	Bit[7:0]: Shadow edge threshold high 4x Range is [0:255]
0x57FD	PDF_3245_D2V2_TOP_2D	0x14	RW	Bit[7:0]: Shadow edge threshold high 8x Range is [0:255]
0x57FE	PDF_3245_D2V2_TOP_2E	0x00	RW	Bit[7:0]: Flat threshold Range is [0:255]
0x57FF	PDF_3245_D2V2_TOP_2F	0x00	RW	Bit[7:0]: Inte threshold Range is [0:255]
0x5800	PDF_3245_D2V2_TOP_30	0x12	RW	Bit[7:6]: Not used Bit[5:0]: Image width[13:8] Range is [0:16383]
0x5801	PDF_3245_D2V2_TOP_31	0x20	RW	Bit[7:0]: Image width[7:0] Range is [0:16383]
0x5802	PDF_3245_D2V2_TOP_32	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: Image height[12:8] Range is [0:8191]
0x5803	PDF_3245_D2V2_TOP_33	0xA0	RW	Bit[7:0]: Image height[7:0] Range is [0:8191]
0x5804	PDF_3245_D2V2_TOP_34	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Window start X[13:8] Range is [0:16383]
0x5805	PDF_3245_D2V2_TOP_35	0x10	RW	Bit[7:0]: Window start X[7:0] Range is [0:16383]
0x5806	PDF_3245_D2V2_TOP_36	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Window start Y[12:8] Range is [0:8191]

table 6-58 PDF_S registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x5807	PDF_3245_D2V2_TOP_37	0x10	RW	Bit[7:0]: Window start Y[7:0] Range is [0:8191]
0x5808	PDF_3245_D2V2_TOP_38	0x12	RW	Bit[7:6]: Not used Bit[5:0]: Window width[13:8] Range is [0:16383]
0x5809	PDF_3245_D2V2_TOP_39	0x00	RW	Bit[7:0]: Window width[7:0] Range is [0:16383]
0x580A	PDF_3245_D2V2_TOP_3A	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: Window height[12:8] Range is [0:8191]
0x580B	PDF_3245_D2V2_TOP_3B	0x80	RW	Bit[7:0]: Window height[7:0] Range is [0:8191]
0x580C	PDF_3245_D2V2_TOP_3C	0x00	RW	Bit[7:6]: Not used Bit[5]: vcnt_out_en Bit[4]: hcnt_out_en Bit[3]: cnt_output_en Bit[2]: engine2_off_en Bit[1]: fix_ptn_mode Bit[0]: fix_ptn_en
0x580D	PDF_3245_D2V2_TOP_3D	0x08	RW	Bit[7:4]: Not used Bit[3]: pd_cnt_clr_man_en Bit[2]: pd_win_man_en Bit[1]: xoffset_man_en Bit[0]: yoffset_man_en
0x580E	PDF_3245_D2V2_TOP_3E	0x00	RW	Bit[7:0]: r_gate_dis[7:0]
0x580F	PDF_3245_D2V2_TOP_3F	0x00	RW	Bit[7:0]: r_gate_dis[15:8]
0x5810	PDF_3245_D2V2_TOP_40	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Xoffset[13:8] Range is [0:16383]
0x5811	PDF_3245_D2V2_TOP_41	0x00	RW	Bit[7:0]: Xoffset[7:0] Range is [0:16383]
0x5812	PDF_3245_D2V2_TOP_42	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Yoffset[12:8] Range is [0:8191]
0x5813	PDF_3245_D2V2_TOP_43	0x00	RW	Bit[7:0]: Yoffset[7:0] Range is [0:8191]
0x5814	PDF_3245_D2V2_TOP_44	0x00	RW	Bit[7:4]: Not used Bit[3:0]: offset_c Range is [0:15]

table 6-58 PDF_S registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x5815	PDF_3245_D2V2_TOP_45	0x05	RW	Bit[7:5]: Not used Bit[4]: PDswitch Range is [0:1] Bit[3]: median_option Range is [0:1] Bit[2:0]: DirWeightCurveNumSquare Range is [0:3]
0x5816	PDF_3245_D2V2_TOP_46	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Xoffset1[13:8] Range is [0:16383]
0x5817	PDF_3245_D2V2_TOP_47	0x00	RW	Bit[7:0]: Xoffset1[7:0] Range is [0:16383]
0x5818~ 0x5819	NOT USED	–	–	Not Used
0x581A	PDF_3245_D2V2_TOP_4A	–	R	Bit[7:0]: Version[15:8]
0x581B	PDF_3245_D2V2_TOP_4B	–	R	Bit[7:0]: Version[7:0]

6.59 PDC_S [0x5850 - 0x594C]

table 6-59 PDC_S registers (sheet 1 of 11)

address	register name	default value	R/W	description
0x5850	PDC_3245_D2V2_TOP_0	0x6C	RW	Bit[7:6]: Not used Bit[5]: m_bML2x2HS Bit[4]: m_bByPassHighComp Bit[3]: m_nPDDOption Bit[2]: m_nEnablePreCompensate Bit[1]: m_nBypassPDCompensation Bit[0]: pdc_map_en
0x5851	PDC_3245_D2V2_TOP_1	0x00	RW	Bit[7:3]: Not used Bit[2]: m_bCurveFlip Bit[1]: m_bCurveMirror Bit[0]: m_nBinCurveEnable

table 6-59 PDC_S registers (sheet 2 of 11)

address	register name	default value	R/W	description
0x5852	PDC_3245_D2V2_TOP_2	0x00	RW	Bit[7]: man_focuswin_en Bit[6]: win_man_en Bit[5]: yoffset_man_en Bit[4]: xoffset_man_en Bit[3]: man_ml2x2ptn_en Bit[2]: man_flip_en Bit[1]: man_mirror_en Bit[0]: man_bin_en
0x5853	PDC_3245_D2V2_TOP_3	0x00	RW	Bit[7:2]: Not used Bit[1]: man_scaler_en Bit[0]: man_pd_en
0x5854	PDC_3245_D2V2_TOP_4	0x00	RW	Bit[7]: Not used Bit[6]: man_ml2x2pattern Bit[5]: man_flip Bit[4]: man_mirror Bit[3:2]: Not used Bit[1]: man_vbin Bit[0]: man_hbin
0x5855	NOT USED	–	–	Not Used
0x5856	PDC_3245_D2V2_TOP_6	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nOffsetX>>8[13:8]
0x5857	PDC_3245_D2V2_TOP_7	0x10	RW	Bit[7:0]: m_nOffsetX[7:0]
0x5858	PDC_3245_D2V2_TOP_8	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nOffsetY>>8[13:8]
0x5859	PDC_3245_D2V2_TOP_9	0x00	RW	Bit[7:0]: m_nOffsetY[7:0]
0x585A	PDC_3245_D2V2_TOP_A	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinXStart>>8[13:8]
0x585B	PDC_3245_D2V2_TOP_B	0x00	RW	Bit[7:0]: m_nWinXStart[7:0]
0x585C	PDC_3245_D2V2_TOP_C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinYStart>>8[13:8]
0x585D	PDC_3245_D2V2_TOP_D	0x00	RW	Bit[7:0]: m_nWinYStart[7:0]
0x585E	PDC_3245_D2V2_TOP_E	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinWidth>>8[13:8]
0x585F	PDC_3245_D2V2_TOP_F	0x80	RW	Bit[7:0]: m_nWinWidth[7:0]
0x5860	PDC_3245_D2V2_TOP_10	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nWinHeight>>8[13:8]
0x5861	PDC_3245_D2V2_TOP_11	0xA0	RW	Bit[7:0]: m_nWinHeight[7:0]
0x5862	PDC_3245_D2V2_TOP_12	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinLeft>>8[13:8]

table 6-59 PDC_S registers (sheet 3 of 11)

address	register name	default value	R/W	description
0x5863	PDC_3245_D2V2_TOP_13	0x00	RW	Bit[7:0]: m_nFocusWinLeft[7:0]
0x5864	PDC_3245_D2V2_TOP_14	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinTop>>8[13:8]
0x5865	PDC_3245_D2V2_TOP_15	0x00	RW	Bit[7:0]: m_nFocusWinTop[7:0]
0x5866	PDC_3245_D2V2_TOP_16	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinWidth>>8[13:8]
0x5867	PDC_3245_D2V2_TOP_17	0x80	RW	Bit[7:0]: m_nFocusWinWidth[7:0]
0x5868	PDC_3245_D2V2_TOP_18	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinHeight>>8[13:8]
0x5869	PDC_3245_D2V2_TOP_19	0xA0	RW	Bit[7:0]: m_nFocusWinHeight[7:0]
0x586A	PDC_3245_D2V2_TOP_1A	0x10	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDCycleX[5:0]
0x586B	PDC_3245_D2V2_TOP_1B	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDCycleY[5:0]
0x586C	PDC_3245_D2V2_TOP_1C	0x01	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDSkipX[4:0]
0x586D	PDC_3245_D2V2_TOP_1D	0x01	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDSkipY[4:0]
0x586E	PDC_3245_D2V2_TOP_1E	0x04	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX1[4:0]
0x586F	PDC_3245_D2V2_TOP_1F	0x04	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX2[4:0]
0x5870	PDC_3245_D2V2_TOP_20	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX3[4:0]
0x5871	PDC_3245_D2V2_TOP_21	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDX4[4:0]
0x5872	PDC_3245_D2V2_TOP_22	0x04	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY1[4:0]
0x5873	PDC_3245_D2V2_TOP_23	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY2[4:0]
0x5874	PDC_3245_D2V2_TOP_24	0x14	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY3[4:0]
0x5875	PDC_3245_D2V2_TOP_25	0x1C	RW	Bit[7:5]: Not used Bit[4:0]: m_nPDY4[4:0]
0x5876	PDC_3245_D2V2_TOP_26	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh1

table 6-59 PDC_S registers (sheet 4 of 11)

address	register name	default value	R/W	description
0x5877	PDC_3245_D2V2_TOP_27	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh2
0x5878	PDC_3245_D2V2_TOP_28	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh3
0x5879	PDC_3245_D2V2_TOP_29	0x02	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDCh4
0x587A	PDC_3245_D2V2_TOP_2A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDFadingScalerH>>8[9:8]
0x587B	PDC_3245_D2V2_TOP_2B	0x40	RW	Bit[7:0]: m_nPDFadingScalerH[7:0]
0x587C	PDC_3245_D2V2_TOP_2C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: m_nPDFadingScalerV>>8[9:8]
0x587D	PDC_3245_D2V2_TOP_2D	0x56	RW	Bit[7:0]: m_nPDFadingScalerV[7:0]
0x587E	PDC_3245_D2V2_TOP_2E	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nBinNumA[3:0]
0x587F	PDC_3245_D2V2_TOP_2F	0x01	RW	Bit[7:4]: Not used Bit[3:0]: m_nBinNumB[3:0]
0x5880	PDC_3245_D2V2_TOP_30	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDWidth_ori>>8[13:8]
0x5881	PDC_3245_D2V2_TOP_31	0x80	RW	Bit[7:0]: m_nPDWidth_ori[7:0]
0x5882	PDC_3245_D2V2_TOP_32	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDHeight_ori>>8[13:8]
0x5883	PDC_3245_D2V2_TOP_33	0xA0	RW	Bit[7:0]: m_nPDHeight_ori[7:0]
0x5884	PDC_3245_D2V2_TOP_34	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nArrayWidth>>8[13:8]
0x5885	PDC_3245_D2V2_TOP_35	0x80	RW	Bit[7:0]: m_nArrayWidth[7:0]
0x5886	PDC_3245_D2V2_TOP_36	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nArrayHeight>>8[13:8]
0x5887	PDC_3245_D2V2_TOP_37	0xA0	RW	Bit[7:0]: m_nArrayHeight[7:0]
0x5888	PDC_3245_D2V2_TOP_38	0x0F	RW	Bit[7:6]: Not used Bit[5:0]: m_nOffsetX>>8[13:8]
0x5889	PDC_3245_D2V2_TOP_39	0xB8	RW	Bit[7:0]: m_nOffsetX[7:0]
0x588A	PDC_3245_D2V2_TOP_3A	0x00	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinLeft>>8[13:8]
0x588B	PDC_3245_D2V2_TOP_3B	0x00	RW	Bit[7:0]: m_nFocusWinLeft[7:0]

table 6-59 PDC_S registers (sheet 5 of 11)

address	register name	default value	R/W	description
0x588C	PDC_3245_D2V2_TOP_3C	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nFocusWinWidth>>8[13:8]
0x588D	PDC_3245_D2V2_TOP_3D	0x80	RW	Bit[7:0]: m_nFocusWinWidth[7:0]
0x588E~ 0x588F	NOT USED	–	–	Not Used
0x5890	PDC_3245_D2V2_TOP_40	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[0]>>8[15:8]
0x5891	PDC_3245_D2V2_TOP_41	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[0][7:0]
0x5892	PDC_3245_D2V2_TOP_42	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[1]>>8[15:8]
0x5893	PDC_3245_D2V2_TOP_43	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[1][7:0]
0x5894	PDC_3245_D2V2_TOP_44	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[2]>>8[15:8]
0x5895	PDC_3245_D2V2_TOP_45	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[2][7:0]
0x5896	PDC_3245_D2V2_TOP_46	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[3]>>8[15:8]
0x5897	PDC_3245_D2V2_TOP_47	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[3][7:0]
0x5898	PDC_3245_D2V2_TOP_48	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[4]>>8[15:8]
0x5899	PDC_3245_D2V2_TOP_49	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[4][7:0]
0x589A	PDC_3245_D2V2_TOP_4A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[5]>>8[15:8]
0x589B	PDC_3245_D2V2_TOP_4B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[5][7:0]
0x589C	PDC_3245_D2V2_TOP_4C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[6]>>8[15:8]
0x589D	PDC_3245_D2V2_TOP_4D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[6][7:0]
0x589E	PDC_3245_D2V2_TOP_4E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[7]>>8[15:8]
0x589F	PDC_3245_D2V2_TOP_4F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[7][7:0]
0x58A0	PDC_3245_D2V2_TOP_50	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[8]>>8[15:8]
0x58A1	PDC_3245_D2V2_TOP_51	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[8][7:0]
0x58A2	PDC_3245_D2V2_TOP_52	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[9]>>8[15:8]
0x58A3	PDC_3245_D2V2_TOP_53	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[9][7:0]
0x58A4	PDC_3245_D2V2_TOP_54	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[10]>>8[15:8]
0x58A5	PDC_3245_D2V2_TOP_55	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[10][7:0]
0x58A6	PDC_3245_D2V2_TOP_56	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[11]>>8[15:8]
0x58A7	PDC_3245_D2V2_TOP_57	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[11][7:0]
0x58A8	PDC_3245_D2V2_TOP_58	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[12]>>8[15:8]
0x58A9	PDC_3245_D2V2_TOP_59	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[12][7:0]

table 6-59 PDC_S registers (sheet 6 of 11)

address	register name	default value	R/W	description
0x58AA	PDC_3245_D2V2_TOP_5A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[13]>>8[15:8]
0x58AB	PDC_3245_D2V2_TOP_5B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[13][7:0]
0x58AC	PDC_3245_D2V2_TOP_5C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[14]>>8[15:8]
0x58AD	PDC_3245_D2V2_TOP_5D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[14][7:0]
0x58AE	PDC_3245_D2V2_TOP_5E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[15]>>8[15:8]
0x58AF	PDC_3245_D2V2_TOP_5F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[15][7:0]
0x58B0	PDC_3245_D2V2_TOP_60	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[16]>>8[15:8]
0x58B1	PDC_3245_D2V2_TOP_61	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[16][7:0]
0x58B2	PDC_3245_D2V2_TOP_62	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[17]>>8[15:8]
0x58B3	PDC_3245_D2V2_TOP_63	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[17][7:0]
0x58B4	PDC_3245_D2V2_TOP_64	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[18]>>8[15:8]
0x58B5	PDC_3245_D2V2_TOP_65	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[18][7:0]
0x58B6	PDC_3245_D2V2_TOP_66	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[19]>>8[15:8]
0x58B7	PDC_3245_D2V2_TOP_67	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[19][7:0]
0x58B8	PDC_3245_D2V2_TOP_68	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[20]>>8[15:8]
0x58B9	PDC_3245_D2V2_TOP_69	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[20][7:0]
0x58BA	PDC_3245_D2V2_TOP_6A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[21]>>8[15:8]
0x58BB	PDC_3245_D2V2_TOP_6B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[21][7:0]
0x58BC	PDC_3245_D2V2_TOP_6C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[22]>>8[15:8]
0x58BD	PDC_3245_D2V2_TOP_6D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[22][7:0]
0x58BE	PDC_3245_D2V2_TOP_6E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[23]>>8[15:8]
0x58BF	PDC_3245_D2V2_TOP_6F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[23][7:0]
0x58C0	PDC_3245_D2V2_TOP_70	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[24]>>8[15:8]
0x58C1	PDC_3245_D2V2_TOP_71	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[24][7:0]
0x58C2	PDC_3245_D2V2_TOP_72	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[25]>>8[15:8]
0x58C3	PDC_3245_D2V2_TOP_73	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[25][7:0]
0x58C4	PDC_3245_D2V2_TOP_74	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[26]>>8[15:8]
0x58C5	PDC_3245_D2V2_TOP_75	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[26][7:0]
0x58C6	PDC_3245_D2V2_TOP_76	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[27]>>8[15:8]
0x58C7	PDC_3245_D2V2_TOP_77	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[27][7:0]

table 6-59 PDC_S registers (sheet 7 of 11)

address	register name	default value	R/W	description
0x58C8	PDC_3245_D2V2_TOP_78	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[28]>>8[15:8]
0x58C9	PDC_3245_D2V2_TOP_79	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[28][7:0]
0x58CA	PDC_3245_D2V2_TOP_7A	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[29]>>8[15:8]
0x58CB	PDC_3245_D2V2_TOP_7B	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[29][7:0]
0x58CC	PDC_3245_D2V2_TOP_7C	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[30]>>8[15:8]
0x58CD	PDC_3245_D2V2_TOP_7D	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[30][7:0]
0x58CE	PDC_3245_D2V2_TOP_7E	0x01	RW	Bit[7:0]: m_pReverseRatio_opt[31]>>8[15:8]
0x58CF	PDC_3245_D2V2_TOP_7F	0x00	RW	Bit[7:0]: m_pReverseRatio_opt[31][7:0]
0x58D0	PDC_3245_D2V2_TOP_80	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[0][5:0]
0x58D1	PDC_3245_D2V2_TOP_81	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[1][5:0]
0x58D2	PDC_3245_D2V2_TOP_82	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[2][5:0]
0x58D3	PDC_3245_D2V2_TOP_83	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[3][5:0]
0x58D4	PDC_3245_D2V2_TOP_84	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[4][5:0]
0x58D5	PDC_3245_D2V2_TOP_85	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[5][5:0]
0x58D6	PDC_3245_D2V2_TOP_86	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[6][5:0]
0x58D7	PDC_3245_D2V2_TOP_87	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[7][5:0]
0x58D8	PDC_3245_D2V2_TOP_88	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[8][5:0]
0x58D9	PDC_3245_D2V2_TOP_89	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[9][5:0]
0x58DA	PDC_3245_D2V2_TOP_8A	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[10][5:0]
0x58DB	PDC_3245_D2V2_TOP_8B	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[11][5:0]
0x58DC	PDC_3245_D2V2_TOP_8C	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[12][5:0]

table 6-59 PDC_S registers (sheet 8 of 11)

address	register name	default value	R/W	description
0x58DD	PDC_3245_D2V2_TOP_8D	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[13][5:0]
0x58DE	PDC_3245_D2V2_TOP_8E	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[14][5:0]
0x58DF	PDC_3245_D2V2_TOP_8F	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[15][5:0]
0x58E0	PDC_3245_D2V2_TOP_90	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[16][5:0]
0x58E1	PDC_3245_D2V2_TOP_91	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[17][5:0]
0x58E2	PDC_3245_D2V2_TOP_92	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[18][5:0]
0x58E3	PDC_3245_D2V2_TOP_93	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[19][5:0]
0x58E4	PDC_3245_D2V2_TOP_94	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[20][5:0]
0x58E5	PDC_3245_D2V2_TOP_95	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[21][5:0]
0x58E6	PDC_3245_D2V2_TOP_96	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[22][5:0]
0x58E7	PDC_3245_D2V2_TOP_97	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[23][5:0]
0x58E8	PDC_3245_D2V2_TOP_98	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[24][5:0]
0x58E9	PDC_3245_D2V2_TOP_99	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[25][5:0]
0x58EA	PDC_3245_D2V2_TOP_9A	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[26][5:0]
0x58EB	PDC_3245_D2V2_TOP_9B	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[27][5:0]
0x58EC	PDC_3245_D2V2_TOP_9C	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[28][5:0]
0x58ED	PDC_3245_D2V2_TOP_9D	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[29][5:0]
0x58EE	PDC_3245_D2V2_TOP_9E	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[30][5:0]
0x58EF	PDC_3245_D2V2_TOP_9F	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_pBinMapping[31][5:0]

table 6-59 PDC_S registers (sheet 9 of 11)

address	register name	default value	R/W	description
0x58F0	PDC_3245_D2V2_TOP_A0	0x01	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[0][5:0]
0x58F1	PDC_3245_D2V2_TOP_A1	0x02	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[1][5:0]
0x58F2	PDC_3245_D2V2_TOP_A2	0x03	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[2][5:0]
0x58F3	PDC_3245_D2V2_TOP_A3	0x04	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[3][5:0]
0x58F4	PDC_3245_D2V2_TOP_A4	0x05	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[4][5:0]
0x58F5	PDC_3245_D2V2_TOP_A5	0x06	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[5][5:0]
0x58F6	PDC_3245_D2V2_TOP_A6	0x07	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[6][5:0]
0x58F7	PDC_3245_D2V2_TOP_A7	0x08	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[7][5:0]
0x58F8	PDC_3245_D2V2_TOP_A8	0x09	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[8][5:0]
0x58F9	PDC_3245_D2V2_TOP_A9	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[9][5:0]
0x58FA	PDC_3245_D2V2_TOP_AA	0x0B	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[10][5:0]
0x58FB	PDC_3245_D2V2_TOP_AB	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[11][5:0]
0x58FC	PDC_3245_D2V2_TOP_AC	0x0D	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[12][5:0]
0x58FD	PDC_3245_D2V2_TOP_AD	0x0E	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[13][5:0]
0x58FE	PDC_3245_D2V2_TOP_AE	0x0F	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[14][5:0]
0x58FF	PDC_3245_D2V2_TOP_AF	0x10	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[15][5:0]
0x5900	PDC_3245_D2V2_TOP_B0	0x11	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[16][5:0]
0x5901	PDC_3245_D2V2_TOP_B1	0x12	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[17][5:0]
0x5902	PDC_3245_D2V2_TOP_B2	0x13	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[18][5:0]

table 6-59 PDC_S registers (sheet 10 of 11)

address	register name	default value	R/W	description
0x5903	PDC_3245_D2V2_TOP_B3	0x14	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[19][5:0]
0x5904	PDC_3245_D2V2_TOP_B4	0x15	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[20][5:0]
0x5905	PDC_3245_D2V2_TOP_B5	0x16	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[21][5:0]
0x5906	PDC_3245_D2V2_TOP_B6	0x17	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[22][5:0]
0x5907	PDC_3245_D2V2_TOP_B7	0x18	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[23][5:0]
0x5908	PDC_3245_D2V2_TOP_B8	0x19	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[24][5:0]
0x5909	PDC_3245_D2V2_TOP_B9	0x1A	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[25][5:0]
0x590A	PDC_3245_D2V2_TOP_BA	0x1B	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[26][5:0]
0x590B	PDC_3245_D2V2_TOP_BB	0x1C	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[27][5:0]
0x590C	PDC_3245_D2V2_TOP_BC	0x1D	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[28][5:0]
0x590D	PDC_3245_D2V2_TOP_BD	0x1E	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[29][5:0]
0x590E	PDC_3245_D2V2_TOP_BE	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[30][5:0]
0x590F	PDC_3245_D2V2_TOP_BF	0x20	RW	Bit[7:6]: Not used Bit[5:0]: m_nPDShadowChannel[31][5:0]
0x5910	PDC_3245_D2V2_TOP_C0	0x03	RW	Bit[7:4]: Not used Bit[3:0]: m_nOverExpoThre>>8[11:8]
0x5911	PDC_3245_D2V2_TOP_C1	0xFF	RW	Bit[7:0]: m_nOverExpoThre[7:0]
0x5912	PDC_3245_D2V2_TOP_C2	0x00	RW	Bit[7:6]: Not used Bit[5:4]: Calculate start select Bit[3:0]: Replace PD by column/row count in debug mode

table 6-59 PDC_S registers (sheet 11 of 11)

address	register name	default value	R/W	description
0x5913	PDC_3245_D2V2_TOP_C3	0x01	RW	Bit[7:5]: Not used Bit[4]: Firmware write SRAM enable Bit[3:2]: Not used Bit[1:0]: Firmware read SRAM select 00: None 01: L 10: M 11: S
0x5914~ 0x592F	NOT USED	–	–	Not Used
0x5930	PDC_3245_D2V2_TOP_E0	0x00	RW	Bit[7:0]: PD restore control
0x5931	PDC_3245_D2V2_TOP_E1	0x02	RW	Bit[7:4]: Not used Bit[3]: m_bFourCell2PD Bit[2]: m_nPDOption Bit[1:0]: m_bMedianFilterOption
0x5932	PDC_3245_D2V2_TOP_E2	0x42	RW	Bit[7:4]: m_nMedianFilterPixel[0][3:0] Bit[3:0]: m_nMedianFilterPixel[1][3:0]
0x5933	PDC_3245_D2V2_TOP_E3	0x24	RW	Bit[7:4]: m_nMedianFilterPixel[2][3:0] Bit[3:0]: m_nMedianFilterPixel[3][3:0]
0x5934	PDC_3245_D2V2_TOP_E4	0x00	RW	Bit[7:5]: Not used Bit[4:2]: PD restore dbg_cnt_sel Bit[1:0]: PD restore dbg_byt_sel
0x5935~ 0x593F	NOT USED	–	–	Not Used
0x5940	PDC_3245_D2V2_TOP_F0	–	R	Bit[7:0]: PDC version[15:8]
0x5941	PDC_3245_D2V2_TOP_F1	–	R	Bit[7:0]: PDC version[7:0]
0x5942~ 0x5944	NOT USED	–	–	Not Used
0x5945	PDC_3245_D2V2_TOP_F5	–	R	Bit[7:0]: PD counter[23:16]
0x5946	PDC_3245_D2V2_TOP_F6	–	R	Bit[7:0]: PD counter[15:8]
0x5947	PDC_3245_D2V2_TOP_F7	–	R	Bit[7:0]: PD counter[7:0]
0x5948	NOT USED	–	–	Not Used
0x5949	PDC_3245_D2V2_TOP_F9	–	R	Bit[7:0]: PD counter[23:16]
0x594A	PDC_3245_D2V2_TOP_FA	–	R	Bit[7:0]: PD counter[15:8]
0x594B	PDC_3245_D2V2_TOP_FB	–	R	Bit[7:0]: PD counter[7:0]
0x594C	PDC_3245_D2V2_TOP_FC	–	R	Bit[7:0]: PD restore PD VC counter

6.60 RAW_DNS_S [0x5950 - 0x595F]

table 6-60 RAW_DNS_S registers

address	register name	default value	R/W	description
0x5950~ 0x5952	NOT USED	–	–	Not Used
0x5953	RAW_DNS_1055_3	0x05	RW	Bit[7:5]: Reserved Bit[4]: dns_para_man_en Bit[3]: dns_mode Bit[2]: avg_dis_1 Range is [0:1] Bit[1]: avg_dis_0 Range is [0:1] Bit[0]: g_dns_en Range is [0:1]
0x5954	RAW_DNS_1055_4	0x04	RW	Bit[7:0]: dns_noise_list_0 Range is [0:7]
0x5955	RAW_DNS_1055_5	0x08	RW	Bit[7:0]: dns_noise_list_1 Range is [8:15]
0x5956	RAW_DNS_1055_6	0x10	RW	Bit[7:0]: dns_noise_list_2 Range is [16:31]
0x5957	RAW_DNS_1055_7	0x18	RW	Bit[7:0]: dns_noise_list_3 Range is [32:63]
0x5958	RAW_DNS_1055_8	0x20	RW	Bit[7:0]: dns_noise_list_4 Range is [64:95]
0x5959	RAW_DNS_1055_9	0x30	RW	Bit[7:0]: dns_noise_list_5 Range is [96:127]
0x595A	RAW_DNS_1055_A	0x40	RW	Bit[7:0]: dns_noise_list_6 Range is [128:191]
0x595B	RAW_DNS_1055_B	0x40	RW	Bit[7:0]: dns_noise_list_7 Range is [192:255]
0x595C~ 0x595E	RSVD	–	–	Reserved
0x595F	RAW_DNS_1055_F	0x08	RW	Bit[7:0]: dns_noise_man

6.61 4CC [0x5980 - 0x59DB]

table 6-61 4CC registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5980	FOURCELLCONVERT_1105_V2D2_0	0x3B	RW	Bit[7]: Use color difference in interpY Bit[6]: Do not add back residuals of B, R for edges Bit[5]: Control if using adaptive wC in CombineHV Bit[4]: Anti-aliasing enable Bit[3]: Enable using original HF for better resolution Bit[2]: Enable HF enhancement Bit[1]: Enable Linear2Log in 4C converter Bit[0]: Enable subtracting BLC in 4C converter
0x5981	FOURCELLCONVERT_1105_V2D2_1	0x14	RW	Bit[7:0]: Noise list
0x5982	FOURCELLCONVERT_1105_V2D2_2	0x1A	RW	Bit[7:0]: Noise list
0x5983	FOURCELLCONVERT_1105_V2D2_3	0x26	RW	Bit[7:0]: Noise list
0x5984	FOURCELLCONVERT_1105_V2D2_4	0x38	RW	Bit[7:0]: Noise list
0x5985	FOURCELLCONVERT_1105_V2D2_5	0x50	RW	Bit[7:0]: Noise list
0x5986	FOURCELLCONVERT_1105_V2D2_6	0x6E	RW	Bit[7:0]: Noise list
0x5987	FOURCELLCONVERT_1105_V2D2_7	0x92	RW	Bit[7:0]: Noise list
0x5988	NOT USED	–	–	Not Used
0x5989	FOURCELLCONVERT_1105_V2D2_9	0x54	RW	Bit[7:4]: Bitforlog Bit[3:0]: Weight of wHC, wVC in CombineHV
0x598A	FOURCELLCONVERT_1105_V2D2_A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Threshold for wHS, wVS adjustment[9:8]
0x598B	FOURCELLCONVERT_1105_V2D2_B	0x64	RW	Bit[7:0]: Threshold for wHS, wVS adjustment[7:0]
0x598C	FOURCELLCONVERT_1105_V2D2_C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Threshold for wHS, wVS adjustment[9:8]

table 6-61 4CC registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x598D	FOURCELLCONVERT_1105_V2D2_D	0x5A	RW	Bit[7:0]: Threshold for wHS, wVS adjustment[7:0]
0x598E	FOURCELLCONVERT_1105_V2D2_E	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Threshold for wHS, wVS adjustment[9:8]
0x598F	FOURCELLCONVERT_1105_V2D2_F	0x50	RW	Bit[7:0]: Threshold for wHS, wVS adjustment[7:0]
0x5990	FOURCELLCONVERT_1105_V2D2_10	0x00	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x5991	FOURCELLCONVERT_1105_V2D2_11	0x02	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x5992	FOURCELLCONVERT_1105_V2D2_12	0x04	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x5993	FOURCELLCONVERT_1105_V2D2_13	0x06	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x5994	FOURCELLCONVERT_1105_V2D2_14	0x08	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x5995	FOURCELLCONVERT_1105_V2D2_15	0x0A	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x5996	FOURCELLCONVERT_1105_V2D2_16	0x0C	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x5997	FOURCELLCONVERT_1105_V2D2_17	0x0F	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x5998	FOURCELLCONVERT_1105_V2D2_18	0x12	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x5999	FOURCELLCONVERT_1105_V2D2_19	0x16	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x599A	FOURCELLCONVERT_1105_V2D2_1A	0x1A	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x599B	FOURCELLCONVERT_1105_V2D2_1B	0x1E	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x599C	FOURCELLCONVERT_1105_V2D2_1C	0x22	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x599D	FOURCELLCONVERT_1105_V2D2_1D	0x27	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x599E	FOURCELLCONVERT_1105_V2D2_1E	0x2C	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV

table 6-61 4CC registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x599F	FOURCELLCONVERT_1105_V2D2_1F	0x32	RW	Bit[7]: Not used Bit[6:0]: m_nWeightS used in CombineHV
0x59A0	NOT USED	–	–	Not Used
0x59A1	FOURCELLCONVERT_1105_V2D2_21	0x04	RW	Bit[7:4]: Not used Bit[3:0]: How much HF will be enhanced
0x59A2	FOURCELLCONVERT_1105_V2D2_22	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: Threshold of HF enhancement
0x59A3	FOURCELLCONVERT_1105_V2D2_23	0x16	RW	Bit[7:6]: Not used Bit[5:0]: Weights for comparison in WeightedInterpolateW
0x59A4	FOURCELLCONVERT_1105_V2D2_24	0x10	RW	Bit[7:6]: Not used Bit[5:0]: Weights for comparison in WeightedInterpolateW
0x59A5	FOURCELLCONVERT_1105_V2D2_25	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: Weights for comparison in WeightedInterpolateW
0x59A6	FOURCELLCONVERT_1105_V2D2_26	0x08	RW	Bit[7:6]: Not used Bit[5:0]: Weights for comparison in WeightedInterpolateW
0x59A7	FOURCELLCONVERT_1105_V2D2_27	0x05	RW	Bit[7:6]: Not used Bit[5:0]: Weights for comparison in WeightedInterpolateW
0x59A8	NOT USED	–	–	Not Used
0x59A9	FOURCELLCONVERT_1105_V2D2_29	0x80	RW	Bit[7:0]: Threshold W_1
0x59AA	FOURCELLCONVERT_1105_V2D2_2A	0x32	RW	Bit[7:0]: Threshold W_2
0x59AB	FOURCELLCONVERT_1105_V2D2_2B	0x18	RW	Bit[7:0]: Threshold W_3
0x59AC	NOT USED	–	–	Not Used
0x59AD	FOURCELLCONVERT_1105_V2D2_2D	0x80	RW	Bit[7:0]: Threshold CD_1
0x59AE	FOURCELLCONVERT_1105_V2D2_2E	0x13	RW	Bit[7:0]: Threshold CD_2
0x59AF	FOURCELLCONVERT_1105_V2D2_2F	0x0D	RW	Bit[7:0]: Threshold CD_3

table 6-61 4CC registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x59B0	FOURCELLCONVERT_1105_V2D2_30	0x06	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59B1	FOURCELLCONVERT_1105_V2D2_31	0x07	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59B2	FOURCELLCONVERT_1105_V2D2_32	0x08	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59B3	FOURCELLCONVERT_1105_V2D2_33	0x09	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59B4	FOURCELLCONVERT_1105_V2D2_34	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59B5	FOURCELLCONVERT_1105_V2D2_35	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59B6	FOURCELLCONVERT_1105_V2D2_36	0x12	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59B7	FOURCELLCONVERT_1105_V2D2_37	0x15	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59B8	FOURCELLCONVERT_1105_V2D2_38	0x17	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59B9	FOURCELLCONVERT_1105_V2D2_39	0x19	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59BA	FOURCELLCONVERT_1105_V2D2_3A	0x1B	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59BB	FOURCELLCONVERT_1105_V2D2_3B	0x1D	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59BC	FOURCELLCONVERT_1105_V2D2_3C	0x1E	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV

table 6-61 4CC registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x59BD	FOURCELLCONVERT_1105_V2D2_3D	0x1F	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59BE	FOURCELLCONVERT_1105_V2D2_3E	0x20	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59BF	FOURCELLCONVERT_1105_V2D2_3F	0x20	RW	Bit[7:6]: Not used Bit[5:0]: Weight_List of wHC, wVC in CombineHV
0x59C0	NOT USED	–	–	Not Used
0x59C1	FOURCELLCONVERT_1105_V2D2_41	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: Threshold for diagonal detection
0x59C2	FOURCELLCONVERT_1105_V2D2_42	0x02	RW	Bit[7:2]: Disable clock gate for sub module Bit[1]: AWB sum enable Bit[0]: Soft reset for awb_sum only
0x59C3	FOURCELLCONVERT_1105_V2D2_43	0x04	RW	Bit[7:4]: Not used Bit[3]: scale_en Bit[2]: dither_en Bit[1]: pvt_det_mode Bit[0]: pvt_det_clr
0x59C4	FOURCELLCONVERT_1105_V2D2_44	0x24	RW	Bit[7:6]: Not used Bit[5:0]: scale_width_out[13:8]
0x59C5	FOURCELLCONVERT_1105_V2D2_45	0x40	RW	Bit[7:0]: scale_width_out[7:0]
0x59C6	FOURCELLCONVERT_1105_V2D2_46	0x1B	RW	Bit[7:5]: Not used Bit[4:0]: scale_height_out[12:8]
0x59C7	FOURCELLCONVERT_1105_V2D2_47	0x40	RW	Bit[7:0]: scale_height_out[7:0]
0x59C8	FOURCELLCONVERT_1105_V2D2_48	0x00	RW	Bit[7:0]: scale_init_phase
0x59C9	FOURCELLCONVERT_1105_V2D2_49	0x00	RW	Bit[7:0]: scale_xoffset_out
0x59CA	FOURCELLCONVERT_1105_V2D2_4A	0x00	RW	Bit[7:0]: scale_yoffset_out
0x59CB	FOURCELLCONVERT_1105_V2D2_4B	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: zoom_anti_alias
0x59CC~ 0x59CF	NOT USED	–	–	Not Used

table 6-61 4CC registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x59D0	FOURCELLCONVERT_1105_V2D2_50	–	R	Bit[7:5]: Not used Bit[4:0]: mean_uv_0[12:8]
0x59D1	FOURCELLCONVERT_1105_V2D2_51	–	R	Bit[7:0]: mean_uv_0[7:0]
0x59D2	FOURCELLCONVERT_1105_V2D2_52	–	R	Bit[7:5]: Not used Bit[4:0]: mean_uv_1[12:8]
0x59D3	FOURCELLCONVERT_1105_V2D2_53	–	R	Bit[7:0]: mean_uv_1[7:0]
0x59D4	FOURCELLCONVERT_1105_V2D2_54	–	R	Bit[7:0]: fourcc_ver[15:8]
0x59D5	FOURCELLCONVERT_1105_V2D2_55	–	R	Bit[7:0]: fourcc_ver[7:0]
0x59D6	FOURCELLCONVERT_1105_V2D2_56	–	R	Bit[7:0]: pvt_det_result[15:8]
0x59D7	FOURCELLCONVERT_1105_V2D2_57	–	R	Bit[7:0]: pvt_det_result[7:0]
0x59D8~ 0x59DA	NOT USED	–	–	Not Used
0x59DB	FOURCELLCONVERT_1105_V2D2_5B	–	R	Bit[7:2]: Not used Bit[1]: pvt_det_overflow Bit[0]: pvt_det_underflow

6.62 XTC [0x5A00 - 0x5A17]

table 6-62 XTC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5A00~ 0x5A01	NOT USED	–	–	Not Used
0x5A02	XTC_1205_D2V2_2	0x0C	RW	Bit[7:5]: Not used Bit[4]: Disable CP out-of-range check Range is [0:1] Bit[3]: Enable dithering Range is [0:1] Bit[2]: Use mean value in step one Range is [0:1] Bit[1]: Enable step two Range is [0:1] Bit[0]: Enable step one Range is [0:1]
0x5A03	XTC_1205_D2V2_3	0x06	RW	Bit[7:3]: Not used Bit[2]: Flip enable Range is [0:1] Bit[1]: Mirror enable Range is [0:1] Bit[0]: Use manual mirror and file enable Range is [0:1]
0x5A04	XTC_1205_D2V2_4	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Left pipe horizontal offset[13:8] Range is [0:9280]
0x5A05	XTC_1205_D2V2_5	0x00	RW	Bit[7:0]: Left pipe horizontal offset[7:0] Range is [0:9280]
0x5A06	XTC_1205_D2V2_6	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Right pipe horizontal offset[13:8] Range is [0:9248]
0x5A07	XTC_1205_D2V2_7	0x00	RW	Bit[7:0]: Right pipe horizontal offset[7:0] Range is [0:9248]
0x5A08	XTC_1205_D2V2_8	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Vertical offset[12:8] Range is [0:6976]
0x5A09	XTC_1205_D2V2_9	0x00	RW	Bit[7:0]: Vertical offset[7:0] Range is [0:6976]
0x5A0A	XTC_1205_D2V2_A	0x24	RW	Bit[7:6]: Not used Bit[5:0]: Image calibration width[12:8] Range is [0:6976]

table 6-62 XTC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5A0B	XTC_1205_D2V2_B	0x40	RW	Bit[7:0]: Image calibration width[7:0] Range is [0:6976]
0x5A0C	XTC_1205_D2V2_C	0x1B	RW	Bit[7:5]: Not used Bit[4:0]: Image calibration height[12:8] Range is [0:9280]
0x5A0D	XTC_1205_D2V2_D	0x40	RW	Bit[7:0]: Image calibration height[7:0] Range is [0:9280]
0x5A0E	XTC_1205_D2V2_E	0x78	RW	Bit[7:0]: XTALK ratio upper limit Range is [-128:127]
0x5A0F	XTC_1205_D2V2_F	0x88	RW	Bit[7:0]: XTALK ratio lower limit Range is [-128:127]
0x5A10~ 0x5A12	NOT USED	–	–	Not Used
0x5A13	XTC_1205_D2V2_13	0x00	RW	Bit[7:2]: Not used Bit[1]: Use manual configuration for image size Range is [0:1] Bit[0]: Use manual configuration for offset Range is [0:1]
0x5A14~ 0x5A15	NOT USED	–	–	Not Used
0x5A16	XTC_1205_D2V2_16	–	R	Bit[7:0]: Version[15:8] Range is [0:255]
0x5A17	XTC_1205_D2V2_17	–	R	Bit[7:0]: Version[7:0] Range is [0:255]

6.63 XTC_1C [0x5A40 - 0x5B5F]

table 6-63 XTC_1C registers (sheet 1 of 11)

address	register name	default value	R/W	description
0x5A40	XTC_1C_CTRL_0000	–	RW	Gb0 Channel Control Parameter 0
0x5A41	XTC_1C_CTRL_0001	–	RW	Gb0 Channel Control Parameter 1
0x5A42	XTC_1C_CTRL_0002	–	RW	Gb0 Channel Control Parameter 2
0x5A43	XTC_1C_CTRL_0003	–	RW	Gb0 Channel Control Parameter 3
0x5A44	XTC_1C_CTRL_0004	–	RW	Gb0 Channel Control Parameter 4

table 6-63 XTC_1C registers (sheet 2 of 11)

address	register name	default value	R/W	description
0x5A45	XTC_1C_CTRL_0005	–	RW	Gb0 Channel Control Parameter 5
0x5A46	XTC_1C_CTRL_0006	–	RW	Gb0 Channel Control Parameter 6
0x5A47	XTC_1C_CTRL_0007	–	RW	Gb0 Channel Control Parameter 7
0x5A48	XTC_1C_CTRL_0008	–	RW	Gb0 Channel Control Parameter 8
0x5A49	XTC_1C_CTRL_0009	–	RW	Gb0 Channel Control Parameter 9
0x5A4A	XTC_1C_CTRL_0010	–	RW	Gb0 Channel Control Parameter 10
0x5A4B	XTC_1C_CTRL_0011	–	RW	Gb0 Channel Control Parameter 11
0x5A4C	XTC_1C_CTRL_0012	–	RW	Gb0 Channel Control Parameter 12
0x5A4D	XTC_1C_CTRL_0013	–	RW	Gb0 Channel Control Parameter 13
0x5A4E	XTC_1C_CTRL_0014	–	RW	Gb0 Channel Control Parameter 14
0x5A4F	XTC_1C_CTRL_0015	–	RW	Gb0 Channel Control Parameter 15
0x5A50	XTC_1C_CTRL_0016	–	RW	Gb0 Channel Control Parameter 16
0x5A51	XTC_1C_CTRL_0017	–	RW	Gb0 Channel Control Parameter 17
0x5A52	XTC_1C_CTRL_0018	–	RW	Gb0 Channel Control Parameter 18
0x5A53	XTC_1C_CTRL_0019	–	RW	Gb0 Channel Control Parameter 19
0x5A54	XTC_1C_CTRL_0020	–	RW	Gb0 Channel Control Parameter 20
0x5A55	XTC_1C_CTRL_0021	–	RW	Gb0 Channel Control Parameter 21
0x5A56	XTC_1C_CTRL_0022	–	RW	Gb0 Channel Control Parameter 22
0x5A57	XTC_1C_CTRL_0023	–	RW	Gb0 Channel Control Parameter 23
0x5A58	XTC_1C_CTRL_0024	–	RW	Gb0 Channel Control Parameter 24
0x5A59	XTC_1C_CTRL_0025	–	RW	Gb0 Channel Control Parameter 25
0x5A5A	XTC_1C_CTRL_0026	–	RW	Gb0 Channel Control Parameter 26
0x5A5B	XTC_1C_CTRL_0027	–	RW	Gb0 Channel Control Parameter 27
0x5A5C	XTC_1C_CTRL_0028	–	RW	Gb0 Channel Control Parameter 28
0x5A5D	XTC_1C_CTRL_0029	–	RW	Gb0 Channel Control Parameter 29
0x5A5E	XTC_1C_CTRL_0030	–	RW	Gb0 Channel Control Parameter 30
0x5A5F	XTC_1C_CTRL_0031	–	RW	Gb0 Channel Control Parameter 31
0x5A60	XTC_1C_CTRL_0032	–	RW	Gb0 Channel Control Parameter 32
0x5A61	XTC_1C_CTRL_0033	–	RW	Gb0 Channel Control Parameter 33
0x5A62	XTC_1C_CTRL_0034	–	RW	Gb0 Channel Control Parameter 34

table 6-63 XTC_1C registers (sheet 3 of 11)

address	register name	default value	R/W	description
0x5A63	XTC_1C_CTRL_0035	–	RW	Gb0 Channel Control Parameter 35
0x5A64	XTC_1C_CTRL_0036	–	RW	Gb1 Channel Control Parameter 0
0x5A65	XTC_1C_CTRL_0037	–	RW	Gb1 Channel Control Parameter 1
0x5A66	XTC_1C_CTRL_0038	–	RW	Gb1 Channel Control Parameter 2
0x5A67	XTC_1C_CTRL_0039	–	RW	Gb1 Channel Control Parameter 3
0x5A68	XTC_1C_CTRL_0040	–	RW	Gb1 Channel Control Parameter 4
0x5A69	XTC_1C_CTRL_0041	–	RW	Gb1 Channel Control Parameter 5
0x5A6A	XTC_1C_CTRL_0042	–	RW	Gb1 Channel Control Parameter 6
0x5A6B	XTC_1C_CTRL_0043	–	RW	Gb1 Channel Control Parameter 7
0x5A6C	XTC_1C_CTRL_0044	–	RW	Gb1 Channel Control Parameter 8
0x5A6D	XTC_1C_CTRL_0045	–	RW	Gb1 Channel Control Parameter 9
0x5A6E	XTC_1C_CTRL_0046	–	RW	Gb1 Channel Control Parameter 10
0x5A6F	XTC_1C_CTRL_0047	–	RW	Gb1 Channel Control Parameter 11
0x5A70	XTC_1C_CTRL_0048	–	RW	Gb1 Channel Control Parameter 12
0x5A71	XTC_1C_CTRL_0049	–	RW	Gb1 Channel Control Parameter 13
0x5A72	XTC_1C_CTRL_0050	–	RW	Gb1 Channel Control Parameter 14
0x5A73	XTC_1C_CTRL_0051	–	RW	Gb1 Channel Control Parameter 15
0x5A74	XTC_1C_CTRL_0052	–	RW	Gb1 Channel Control Parameter 16
0x5A75	XTC_1C_CTRL_0053	–	RW	Gb1 Channel Control Parameter 17
0x5A76	XTC_1C_CTRL_0054	–	RW	Gb1 Channel Control Parameter 18
0x5A77	XTC_1C_CTRL_0055	–	RW	Gb1 Channel Control Parameter 19
0x5A78	XTC_1C_CTRL_0056	–	RW	Gb1 Channel Control Parameter 20
0x5A79	XTC_1C_CTRL_0057	–	RW	Gb1 Channel Control Parameter 21
0x5A7A	XTC_1C_CTRL_0058	–	RW	Gb1 Channel Control Parameter 22
0x5A7B	XTC_1C_CTRL_0059	–	RW	Gb1 Channel Control Parameter 23
0x5A7C	XTC_1C_CTRL_0060	–	RW	Gb1 Channel Control Parameter 24
0x5A7D	XTC_1C_CTRL_0061	–	RW	Gb1 Channel Control Parameter 25
0x5A7E	XTC_1C_CTRL_0062	–	RW	Gb1 Channel Control Parameter 26
0x5A7F	XTC_1C_CTRL_0063	–	RW	Gb1 Channel Control Parameter 27
0x5A80	XTC_1C_CTRL_0064	–	RW	Gb1 Channel Control Parameter 28

table 6-63 XTC_1C registers (sheet 4 of 11)

address	register name	default value	R/W	description
0x5A81	XTC_1C_CTRL_0065	–	RW	Gb1 Channel Control Parameter 29
0x5A82	XTC_1C_CTRL_0066	–	RW	Gb1 Channel Control Parameter 30
0x5A83	XTC_1C_CTRL_0067	–	RW	Gb1 Channel Control Parameter 31
0x5A84	XTC_1C_CTRL_0068	–	RW	Gb1 Channel Control Parameter 32
0x5A85	XTC_1C_CTRL_0069	–	RW	Gb1 Channel Control Parameter 33
0x5A86	XTC_1C_CTRL_0070	–	RW	Gb1 Channel Control Parameter 34
0x5A87	XTC_1C_CTRL_0071	–	RW	Gb1 Channel Control Parameter 35
0x5A88	XTC_1C_CTRL_0072	–	RW	Gb2 Channel Control Parameter 0
0x5A89	XTC_1C_CTRL_0073	–	RW	Gb2 Channel Control Parameter 1
0x5A8A	XTC_1C_CTRL_0074	–	RW	Gb2 Channel Control Parameter 2
0x5A8B	XTC_1C_CTRL_0075	–	RW	Gb2 Channel Control Parameter 3
0x5A8C	XTC_1C_CTRL_0076	–	RW	Gb2 Channel Control Parameter 4
0x5A8D	XTC_1C_CTRL_0077	–	RW	Gb2 Channel Control Parameter 5
0x5A8E	XTC_1C_CTRL_0078	–	RW	Gb2 Channel Control Parameter 6
0x5A8F	XTC_1C_CTRL_0079	–	RW	Gb2 Channel Control Parameter 7
0x5A90	XTC_1C_CTRL_0080	–	RW	Gb2 Channel Control Parameter 8
0x5A91	XTC_1C_CTRL_0081	–	RW	Gb2 Channel Control Parameter 9
0x5A92	XTC_1C_CTRL_0082	–	RW	Gb2 Channel Control Parameter 10
0x5A93	XTC_1C_CTRL_0083	–	RW	Gb2 Channel Control Parameter 11
0x5A94	XTC_1C_CTRL_0084	–	RW	Gb2 Channel Control Parameter 12
0x5A95	XTC_1C_CTRL_0085	–	RW	Gb2 Channel Control Parameter 13
0x5A96	XTC_1C_CTRL_0086	–	RW	Gb2 Channel Control Parameter 14
0x5A97	XTC_1C_CTRL_0087	–	RW	Gb2 Channel Control Parameter 15
0x5A98	XTC_1C_CTRL_0088	–	RW	Gb2 Channel Control Parameter 16
0x5A99	XTC_1C_CTRL_0089	–	RW	Gb2 Channel Control Parameter 17
0x5A9A	XTC_1C_CTRL_0090	–	RW	Gb2 Channel Control Parameter 18
0x5A9B	XTC_1C_CTRL_0091	–	RW	Gb2 Channel Control Parameter 19
0x5A9C	XTC_1C_CTRL_0092	–	RW	Gb2 Channel Control Parameter 20
0x5A9D	XTC_1C_CTRL_0093	–	RW	Gb2 Channel Control Parameter 21
0x5A9E	XTC_1C_CTRL_0094	–	RW	Gb2 Channel Control Parameter 22

table 6-63 XTC_1C registers (sheet 5 of 11)

address	register name	default value	R/W	description
0x5A9F	XTC_1C_CTRL_0095	–	RW	Gb2 Channel Control Parameter 23
0x5AA0	XTC_1C_CTRL_0096	–	RW	Gb2 Channel Control Parameter 24
0x5AA1	XTC_1C_CTRL_0097	–	RW	Gb2 Channel Control Parameter 25
0x5AA2	XTC_1C_CTRL_0098	–	RW	Gb2 Channel Control Parameter 26
0x5AA3	XTC_1C_CTRL_0099	–	RW	Gb2 Channel Control Parameter 27
0x5AA4	XTC_1C_CTRL_0100	–	RW	Gb2 Channel Control Parameter 28
0x5AA5	XTC_1C_CTRL_0101	–	RW	Gb2 Channel Control Parameter 29
0x5AA6	XTC_1C_CTRL_0102	–	RW	Gb2 Channel Control Parameter 30
0x5AA7	XTC_1C_CTRL_0103	–	RW	Gb2 Channel Control Parameter 31
0x5AA8	XTC_1C_CTRL_0104	–	RW	Gb2 Channel Control Parameter 32
0x5AA9	XTC_1C_CTRL_0105	–	RW	Gb2 Channel Control Parameter 33
0x5AAA	XTC_1C_CTRL_0106	–	RW	Gb2 Channel Control Parameter 34
0x5AAB	XTC_1C_CTRL_0107	–	RW	Gb2 Channel Control Parameter 35
0x5AAC	XTC_1C_CTRL_0108	–	RW	Gb3 Channel Control Parameter 0
0x5AAD	XTC_1C_CTRL_0109	–	RW	Gb3 Channel Control Parameter 1
0x5AAE	XTC_1C_CTRL_0110	–	RW	Gb3 Channel Control Parameter 2
0x5AAF	XTC_1C_CTRL_0111	–	RW	Gb3 Channel Control Parameter 3
0x5AB0	XTC_1C_CTRL_0112	–	RW	Gb3 Channel Control Parameter 4
0x5AB1	XTC_1C_CTRL_0113	–	RW	Gb3 Channel Control Parameter 5
0x5AB2	XTC_1C_CTRL_0114	–	RW	Gb3 Channel Control Parameter 6
0x5AB3	XTC_1C_CTRL_0115	–	RW	Gb3 Channel Control Parameter 7
0x5AB4	XTC_1C_CTRL_0116	–	RW	Gb3 Channel Control Parameter 8
0x5AB5	XTC_1C_CTRL_0117	–	RW	Gb3 Channel Control Parameter 9
0x5AB6	XTC_1C_CTRL_0118	–	RW	Gb3 Channel Control Parameter 10
0x5AB7	XTC_1C_CTRL_0119	–	RW	Gb3 Channel Control Parameter 11
0x5AB8	XTC_1C_CTRL_0120	–	RW	Gb3 Channel Control Parameter 12
0x5AB9	XTC_1C_CTRL_0121	–	RW	Gb3 Channel Control Parameter 13
0x5ABA	XTC_1C_CTRL_0122	–	RW	Gb3 Channel Control Parameter 14
0x5ABB	XTC_1C_CTRL_0123	–	RW	Gb3 Channel Control Parameter 15
0x5ABC	XTC_1C_CTRL_0124	–	RW	Gb3 Channel Control Parameter 16

table 6-63 XTC_1C registers (sheet 6 of 11)

address	register name	default value	R/W	description
0x5ABD	XTC_1C_CTRL_0125	–	RW	Gb3 Channel Control Parameter 17
0x5ABE	XTC_1C_CTRL_0126	–	RW	Gb3 Channel Control Parameter 18
0x5ABF	XTC_1C_CTRL_0127	–	RW	Gb3 Channel Control Parameter 19
0x5AC0	XTC_1C_CTRL_0128	–	RW	Gb3 Channel Control Parameter 20
0x5AC1	XTC_1C_CTRL_0129	–	RW	Gb3 Channel Control Parameter 21
0x5AC2	XTC_1C_CTRL_0130	–	RW	Gb3 Channel Control Parameter 22
0x5AC3	XTC_1C_CTRL_0131	–	RW	Gb3 Channel Control Parameter 23
0x5AC4	XTC_1C_CTRL_0132	–	RW	Gb3 Channel Control Parameter 24
0x5AC5	XTC_1C_CTRL_0133	–	RW	Gb3 Channel Control Parameter 25
0x5AC6	XTC_1C_CTRL_0134	–	RW	Gb3 Channel Control Parameter 26
0x5AC7	XTC_1C_CTRL_0135	–	RW	Gb3 Channel Control Parameter 27
0x5AC8	XTC_1C_CTRL_0136	–	RW	Gb3 Channel Control Parameter 28
0x5AC9	XTC_1C_CTRL_0137	–	RW	Gb3 Channel Control Parameter 29
0x5ACA	XTC_1C_CTRL_0138	–	RW	Gb3 Channel Control Parameter 30
0x5ACB	XTC_1C_CTRL_0139	–	RW	Gb3 Channel Control Parameter 31
0x5ACC	XTC_1C_CTRL_0140	–	RW	Gb3 Channel Control Parameter 32
0x5ACD	XTC_1C_CTRL_0141	–	RW	Gb3 Channel Control Parameter 33
0x5ACE	XTC_1C_CTRL_0142	–	RW	Gb3 Channel Control Parameter 34
0x5ACF	XTC_1C_CTRL_0143	–	RW	Gb3 Channel Control Parameter 35
0x5AD0	XTC_1C_CTRL_0144	–	RW	Gr0 Channel Control Parameter 0
0x5AD1	XTC_1C_CTRL_0145	–	RW	Gr0 Channel Control Parameter 1
0x5AD2	XTC_1C_CTRL_0146	–	RW	Gr0 Channel Control Parameter 2
0x5AD3	XTC_1C_CTRL_0147	–	RW	Gr0 Channel Control Parameter 3
0x5AD4	XTC_1C_CTRL_0148	–	RW	Gr0 Channel Control Parameter 4
0x5AD5	XTC_1C_CTRL_0149	–	RW	Gr0 Channel Control Parameter 5
0x5AD6	XTC_1C_CTRL_0150	–	RW	Gr0 Channel Control Parameter 6
0x5AD7	XTC_1C_CTRL_0151	–	RW	Gr0 Channel Control Parameter 7
0x5AD8	XTC_1C_CTRL_0152	–	RW	Gr0 Channel Control Parameter 8
0x5AD9	XTC_1C_CTRL_0153	–	RW	Gr0 Channel Control Parameter 9
0x5ADA	XTC_1C_CTRL_0154	–	RW	Gr0 Channel Control Parameter 10

table 6-63 XTC_1C registers (sheet 7 of 11)

address	register name	default value	R/W	description
0x5ADB	XTC_1C_CTRL_0155	–	RW	Gr0 Channel Control Parameter 11
0x5ADC	XTC_1C_CTRL_0156	–	RW	Gr0 Channel Control Parameter 12
0x5ADD	XTC_1C_CTRL_0157	–	RW	Gr0 Channel Control Parameter 13
0x5ADE	XTC_1C_CTRL_0158	–	RW	Gr0 Channel Control Parameter 14
0x5ADF	XTC_1C_CTRL_0159	–	RW	Gr0 Channel Control Parameter 15
0x5AE0	XTC_1C_CTRL_0160	–	RW	Gr0 Channel Control Parameter 16
0x5AE1	XTC_1C_CTRL_0161	–	RW	Gr0 Channel Control Parameter 17
0x5AE2	XTC_1C_CTRL_0162	–	RW	Gr0 Channel Control Parameter 18
0x5AE3	XTC_1C_CTRL_0163	–	RW	Gr0 Channel Control Parameter 19
0x5AE4	XTC_1C_CTRL_0164	–	RW	Gr0 Channel Control Parameter 20
0x5AE5	XTC_1C_CTRL_0165	–	RW	Gr0 Channel Control Parameter 21
0x5AE6	XTC_1C_CTRL_0166	–	RW	Gr0 Channel Control Parameter 22
0x5AE7	XTC_1C_CTRL_0167	–	RW	Gr0 Channel Control Parameter 23
0x5AE8	XTC_1C_CTRL_0168	–	RW	Gr0 Channel Control Parameter 24
0x5AE9	XTC_1C_CTRL_0169	–	RW	Gr0 Channel Control Parameter 25
0x5AEA	XTC_1C_CTRL_0170	–	RW	Gr0 Channel Control Parameter 26
0x5AEB	XTC_1C_CTRL_0171	–	RW	Gr0 Channel Control Parameter 27
0x5AEC	XTC_1C_CTRL_0172	–	RW	Gr0 Channel Control Parameter 28
0x5AED	XTC_1C_CTRL_0173	–	RW	Gr0 Channel Control Parameter 29
0x5AEE	XTC_1C_CTRL_0174	–	RW	Gr0 Channel Control Parameter 30
0x5AEF	XTC_1C_CTRL_0175	–	RW	Gr0 Channel Control Parameter 31
0x5AF0	XTC_1C_CTRL_0176	–	RW	Gr0 Channel Control Parameter 32
0x5AF1	XTC_1C_CTRL_0177	–	RW	Gr0 Channel Control Parameter 33
0x5AF2	XTC_1C_CTRL_0178	–	RW	Gr0 Channel Control Parameter 34
0x5AF3	XTC_1C_CTRL_0179	–	RW	Gr0 Channel Control Parameter 35
0x5AF4	XTC_1C_CTRL_0180	–	RW	Gr1 Channel Control Parameter 0
0x5AF5	XTC_1C_CTRL_0181	–	RW	Gr1 Channel Control Parameter 1
0x5AF6	XTC_1C_CTRL_0182	–	RW	Gr1 Channel Control Parameter 2
0x5AF7	XTC_1C_CTRL_0183	–	RW	Gr1 Channel Control Parameter 3
0x5AF8	XTC_1C_CTRL_0184	–	RW	Gr1 Channel Control Parameter 4

table 6-63 XTC_1C registers (sheet 8 of 11)

address	register name	default value	R/W	description
0x5AF9	XTC_1C_CTRL_0185	–	RW	Gr1 Channel Control Parameter 5
0x5AFA	XTC_1C_CTRL_0186	–	RW	Gr1 Channel Control Parameter 6
0x5AFB	XTC_1C_CTRL_0187	–	RW	Gr1 Channel Control Parameter 7
0x5AFC	XTC_1C_CTRL_0188	–	RW	Gr1 Channel Control Parameter 8
0x5AFD	XTC_1C_CTRL_0189	–	RW	Gr1 Channel Control Parameter 9
0x5AFE	XTC_1C_CTRL_0190	–	RW	Gr1 Channel Control Parameter 10
0x5AFF	XTC_1C_CTRL_0191	–	RW	Gr1 Channel Control Parameter 11
0x5B00	XTC_1C_CTRL_0192	–	RW	Gr1 Channel Control Parameter 12
0x5B01	XTC_1C_CTRL_0193	–	RW	Gr1 Channel Control Parameter 13
0x5B02	XTC_1C_CTRL_0194	–	RW	Gr1 Channel Control Parameter 14
0x5B03	XTC_1C_CTRL_0195	–	RW	Gr1 Channel Control Parameter 15
0x5B04	XTC_1C_CTRL_0196	–	RW	Gr1 Channel Control Parameter 16
0x5B05	XTC_1C_CTRL_0197	–	RW	Gr1 Channel Control Parameter 17
0x5B06	XTC_1C_CTRL_0198	–	RW	Gr1 Channel Control Parameter 18
0x5B07	XTC_1C_CTRL_0199	–	RW	Gr1 Channel Control Parameter 19
0x5B08	XTC_1C_CTRL_0200	–	RW	Gr1 Channel Control Parameter 20
0x5B09	XTC_1C_CTRL_0201	–	RW	Gr1 Channel Control Parameter 21
0x5B0A	XTC_1C_CTRL_0202	–	RW	Gr1 Channel Control Parameter 22
0x5B0B	XTC_1C_CTRL_0203	–	RW	Gr1 Channel Control Parameter 23
0x5B0C	XTC_1C_CTRL_0204	–	RW	Gr1 Channel Control Parameter 24
0x5B0D	XTC_1C_CTRL_0205	–	RW	Gr1 Channel Control Parameter 25
0x5B0E	XTC_1C_CTRL_0206	–	RW	Gr1 Channel Control Parameter 26
0x5B0F	XTC_1C_CTRL_0207	–	RW	Gr1 Channel Control Parameter 27
0x5B10	XTC_1C_CTRL_0208	–	RW	Gr1 Channel Control Parameter 28
0x5B11	XTC_1C_CTRL_0209	–	RW	Gr1 Channel Control Parameter 29
0x5B12	XTC_1C_CTRL_0210	–	RW	Gr1 Channel Control Parameter 30
0x5B13	XTC_1C_CTRL_0211	–	RW	Gr1 Channel Control Parameter 31
0x5B14	XTC_1C_CTRL_0212	–	RW	Gr1 Channel Control Parameter 32
0x5B15	XTC_1C_CTRL_0213	–	RW	Gr1 Channel Control Parameter 33
0x5B16	XTC_1C_CTRL_0214	–	RW	Gr1 Channel Control Parameter 34

table 6-63 XTC_1C registers (sheet 9 of 11)

address	register name	default value	R/W	description
0x5B17	XTC_1C_CTRL_0215	–	RW	Gr1 Channel Control Parameter 35
0x5B18	XTC_1C_CTRL_0216	–	RW	Gr2 Channel Control Parameter 0
0x5B19	XTC_1C_CTRL_0217	–	RW	Gr2 Channel Control Parameter 1
0x5B1A	XTC_1C_CTRL_0218	–	RW	Gr2 Channel Control Parameter 2
0x5B1B	XTC_1C_CTRL_0219	–	RW	Gr2 Channel Control Parameter 3
0x5B1C	XTC_1C_CTRL_0220	–	RW	Gr2 Channel Control Parameter 4
0x5B1D	XTC_1C_CTRL_0221	–	RW	Gr2 Channel Control Parameter 5
0x5B1E	XTC_1C_CTRL_0222	–	RW	Gr2 Channel Control Parameter 6
0x5B1F	XTC_1C_CTRL_0223	–	RW	Gr2 Channel Control Parameter 7
0x5B20	XTC_1C_CTRL_0224	–	RW	Gr2 Channel Control Parameter 8
0x5B21	XTC_1C_CTRL_0225	–	RW	Gr2 Channel Control Parameter 9
0x5B22	XTC_1C_CTRL_0226	–	RW	Gr2 Channel Control Parameter 10
0x5B23	XTC_1C_CTRL_0227	–	RW	Gr2 Channel Control Parameter 11
0x5B24	XTC_1C_CTRL_0228	–	RW	Gr2 Channel Control Parameter 12
0x5B25	XTC_1C_CTRL_0229	–	RW	Gr2 Channel Control Parameter 13
0x5B26	XTC_1C_CTRL_0230	–	RW	Gr2 Channel Control Parameter 14
0x5B27	XTC_1C_CTRL_0231	–	RW	Gr2 Channel Control Parameter 15
0x5B28	XTC_1C_CTRL_0232	–	RW	Gr2 Channel Control Parameter 16
0x5B29	XTC_1C_CTRL_0233	–	RW	Gr2 Channel Control Parameter 17
0x5B2A	XTC_1C_CTRL_0234	–	RW	Gr2 Channel Control Parameter 18
0x5B2B	XTC_1C_CTRL_0235	–	RW	Gr2 Channel Control Parameter 19
0x5B2C	XTC_1C_CTRL_0236	–	RW	Gr2 Channel Control Parameter 20
0x5B2D	XTC_1C_CTRL_0237	–	RW	Gr2 Channel Control Parameter 21
0x5B2E	XTC_1C_CTRL_0238	–	RW	Gr2 Channel Control Parameter 22
0x5B2F	XTC_1C_CTRL_0239	–	RW	Gr2 Channel Control Parameter 23
0x5B30	XTC_1C_CTRL_0240	–	RW	Gr2 Channel Control Parameter 24
0x5B31	XTC_1C_CTRL_0241	–	RW	Gr2 Channel Control Parameter 25
0x5B32	XTC_1C_CTRL_0242	–	RW	Gr2 Channel Control Parameter 26
0x5B33	XTC_1C_CTRL_0243	–	RW	Gr2 Channel Control Parameter 27
0x5B34	XTC_1C_CTRL_0244	–	RW	Gr2 Channel Control Parameter 28

table 6-63 XTC_1C registers (sheet 10 of 11)

address	register name	default value	R/W	description
0x5B35	XTC_1C_CTRL_0245	–	RW	Gr2 Channel Control Parameter 29
0x5B36	XTC_1C_CTRL_0246	–	RW	Gr2 Channel Control Parameter 30
0x5B37	XTC_1C_CTRL_0247	–	RW	Gr2 Channel Control Parameter 31
0x5B38	XTC_1C_CTRL_0248	–	RW	Gr2 Channel Control Parameter 32
0x5B39	XTC_1C_CTRL_0249	–	RW	Gr2 Channel Control Parameter 33
0x5B3A	XTC_1C_CTRL_0250	–	RW	Gr2 Channel Control Parameter 34
0x5B3B	XTC_1C_CTRL_0251	–	RW	Gr2 Channel Control Parameter 35
0x5B3C	XTC_1C_CTRL_0252	–	RW	Gr3 Channel Control Parameter 0
0x5B3D	XTC_1C_CTRL_0253	–	RW	Gr3 Channel Control Parameter 1
0x5B3E	XTC_1C_CTRL_0254	–	RW	Gr3 Channel Control Parameter 2
0x5B3F	XTC_1C_CTRL_0255	–	RW	Gr3 Channel Control Parameter 3
0x5B40	XTC_1C_CTRL_0256	–	RW	Gr3 Channel Control Parameter 4
0x5B41	XTC_1C_CTRL_0257	–	RW	Gr3 Channel Control Parameter 5
0x5B42	XTC_1C_CTRL_0258	–	RW	Gr3 Channel Control Parameter 6
0x5B43	XTC_1C_CTRL_0259	–	RW	Gr3 Channel Control Parameter 7
0x5B44	XTC_1C_CTRL_0260	–	RW	Gr3 Channel Control Parameter 8
0x5B45	XTC_1C_CTRL_0261	–	RW	Gr3 Channel Control Parameter 9
0x5B46	XTC_1C_CTRL_0262	–	RW	Gr3 Channel Control Parameter 10
0x5B47	XTC_1C_CTRL_0263	–	RW	Gr3 Channel Control Parameter 11
0x5B48	XTC_1C_CTRL_0264	–	RW	Gr3 Channel Control Parameter 12
0x5B49	XTC_1C_CTRL_0265	–	RW	Gr3 Channel Control Parameter 13
0x5B4A	XTC_1C_CTRL_0266	–	RW	Gr3 Channel Control Parameter 14
0x5B4B	XTC_1C_CTRL_0267	–	RW	Gr3 Channel Control Parameter 15
0x5B4C	XTC_1C_CTRL_0268	–	RW	Gr3 Channel Control Parameter 16
0x5B4D	XTC_1C_CTRL_0269	–	RW	Gr3 Channel Control Parameter 17
0x5B4E	XTC_1C_CTRL_0270	–	RW	Gr3 Channel Control Parameter 18
0x5B4F	XTC_1C_CTRL_0271	–	RW	Gr3 Channel Control Parameter 19
0x5B50	XTC_1C_CTRL_0272	–	RW	Gr3 Channel Control Parameter 20
0x5B51	XTC_1C_CTRL_0273	–	RW	Gr3 Channel Control Parameter 21
0x5B52	XTC_1C_CTRL_0274	–	RW	Gr3 Channel Control Parameter 22

table 6-63 XTC_1C registers (sheet 11 of 11)

address	register name	default value	R/W	description
0x5B53	XTC_1C_CTRL_0275	–	RW	Gr3 Channel Control Parameter 23
0x5B54	XTC_1C_CTRL_0276	–	RW	Gr3 Channel Control Parameter 24
0x5B55	XTC_1C_CTRL_0277	–	RW	Gr3 Channel Control Parameter 25
0x5B56	XTC_1C_CTRL_0278	–	RW	Gr3 Channel Control Parameter 26
0x5B57	XTC_1C_CTRL_0279	–	RW	Gr3 Channel Control Parameter 27
0x5B58	XTC_1C_CTRL_0280	–	RW	Gr3 Channel Control Parameter 28
0x5B59	XTC_1C_CTRL_0281	–	RW	Gr3 Channel Control Parameter 29
0x5B5A	XTC_1C_CTRL_0282	–	RW	Gr3 Channel Control Parameter 30
0x5B5B	XTC_1C_CTRL_0283	–	RW	Gr3 Channel Control Parameter 31
0x5B5C	XTC_1C_CTRL_0284	–	RW	Gr3 Channel Control Parameter 32
0x5B5D	XTC_1C_CTRL_0285	–	RW	Gr3 Channel Control Parameter 33
0x5B5E	XTC_1C_CTRL_0286	–	RW	Gr3 Channel Control Parameter 34
0x5B5F	XTC_1C_CTRL_0287	–	RW	Gr3 Channel Control Parameter 35

6.64 XTC_3C [0x5B80 - 0x5EDF]

table 6-64 XTC_3C registers (sheet 1 of 30)

address	register name	default value	R/W	description
0x5B80	XTC_3C_CTRL_0000	–	RW	Gb0 Channel B Control Parameter 0
0x5B81	XTC_3C_CTRL_0001	–	RW	Gb0 Channel B Control Parameter 1
0x5B82	XTC_3C_CTRL_0002	–	RW	Gb0 Channel B Control Parameter 2
0x5B83	XTC_3C_CTRL_0003	–	RW	Gb0 Channel B Control Parameter 3
0x5B84	XTC_3C_CTRL_0004	–	RW	Gb0 Channel B Control Parameter 4
0x5B85	XTC_3C_CTRL_0005	–	RW	Gb0 Channel B Control Parameter 5
0x5B86	XTC_3C_CTRL_0006	–	RW	Gb0 Channel B Control Parameter 6
0x5B87	XTC_3C_CTRL_0007	–	RW	Gb0 Channel B Control Parameter 7
0x5B88	XTC_3C_CTRL_0008	–	RW	Gb0 Channel B Control Parameter 8
0x5B89	XTC_3C_CTRL_0009	–	RW	Gb0 Channel B Control Parameter 9

table 6-64 XTC_3C registers (sheet 2 of 30)

address	register name	default value	R/W	description
0x5B8A	XTC_3C_CTRL_0010	–	RW	Gb0 Channel B Control Parameter 10
0x5B8B	XTC_3C_CTRL_0011	–	RW	Gb0 Channel B Control Parameter 11
0x5B8C	XTC_3C_CTRL_0012	–	RW	Gb0 Channel B Control Parameter 12
0x5B8D	XTC_3C_CTRL_0013	–	RW	Gb0 Channel B Control Parameter 13
0x5B8E	XTC_3C_CTRL_0014	–	RW	Gb0 Channel B Control Parameter 14
0x5B8F	XTC_3C_CTRL_0015	–	RW	Gb0 Channel B Control Parameter 15
0x5B90	XTC_3C_CTRL_0016	–	RW	Gb0 Channel B Control Parameter 16
0x5B91	XTC_3C_CTRL_0017	–	RW	Gb0 Channel B Control Parameter 17
0x5B92	XTC_3C_CTRL_0018	–	RW	Gb0 Channel B Control Parameter 18
0x5B93	XTC_3C_CTRL_0019	–	RW	Gb0 Channel B Control Parameter 19
0x5B94	XTC_3C_CTRL_0020	–	RW	Gb0 Channel B Control Parameter 20
0x5B95	XTC_3C_CTRL_0021	–	RW	Gb0 Channel B Control Parameter 21
0x5B96	XTC_3C_CTRL_0022	–	RW	Gb0 Channel B Control Parameter 22
0x5B97	XTC_3C_CTRL_0023	–	RW	Gb0 Channel B Control Parameter 23
0x5B98	XTC_3C_CTRL_0024	–	RW	Gb0 Channel B Control Parameter 24
0x5B99	XTC_3C_CTRL_0025	–	RW	Gb0 Channel B Control Parameter 25
0x5B9A	XTC_3C_CTRL_0026	–	RW	Gb0 Channel B Control Parameter 26
0x5B9B	XTC_3C_CTRL_0027	–	RW	Gb0 Channel B Control Parameter 27
0x5B9C	XTC_3C_CTRL_0028	–	RW	Gb0 Channel B Control Parameter 28
0x5B9D	XTC_3C_CTRL_0029	–	RW	Gb0 Channel B Control Parameter 29
0x5B9E	XTC_3C_CTRL_0030	–	RW	Gb0 Channel B Control Parameter 30
0x5B9F	XTC_3C_CTRL_0031	–	RW	Gb0 Channel B Control Parameter 31
0x5BA0	XTC_3C_CTRL_0032	–	RW	Gb0 Channel B Control Parameter 32
0x5BA1	XTC_3C_CTRL_0033	–	RW	Gb0 Channel B Control Parameter 33
0x5BA2	XTC_3C_CTRL_0034	–	RW	Gb0 Channel B Control Parameter 34
0x5BA3	XTC_3C_CTRL_0035	–	RW	Gb0 Channel B Control Parameter 35
0x5BA4	XTC_3C_CTRL_0036	–	RW	Gb0 Channel G Control Parameter 0
0x5BA5	XTC_3C_CTRL_0037	–	RW	Gb0 Channel G Control Parameter 1
0x5BA6	XTC_3C_CTRL_0038	–	RW	Gb0 Channel G Control Parameter 2
0x5BA7	XTC_3C_CTRL_0039	–	RW	Gb0 Channel G Control Parameter 3

table 6-64 XTC_3C registers (sheet 3 of 30)

address	register name	default value	R/W	description
0x5BA8	XTC_3C_CTRL_0040	–	RW	Gb0 Channel G Control Parameter 4
0x5BA9	XTC_3C_CTRL_0041	–	RW	Gb0 Channel G Control Parameter 5
0x5BAA	XTC_3C_CTRL_0042	–	RW	Gb0 Channel G Control Parameter 6
0x5BAB	XTC_3C_CTRL_0043	–	RW	Gb0 Channel G Control Parameter 7
0x5BAC	XTC_3C_CTRL_0044	–	RW	Gb0 Channel G Control Parameter 8
0x5BAD	XTC_3C_CTRL_0045	–	RW	Gb0 Channel G Control Parameter 9
0x5BAE	XTC_3C_CTRL_0046	–	RW	Gb0 Channel G Control Parameter 10
0x5BAF	XTC_3C_CTRL_0047	–	RW	Gb0 Channel G Control Parameter 11
0x5BB0	XTC_3C_CTRL_0048	–	RW	Gb0 Channel G Control Parameter 12
0x5BB1	XTC_3C_CTRL_0049	–	RW	Gb0 Channel G Control Parameter 13
0x5BB2	XTC_3C_CTRL_0050	–	RW	Gb0 Channel G Control Parameter 14
0x5BB3	XTC_3C_CTRL_0051	–	RW	Gb0 Channel G Control Parameter 15
0x5BB4	XTC_3C_CTRL_0052	–	RW	Gb0 Channel G Control Parameter 16
0x5BB5	XTC_3C_CTRL_0053	–	RW	Gb0 Channel G Control Parameter 17
0x5BB6	XTC_3C_CTRL_0054	–	RW	Gb0 Channel G Control Parameter 18
0x5BB7	XTC_3C_CTRL_0055	–	RW	Gb0 Channel G Control Parameter 19
0x5BB8	XTC_3C_CTRL_0056	–	RW	Gb0 Channel G Control Parameter 20
0x5BB9	XTC_3C_CTRL_0057	–	RW	Gb0 Channel G Control Parameter 21
0x5BBA	XTC_3C_CTRL_0058	–	RW	Gb0 Channel G Control Parameter 22
0x5BBB	XTC_3C_CTRL_0059	–	RW	Gb0 Channel G Control Parameter 23
0x5BBC	XTC_3C_CTRL_0060	–	RW	Gb0 Channel G Control Parameter 24
0x5BBD	XTC_3C_CTRL_0061	–	RW	Gb0 Channel G Control Parameter 25
0x5BBE	XTC_3C_CTRL_0062	–	RW	Gb0 Channel G Control Parameter 26
0x5BBF	XTC_3C_CTRL_0063	–	RW	Gb0 Channel G Control Parameter 27
0x5BC0	XTC_3C_CTRL_0064	–	RW	Gb0 Channel G Control Parameter 28
0x5BC1	XTC_3C_CTRL_0065	–	RW	Gb0 Channel G Control Parameter 29
0x5BC2	XTC_3C_CTRL_0066	–	RW	Gb0 Channel G Control Parameter 30
0x5BC3	XTC_3C_CTRL_0067	–	RW	Gb0 Channel G Control Parameter 31
0x5BC4	XTC_3C_CTRL_0068	–	RW	Gb0 Channel G Control Parameter 32
0x5BC5	XTC_3C_CTRL_0069	–	RW	Gb0 Channel G Control Parameter 33

table 6-64 XTC_3C registers (sheet 4 of 30)

address	register name	default value	R/W	description
0x5BC6	XTC_3C_CTRL_0070	–	RW	Gb0 Channel G Control Parameter 34
0x5BC7	XTC_3C_CTRL_0071	–	RW	Gb0 Channel G Control Parameter 35
0x5BC8	XTC_3C_CTRL_0072	–	RW	Gb0 Channel R Control Parameter 0
0x5BC9	XTC_3C_CTRL_0073	–	RW	Gb0 Channel R Control Parameter 1
0x5BCA	XTC_3C_CTRL_0074	–	RW	Gb0 Channel R Control Parameter 2
0x5BCB	XTC_3C_CTRL_0075	–	RW	Gb0 Channel R Control Parameter 3
0x5BCC	XTC_3C_CTRL_0076	–	RW	Gb0 Channel R Control Parameter 4
0x5BCD	XTC_3C_CTRL_0077	–	RW	Gb0 Channel R Control Parameter 5
0x5BCE	XTC_3C_CTRL_0078	–	RW	Gb0 Channel R Control Parameter 6
0x5BCF	XTC_3C_CTRL_0079	–	RW	Gb0 Channel R Control Parameter 7
0x5BD0	XTC_3C_CTRL_0080	–	RW	Gb0 Channel R Control Parameter 8
0x5BD1	XTC_3C_CTRL_0081	–	RW	Gb0 Channel R Control Parameter 9
0x5BD2	XTC_3C_CTRL_0082	–	RW	Gb0 Channel R Control Parameter 10
0x5BD3	XTC_3C_CTRL_0083	–	RW	Gb0 Channel R Control Parameter 11
0x5BD4	XTC_3C_CTRL_0084	–	RW	Gb0 Channel R Control Parameter 12
0x5BD5	XTC_3C_CTRL_0085	–	RW	Gb0 Channel R Control Parameter 13
0x5BD6	XTC_3C_CTRL_0086	–	RW	Gb0 Channel R Control Parameter 14
0x5BD7	XTC_3C_CTRL_0087	–	RW	Gb0 Channel R Control Parameter 15
0x5BD8	XTC_3C_CTRL_008	–	RW	Gb0 Channel R Control Parameter 16
0x5BD9	XTC_3C_CTRL_0089	–	RW	Gb0 Channel R Control Parameter 17
0x5BDA	XTC_3C_CTRL_0090	–	RW	Gb0 Channel R Control Parameter 18
0x5BDB	XTC_3C_CTRL_0091	–	RW	Gb0 Channel R Control Parameter 19
0x5BDC	XTC_3C_CTRL_0092	–	RW	Gb0 Channel R Control Parameter 20
0x5BDD	XTC_3C_CTRL_0093	–	RW	Gb0 Channel R Control Parameter 21
0x5BDE	XTC_3C_CTRL_0094	–	RW	Gb0 Channel R Control Parameter 22
0x5BDF	XTC_3C_CTRL_0095	–	RW	Gb0 Channel R Control Parameter 23
0x5BE0	XTC_3C_CTRL_0096	–	RW	Gb0 Channel R Control Parameter 24
0x5BE1	XTC_3C_CTRL_0097	–	RW	Gb0 Channel R Control Parameter 25
0x5BE2	XTC_3C_CTRL_0098	–	RW	Gb0 Channel R Control Parameter 26
0x5BE3	XTC_3C_CTRL_0099	–	RW	Gb0 Channel R Control Parameter 27

table 6-64 XTC_3C registers (sheet 5 of 30)

address	register name	default value	R/W	description
0x5BE4	XTC_3C_CTRL_0100	–	RW	Gb0 Channel R Control Parameter 28
0x5BE5	XTC_3C_CTRL_0101	–	RW	Gb0 Channel R Control Parameter 29
0x5BE6	XTC_3C_CTRL_0102	–	RW	Gb0 Channel R Control Parameter 30
0x5BE7	XTC_3C_CTRL_0103	–	RW	Gb0 Channel R Control Parameter 31
0x5BE8	XTC_3C_CTRL_0104	–	RW	Gb0 Channel R Control Parameter 32
0x5BE9	XTC_3C_CTRL_0105	–	RW	Gb0 Channel R Control Parameter 33
0x5BEA	XTC_3C_CTRL_0106	–	RW	Gb0 Channel R Control Parameter 34
0x5BEB	XTC_3C_CTRL_0107	–	RW	Gb0 Channel R Control Parameter 35
0x5BEC	XTC_3C_CTRL_0108	–	RW	Gb1 Channel B Control Parameter 0
0x5BED	XTC_3C_CTRL_0109	–	RW	Gb1 Channel B Control Parameter 1
0x5BEE	XTC_3C_CTRL_0110	–	RW	Gb1 Channel B Control Parameter 2
0x5BEF	XTC_3C_CTRL_0111	–	RW	Gb1 Channel B Control Parameter 3
0x5BF0	XTC_3C_CTRL_0112	–	RW	Gb1 Channel B Control Parameter 4
0x5BF1	XTC_3C_CTRL_0113	–	RW	Gb1 Channel B Control Parameter 5
0x5BF2	XTC_3C_CTRL_0114	–	RW	Gb1 Channel B Control Parameter 6
0x5BF3	XTC_3C_CTRL_0115	–	RW	Gb1 Channel B Control Parameter 7
0x5BF4	XTC_3C_CTRL_0116	–	RW	Gb1 Channel B Control Parameter 8
0x5BF5	XTC_3C_CTRL_0117	–	RW	Gb1 Channel B Control Parameter 9
0x5BF6	XTC_3C_CTRL_0118	–	RW	Gb1 Channel B Control Parameter 10
0x5BF7	XTC_3C_CTRL_0119	–	RW	Gb1 Channel B Control Parameter 11
0x5BF8	XTC_3C_CTRL_0120	–	RW	Gb1 Channel B Control Parameter 12
0x5BF9	XTC_3C_CTRL_0121	–	RW	Gb1 Channel B Control Parameter 13
0x5BFA	XTC_3C_CTRL_0122	–	RW	Gb1 Channel B Control Parameter 14
0x5BFB	XTC_3C_CTRL_0123	–	RW	Gb1 Channel B Control Parameter 15
0x5BFC	XTC_3C_CTRL_0124	–	RW	Gb1 Channel B Control Parameter 16
0x5BFD	XTC_3C_CTRL_0125	–	RW	Gb1 Channel B Control Parameter 17
0x5BFE	XTC_3C_CTRL_0126	–	RW	Gb1 Channel B Control Parameter 18
0x5BFF	XTC_3C_CTRL_0127	–	RW	Gb1 Channel B Control Parameter 19
0x5C00	XTC_3C_CTRL_0128	–	RW	Gb1 Channel B Control Parameter 20
0x5C01	XTC_3C_CTRL_0129	–	RW	Gb1 Channel B Control Parameter 21

table 6-64 XTC_3C registers (sheet 6 of 30)

address	register name	default value	R/W	description
0x5C02	XTC_3C_CTRL_0130	–	RW	Gb1 Channel B Control Parameter 22
0x5C03	XTC_3C_CTRL_0131	–	RW	Gb1 Channel B Control Parameter 23
0x5C04	XTC_3C_CTRL_0132	–	RW	Gb1 Channel B Control Parameter 24
0x5C05	XTC_3C_CTRL_0133	–	RW	Gb1 Channel B Control Parameter 25
0x5C06	XTC_3C_CTRL_0134	–	RW	Gb1 Channel B Control Parameter 26
0x5C07	XTC_3C_CTRL_0135	–	RW	Gb1 Channel B Control Parameter 27
0x5C08	XTC_3C_CTRL_0136	–	RW	Gb1 Channel B Control Parameter 28
0x5C09	XTC_3C_CTRL_0137	–	RW	Gb1 Channel B Control Parameter 29
0x5C0A	XTC_3C_CTRL_0138	–	RW	Gb1 Channel B Control Parameter 30
0x5C0B	XTC_3C_CTRL_0139	–	RW	Gb1 Channel B Control Parameter 31
0x5C0C	XTC_3C_CTRL_0140	–	RW	Gb1 Channel B Control Parameter 32
0x5C0D	XTC_3C_CTRL_0141	–	RW	Gb1 Channel B Control Parameter 33
0x5C0E	XTC_3C_CTRL_0142	–	RW	Gb1 Channel B Control Parameter 34
0x5C0F	XTC_3C_CTRL_0143	–	RW	Gb1 Channel B Control Parameter 35
0x5C10	XTC_3C_CTRL_0144	–	RW	Gb1 Channel G Control Parameter 0
0x5C11	XTC_3C_CTRL_0145	–	RW	Gb1 Channel G Control Parameter 1
0x5C12	XTC_3C_CTRL_0146	–	RW	Gb1 Channel G Control Parameter 2
0x5C13	XTC_3C_CTRL_0147	–	RW	Gb1 Channel G Control Parameter 3
0x5C14	XTC_3C_CTRL_0148	–	RW	Gb1 Channel G Control Parameter 4
0x5C15	XTC_3C_CTRL_0149	–	RW	Gb1 Channel G Control Parameter 5
0x5C16	XTC_3C_CTRL_0150	–	RW	Gb1 Channel G Control Parameter 6
0x5C17	XTC_3C_CTRL_0151	–	RW	Gb1 Channel G Control Parameter 7
0x5C18	XTC_3C_CTRL_0152	–	RW	Gb1 Channel G Control Parameter 8
0x5C19	XTC_3C_CTRL_0153	–	RW	Gb1 Channel G Control Parameter 9
0x5C1A	XTC_3C_CTRL_0154	–	RW	Gb1 Channel G Control Parameter 10
0x5C1B	XTC_3C_CTRL_0155	–	RW	Gb1 Channel G Control Parameter 11
0x5C1C	XTC_3C_CTRL_0156	–	RW	Gb1 Channel G Control Parameter 12
0x5C1D	XTC_3C_CTRL_0157	–	RW	Gb1 Channel G Control Parameter 13
0x5C1E	XTC_3C_CTRL_0158	–	RW	Gb1 Channel G Control Parameter 14
0x5C1F	XTC_3C_CTRL_0159	–	RW	Gb1 Channel G Control Parameter 15

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address	register name	default value	R/W	description
0x5C20	XTC_3C_CTRL_0160	–	RW	Gb1 Channel G Control Parameter 16
0x5C21	XTC_3C_CTRL_0161	–	RW	Gb1 Channel G Control Parameter 17
0x5C22	XTC_3C_CTRL_0162	–	RW	Gb1 Channel G Control Parameter 18
0x5C23	XTC_3C_CTRL_0163	–	RW	Gb1 Channel G Control Parameter 19
0x5C24	XTC_3C_CTRL_0164	–	RW	Gb1 Channel G Control Parameter 20
0x5C25	XTC_3C_CTRL_0165	–	RW	Gb1 Channel G Control Parameter 21
0x5C26	XTC_3C_CTRL_0166	–	RW	Gb1 Channel G Control Parameter 22
0x5C27	XTC_3C_CTRL_0167	–	RW	Gb1 Channel G Control Parameter 23
0x5C28	XTC_3C_CTRL_0168	–	RW	Gb1 Channel G Control Parameter 24
0x5C29	XTC_3C_CTRL_0169	–	RW	Gb1 Channel G Control Parameter 25
0x5C2A	XTC_3C_CTRL_0170	–	RW	Gb1 Channel G Control Parameter 26
0x5C2B	XTC_3C_CTRL_0171	–	RW	Gb1 Channel G Control Parameter 27
0x5C2C	XTC_3C_CTRL_0172	–	RW	Gb1 Channel G Control Parameter 28
0x5C2D	XTC_3C_CTRL_0173	–	RW	Gb1 Channel G Control Parameter 29
0x5C2E	XTC_3C_CTRL_0174	–	RW	Gb1 Channel G Control Parameter 30
0x5C2F	XTC_3C_CTRL_0175	–	RW	Gb1 Channel G Control Parameter 31
0x5C30	XTC_3C_CTRL_0176	–	RW	Gb1 Channel G Control Parameter 32
0x5C31	XTC_3C_CTRL_0177	–	RW	Gb1 Channel G Control Parameter 33
0x5C32	XTC_3C_CTRL_0178	–	RW	Gb1 Channel G Control Parameter 34
0x5C33	XTC_3C_CTRL_0179	–	RW	Gb1 Channel G Control Parameter 35
0x5C34	XTC_3C_CTRL_0180	–	RW	Gb1 Channel R Control Parameter 0
0x5C35	XTC_3C_CTRL_0181	–	RW	Gb1 Channel R Control Parameter 1
0x5C36	XTC_3C_CTRL_0182	–	RW	Gb1 Channel R Control Parameter 2
0x5C37	XTC_3C_CTRL_0183	–	RW	Gb1 Channel R Control Parameter 3
0x5C38	XTC_3C_CTRL_0184	–	RW	Gb1 Channel R Control Parameter 4
0x5C39	XTC_3C_CTRL_0185	–	RW	Gb1 Channel R Control Parameter 5
0x5C3A	XTC_3C_CTRL_0186	–	RW	Gb1 Channel R Control Parameter 6
0x5C3B	XTC_3C_CTRL_0187	–	RW	Gb1 Channel R Control Parameter 7
0x5C3C	XTC_3C_CTRL_018	–	RW	Gb1 Channel R Control Parameter 8
0x5C3D	XTC_3C_CTRL_0189	–	RW	Gb1 Channel R Control Parameter 9

table 6-64 XTC_3C registers (sheet 8 of 30)

address	register name	default value	R/W	description
0x5C3E	XTC_3C_CTRL_0190	–	RW	Gb1 Channel R Control Parameter 10
0x5C3F	XTC_3C_CTRL_0191	–	RW	Gb1 Channel R Control Parameter 11
0x5C40	XTC_3C_CTRL_0192	–	RW	Gb1 Channel R Control Parameter 12
0x5C41	XTC_3C_CTRL_0193	–	RW	Gb1 Channel R Control Parameter 13
0x5C42	XTC_3C_CTRL_0194	–	RW	Gb1 Channel R Control Parameter 14
0x5C43	XTC_3C_CTRL_0195	–	RW	Gb1 Channel R Control Parameter 15
0x5C44	XTC_3C_CTRL_0196	–	RW	Gb1 Channel R Control Parameter 16
0x5C45	XTC_3C_CTRL_0197	–	RW	Gb1 Channel R Control Parameter 17
0x5C46	XTC_3C_CTRL_0198	–	RW	Gb1 Channel R Control Parameter 18
0x5C47	XTC_3C_CTRL_0199	–	RW	Gb1 Channel R Control Parameter 19
0x5C48	XTC_3C_CTRL_0200	–	RW	Gb1 Channel R Control Parameter 20
0x5C49	XTC_3C_CTRL_0201	–	RW	Gb1 Channel R Control Parameter 21
0x5C4A	XTC_3C_CTRL_0202	–	RW	Gb1 Channel R Control Parameter 22
0x5C4B	XTC_3C_CTRL_0203	–	RW	Gb1 Channel R Control Parameter 23
0x5C4C	XTC_3C_CTRL_0204	–	RW	Gb1 Channel R Control Parameter 24
0x5C4D	XTC_3C_CTRL_0205	–	RW	Gb1 Channel R Control Parameter 25
0x5C4E	XTC_3C_CTRL_0206	–	RW	Gb1 Channel R Control Parameter 26
0x5C4F	XTC_3C_CTRL_0207	–	RW	Gb1 Channel R Control Parameter 27
0x5C50	XTC_3C_CTRL_0208	–	RW	Gb1 Channel R Control Parameter 28
0x5C51	XTC_3C_CTRL_0209	–	RW	Gb1 Channel R Control Parameter 29
0x5C52	XTC_3C_CTRL_0210	–	RW	Gb1 Channel R Control Parameter 30
0x5C53	XTC_3C_CTRL_0211	–	RW	Gb1 Channel R Control Parameter 31
0x5C54	XTC_3C_CTRL_0212	–	RW	Gb1 Channel R Control Parameter 32
0x5C55	XTC_3C_CTRL_0213	–	RW	Gb1 Channel R Control Parameter 33
0x5C56	XTC_3C_CTRL_0214	–	RW	Gb1 Channel R Control Parameter 34
0x5C57	XTC_3C_CTRL_0215	–	RW	Gb1 Channel R Control Parameter 35
0x5C58	XTC_3C_CTRL_0216	–	RW	Gb2 Channel B Control Parameter 0
0x5C59	XTC_3C_CTRL_0217	–	RW	Gb2 Channel B Control Parameter 1
0x5C5A	XTC_3C_CTRL_0218	–	RW	Gb2 Channel B Control Parameter 2
0x5C5B	XTC_3C_CTRL_0219	–	RW	Gb2 Channel B Control Parameter 3

table 6-64 XTC_3C registers (sheet 9 of 30)

address	register name	default value	R/W	description
0x5C5C	XTC_3C_CTRL_0220	–	RW	Gb2 Channel B Control Parameter 4
0x5C5D	XTC_3C_CTRL_0221	–	RW	Gb2 Channel B Control Parameter 5
0x5C5E	XTC_3C_CTRL_0222	–	RW	Gb2 Channel B Control Parameter 6
0x5C5F	XTC_3C_CTRL_0223	–	RW	Gb2 Channel B Control Parameter 7
0x5C60	XTC_3C_CTRL_0224	–	RW	Gb2 Channel B Control Parameter 8
0x5C61	XTC_3C_CTRL_0225	–	RW	Gb2 Channel B Control Parameter 9
0x5C62	XTC_3C_CTRL_0226	–	RW	Gb2 Channel B Control Parameter 10
0x5C63	XTC_3C_CTRL_0227	–	RW	Gb2 Channel B Control Parameter 11
0x5C64	XTC_3C_CTRL_0228	–	RW	Gb2 Channel B Control Parameter 12
0x5C65	XTC_3C_CTRL_0229	–	RW	Gb2 Channel B Control Parameter 13
0x5C66	XTC_3C_CTRL_0230	–	RW	Gb2 Channel B Control Parameter 14
0x5C67	XTC_3C_CTRL_0231	–	RW	Gb2 Channel B Control Parameter 15
0x5C68	XTC_3C_CTRL_0232	–	RW	Gb2 Channel B Control Parameter 16
0x5C69	XTC_3C_CTRL_0233	–	RW	Gb2 Channel B Control Parameter 17
0x5C6A	XTC_3C_CTRL_0234	–	RW	Gb2 Channel B Control Parameter 18
0x5C6B	XTC_3C_CTRL_0235	–	RW	Gb2 Channel B Control Parameter 19
0x5C6C	XTC_3C_CTRL_0236	–	RW	Gb2 Channel B Control Parameter 20
0x5C6D	XTC_3C_CTRL_0237	–	RW	Gb2 Channel B Control Parameter 21
0x5C6E	XTC_3C_CTRL_0238	–	RW	Gb2 Channel B Control Parameter 22
0x5C6F	XTC_3C_CTRL_0239	–	RW	Gb2 Channel B Control Parameter 23
0x5C70	XTC_3C_CTRL_0240	–	RW	Gb2 Channel B Control Parameter 24
0x5C71	XTC_3C_CTRL_0241	–	RW	Gb2 Channel B Control Parameter 25
0x5C72	XTC_3C_CTRL_0242	–	RW	Gb2 Channel B Control Parameter 26
0x5C73	XTC_3C_CTRL_0243	–	RW	Gb2 Channel B Control Parameter 27
0x5C74	XTC_3C_CTRL_0244	–	RW	Gb2 Channel B Control Parameter 28
0x5C75	XTC_3C_CTRL_0245	–	RW	Gb2 Channel B Control Parameter 29
0x5C76	XTC_3C_CTRL_0246	–	RW	Gb2 Channel B Control Parameter 30
0x5C77	XTC_3C_CTRL_0247	–	RW	Gb2 Channel B Control Parameter 31
0x5C78	XTC_3C_CTRL_0248	–	RW	Gb2 Channel B Control Parameter 32
0x5C79	XTC_3C_CTRL_0249	–	RW	Gb2 Channel B Control Parameter 33

table 6-64 XTC_3C registers (sheet 10 of 30)

address	register name	default value	R/W	description
0x5C7A	XTC_3C_CTRL_0250	–	RW	Gb2 Channel B Control Parameter 34
0x5C7B	XTC_3C_CTRL_0251	–	RW	Gb2 Channel B Control Parameter 35
0x5C7C	XTC_3C_CTRL_0252	–	RW	Gb2 Channel G Control Parameter 0
0x5C7D	XTC_3C_CTRL_0253	–	RW	Gb2 Channel G Control Parameter 1
0x5C7E	XTC_3C_CTRL_0254	–	RW	Gb2 Channel G Control Parameter 2
0x5C7F	XTC_3C_CTRL_0255	–	RW	Gb2 Channel G Control Parameter 3
0x5C80	XTC_3C_CTRL_0256	–	RW	Gb2 Channel G Control Parameter 4
0x5C81	XTC_3C_CTRL_0257	–	RW	Gb2 Channel G Control Parameter 5
0x5C82	XTC_3C_CTRL_0258	–	RW	Gb2 Channel G Control Parameter 6
0x5C83	XTC_3C_CTRL_0259	–	RW	Gb2 Channel G Control Parameter 7
0x5C84	XTC_3C_CTRL_0260	–	RW	Gb2 Channel G Control Parameter 8
0x5C85	XTC_3C_CTRL_0261	–	RW	Gb2 Channel G Control Parameter 9
0x5C86	XTC_3C_CTRL_0262	–	RW	Gb2 Channel G Control Parameter 10
0x5C87	XTC_3C_CTRL_0263	–	RW	Gb2 Channel G Control Parameter 11
0x5C88	XTC_3C_CTRL_0264	–	RW	Gb2 Channel G Control Parameter 12
0x5C89	XTC_3C_CTRL_0265	–	RW	Gb2 Channel G Control Parameter 13
0x5C8A	XTC_3C_CTRL_0266	–	RW	Gb2 Channel G Control Parameter 14
0x5C8B	XTC_3C_CTRL_0267	–	RW	Gb2 Channel G Control Parameter 15
0x5C8C	XTC_3C_CTRL_0268	–	RW	Gb2 Channel G Control Parameter 16
0x5C8D	XTC_3C_CTRL_0269	–	RW	Gb2 Channel G Control Parameter 17
0x5C8E	XTC_3C_CTRL_0270	–	RW	Gb2 Channel G Control Parameter 18
0x5C8F	XTC_3C_CTRL_0271	–	RW	Gb2 Channel G Control Parameter 19
0x5C90	XTC_3C_CTRL_0272	–	RW	Gb2 Channel G Control Parameter 20
0x5C91	XTC_3C_CTRL_0273	–	RW	Gb2 Channel G Control Parameter 21
0x5C92	XTC_3C_CTRL_0274	–	RW	Gb2 Channel G Control Parameter 22
0x5C93	XTC_3C_CTRL_0275	–	RW	Gb2 Channel G Control Parameter 23
0x5C94	XTC_3C_CTRL_0276	–	RW	Gb2 Channel G Control Parameter 24
0x5C95	XTC_3C_CTRL_0277	–	RW	Gb2 Channel G Control Parameter 25
0x5C96	XTC_3C_CTRL_0278	–	RW	Gb2 Channel G Control Parameter 26
0x5C97	XTC_3C_CTRL_0279	–	RW	Gb2 Channel G Control Parameter 27

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address	register name	default value	R/W	description
0x5C98	XTC_3C_CTRL_0280	–	RW	Gb2 Channel G Control Parameter 28
0x5C99	XTC_3C_CTRL_0281	–	RW	Gb2 Channel G Control Parameter 29
0x5C9A	XTC_3C_CTRL_0282	–	RW	Gb2 Channel G Control Parameter 30
0x5C9B	XTC_3C_CTRL_0283	–	RW	Gb2 Channel G Control Parameter 31
0x5C9C	XTC_3C_CTRL_0284	–	RW	Gb2 Channel G Control Parameter 32
0x5C9D	XTC_3C_CTRL_0285	–	RW	Gb2 Channel G Control Parameter 33
0x5C9E	XTC_3C_CTRL_0286	–	RW	Gb2 Channel G Control Parameter 34
0x5C9F	XTC_3C_CTRL_0287	–	RW	Gb2 Channel G Control Parameter 35
0x5CA0	XTC_3C_CTRL_028	–	RW	Gb2 Channel R Control Parameter 0
0x5CA1	XTC_3C_CTRL_0289	–	RW	Gb2 Channel R Control Parameter 1
0x5CA2	XTC_3C_CTRL_0290	–	RW	Gb2 Channel R Control Parameter 2
0x5CA3	XTC_3C_CTRL_0291	–	RW	Gb2 Channel R Control Parameter 3
0x5CA4	XTC_3C_CTRL_0292	–	RW	Gb2 Channel R Control Parameter 4
0x5CA5	XTC_3C_CTRL_0293	–	RW	Gb2 Channel R Control Parameter 5
0x5CA6	XTC_3C_CTRL_0294	–	RW	Gb2 Channel R Control Parameter 6
0x5CA7	XTC_3C_CTRL_0295	–	RW	Gb2 Channel R Control Parameter 7
0x5CA8	XTC_3C_CTRL_0296	–	RW	Gb2 Channel R Control Parameter 8
0x5CA9	XTC_3C_CTRL_0297	–	RW	Gb2 Channel R Control Parameter 9
0x5CAA	XTC_3C_CTRL_0298	–	RW	Gb2 Channel R Control Parameter 10
0x5CAB	XTC_3C_CTRL_0299	–	RW	Gb2 Channel R Control Parameter 11
0x5CAC	XTC_3C_CTRL_0300	–	RW	Gb2 Channel R Control Parameter 12
0x5CAD	XTC_3C_CTRL_0301	–	RW	Gb2 Channel R Control Parameter 13
0x5CAE	XTC_3C_CTRL_0302	–	RW	Gb2 Channel R Control Parameter 14
0x5CAF	XTC_3C_CTRL_0303	–	RW	Gb2 Channel R Control Parameter 15
0x5CB0	XTC_3C_CTRL_0304	–	RW	Gb2 Channel R Control Parameter 16
0x5CB1	XTC_3C_CTRL_0305	–	RW	Gb2 Channel R Control Parameter 17
0x5CB2	XTC_3C_CTRL_0306	–	RW	Gb2 Channel R Control Parameter 18
0x5CB3	XTC_3C_CTRL_0307	–	RW	Gb2 Channel R Control Parameter 19
0x5CB4	XTC_3C_CTRL_0308	–	RW	Gb2 Channel R Control Parameter 20
0x5CB5	XTC_3C_CTRL_0309	–	RW	Gb2 Channel R Control Parameter 21

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address	register name	default value	R/W	description
0x5CB6	XTC_3C_CTRL_0310	–	RW	Gb2 Channel R Control Parameter 22
0x5CB7	XTC_3C_CTRL_0311	–	RW	Gb2 Channel R Control Parameter 23
0x5CB8	XTC_3C_CTRL_0312	–	RW	Gb2 Channel R Control Parameter 24
0x5CB9	XTC_3C_CTRL_0313	–	RW	Gb2 Channel R Control Parameter 25
0x5CBA	XTC_3C_CTRL_0314	–	RW	Gb2 Channel R Control Parameter 26
0x5CBB	XTC_3C_CTRL_0315	–	RW	Gb2 Channel R Control Parameter 27
0x5CBC	XTC_3C_CTRL_0316	–	RW	Gb2 Channel R Control Parameter 28
0x5CBD	XTC_3C_CTRL_0317	–	RW	Gb2 Channel R Control Parameter 29
0x5CBE	XTC_3C_CTRL_0318	–	RW	Gb2 Channel R Control Parameter 30
0x5CBF	XTC_3C_CTRL_0319	–	RW	Gb2 Channel R Control Parameter 31
0x5CC0	XTC_3C_CTRL_0320	–	RW	Gb2 Channel R Control Parameter 32
0x5CC1	XTC_3C_CTRL_0321	–	RW	Gb2 Channel R Control Parameter 33
0x5CC2	XTC_3C_CTRL_0322	–	RW	Gb2 Channel R Control Parameter 34
0x5CC3	XTC_3C_CTRL_0323	–	RW	Gb2 Channel R Control Parameter 35
0x5CC4	XTC_3C_CTRL_0324	–	RW	Gb3 Channel B Control Parameter 0
0x5CC5	XTC_3C_CTRL_0325	–	RW	Gb3 Channel B Control Parameter 1
0x5CC6	XTC_3C_CTRL_0326	–	RW	Gb3 Channel B Control Parameter 2
0x5CC7	XTC_3C_CTRL_0327	–	RW	Gb3 Channel B Control Parameter 3
0x5CC8	XTC_3C_CTRL_0328	–	RW	Gb3 Channel B Control Parameter 4
0x5CC9	XTC_3C_CTRL_0329	–	RW	Gb3 Channel B Control Parameter 5
0x5CCA	XTC_3C_CTRL_0330	–	RW	Gb3 Channel B Control Parameter 6
0x5CCB	XTC_3C_CTRL_0331	–	RW	Gb3 Channel B Control Parameter 7
0x5CCC	XTC_3C_CTRL_0332	–	RW	Gb3 Channel B Control Parameter 8
0x5CCD	XTC_3C_CTRL_0333	–	RW	Gb3 Channel B Control Parameter 9
0x5CCE	XTC_3C_CTRL_0334	–	RW	Gb3 Channel B Control Parameter 10
0x5CCF	XTC_3C_CTRL_0335	–	RW	Gb3 Channel B Control Parameter 11
0x5CD0	XTC_3C_CTRL_0336	–	RW	Gb3 Channel B Control Parameter 12
0x5CD1	XTC_3C_CTRL_0337	–	RW	Gb3 Channel B Control Parameter 13
0x5CD2	XTC_3C_CTRL_0338	–	RW	Gb3 Channel B Control Parameter 14
0x5CD3	XTC_3C_CTRL_0339	–	RW	Gb3 Channel B Control Parameter 15

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address	register name	default value	R/W	description
0x5CD4	XTC_3C_CTRL_0340	–	RW	Gb3 Channel B Control Parameter 16
0x5CD5	XTC_3C_CTRL_0341	–	RW	Gb3 Channel B Control Parameter 17
0x5CD6	XTC_3C_CTRL_0342	–	RW	Gb3 Channel B Control Parameter 18
0x5CD7	XTC_3C_CTRL_0343	–	RW	Gb3 Channel B Control Parameter 19
0x5CD8	XTC_3C_CTRL_0344	–	RW	Gb3 Channel B Control Parameter 20
0x5CD9	XTC_3C_CTRL_0345	–	RW	Gb3 Channel B Control Parameter 21
0x5CDA	XTC_3C_CTRL_0346	–	RW	Gb3 Channel B Control Parameter 22
0x5CDB	XTC_3C_CTRL_0347	–	RW	Gb3 Channel B Control Parameter 23
0x5CDC	XTC_3C_CTRL_0348	–	RW	Gb3 Channel B Control Parameter 24
0x5CDD	XTC_3C_CTRL_0349	–	RW	Gb3 Channel B Control Parameter 25
0x5CDE	XTC_3C_CTRL_0350	–	RW	Gb3 Channel B Control Parameter 26
0x5CDF	XTC_3C_CTRL_0351	–	RW	Gb3 Channel B Control Parameter 27
0x5CE0	XTC_3C_CTRL_0352	–	RW	Gb3 Channel B Control Parameter 28
0x5CE1	XTC_3C_CTRL_0353	–	RW	Gb3 Channel B Control Parameter 29
0x5CE2	XTC_3C_CTRL_0354	–	RW	Gb3 Channel B Control Parameter 30
0x5CE3	XTC_3C_CTRL_0355	–	RW	Gb3 Channel B Control Parameter 31
0x5CE4	XTC_3C_CTRL_0356	–	RW	Gb3 Channel B Control Parameter 32
0x5CE5	XTC_3C_CTRL_0357	–	RW	Gb3 Channel B Control Parameter 33
0x5CE6	XTC_3C_CTRL_0358	–	RW	Gb3 Channel B Control Parameter 34
0x5CE7	XTC_3C_CTRL_0359	–	RW	Gb3 Channel B Control Parameter 35
0x5CE8	XTC_3C_CTRL_0360	–	RW	Gb3 Channel G Control Parameter 0
0x5CE9	XTC_3C_CTRL_0361	–	RW	Gb3 Channel G Control Parameter 1
0x5CEA	XTC_3C_CTRL_0362	–	RW	Gb3 Channel G Control Parameter 2
0x5CEB	XTC_3C_CTRL_0363	–	RW	Gb3 Channel G Control Parameter 3
0x5CEC	XTC_3C_CTRL_0364	–	RW	Gb3 Channel G Control Parameter 4
0x5CED	XTC_3C_CTRL_0365	–	RW	Gb3 Channel G Control Parameter 5
0x5CEE	XTC_3C_CTRL_0366	–	RW	Gb3 Channel G Control Parameter 6
0x5CEF	XTC_3C_CTRL_0367	–	RW	Gb3 Channel G Control Parameter 7
0x5CF0	XTC_3C_CTRL_0368	–	RW	Gb3 Channel G Control Parameter 8
0x5CF1	XTC_3C_CTRL_0369	–	RW	Gb3 Channel G Control Parameter 9

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address	register name	default value	R/W	description
0x5CF2	XTC_3C_CTRL_0370	–	RW	Gb3 Channel G Control Parameter 10
0x5CF3	XTC_3C_CTRL_0371	–	RW	Gb3 Channel G Control Parameter 11
0x5CF4	XTC_3C_CTRL_0372	–	RW	Gb3 Channel G Control Parameter 12
0x5CF5	XTC_3C_CTRL_0373	–	RW	Gb3 Channel G Control Parameter 13
0x5CF6	XTC_3C_CTRL_0374	–	RW	Gb3 Channel G Control Parameter 14
0x5CF7	XTC_3C_CTRL_0375	–	RW	Gb3 Channel G Control Parameter 15
0x5CF8	XTC_3C_CTRL_0376	–	RW	Gb3 Channel G Control Parameter 16
0x5CF9	XTC_3C_CTRL_0377	–	RW	Gb3 Channel G Control Parameter 17
0x5CFA	XTC_3C_CTRL_0378	–	RW	Gb3 Channel G Control Parameter 18
0x5CFB	XTC_3C_CTRL_0379	–	RW	Gb3 Channel G Control Parameter 19
0x5CFC	XTC_3C_CTRL_0380	–	RW	Gb3 Channel G Control Parameter 20
0x5CFD	XTC_3C_CTRL_0381	–	RW	Gb3 Channel G Control Parameter 21
0x5CFE	XTC_3C_CTRL_0382	–	RW	Gb3 Channel G Control Parameter 22
0x5CFF	XTC_3C_CTRL_0383	–	RW	Gb3 Channel G Control Parameter 23
0x5D00	XTC_3C_CTRL_0384	–	RW	Gb3 Channel G Control Parameter 24
0x5D01	XTC_3C_CTRL_0385	–	RW	Gb3 Channel G Control Parameter 25
0x5D02	XTC_3C_CTRL_0386	–	RW	Gb3 Channel G Control Parameter 26
0x5D03	XTC_3C_CTRL_0387	–	RW	Gb3 Channel G Control Parameter 27
0x5D04	XTC_3C_CTRL_038	–	RW	Gb3 Channel G Control Parameter 28
0x5D05	XTC_3C_CTRL_0389	–	RW	Gb3 Channel G Control Parameter 29
0x5D06	XTC_3C_CTRL_0390	–	RW	Gb3 Channel G Control Parameter 30
0x5D07	XTC_3C_CTRL_0391	–	RW	Gb3 Channel G Control Parameter 31
0x5D08	XTC_3C_CTRL_0392	–	RW	Gb3 Channel G Control Parameter 32
0x5D09	XTC_3C_CTRL_0393	–	RW	Gb3 Channel G Control Parameter 33
0x5D0A	XTC_3C_CTRL_0394	–	RW	Gb3 Channel G Control Parameter 34
0x5D0B	XTC_3C_CTRL_0395	–	RW	Gb3 Channel G Control Parameter 35
0x5D0C	XTC_3C_CTRL_0396	–	RW	Gb3 Channel R Control Parameter 0
0x5D0D	XTC_3C_CTRL_0397	–	RW	Gb3 Channel R Control Parameter 1
0x5D0E	XTC_3C_CTRL_0398	–	RW	Gb3 Channel R Control Parameter 2
0x5D0F	XTC_3C_CTRL_0399	–	RW	Gb3 Channel R Control Parameter 3

table 6-64 XTC_3C registers (sheet 15 of 30)

address	register name	default value	R/W	description
0x5D10	XTC_3C_CTRL_0400	–	RW	Gb3 Channel R Control Parameter 4
0x5D11	XTC_3C_CTRL_0401	–	RW	Gb3 Channel R Control Parameter 5
0x5D12	XTC_3C_CTRL_0402	–	RW	Gb3 Channel R Control Parameter 6
0x5D13	XTC_3C_CTRL_0403	–	RW	Gb3 Channel R Control Parameter 7
0x5D14	XTC_3C_CTRL_0404	–	RW	Gb3 Channel R Control Parameter 8
0x5D15	XTC_3C_CTRL_0405	–	RW	Gb3 Channel R Control Parameter 9
0x5D16	XTC_3C_CTRL_0406	–	RW	Gb3 Channel R Control Parameter 10
0x5D17	XTC_3C_CTRL_0407	–	RW	Gb3 Channel R Control Parameter 11
0x5D18	XTC_3C_CTRL_0408	–	RW	Gb3 Channel R Control Parameter 12
0x5D19	XTC_3C_CTRL_0409	–	RW	Gb3 Channel R Control Parameter 13
0x5D1A	XTC_3C_CTRL_0410	–	RW	Gb3 Channel R Control Parameter 14
0x5D1B	XTC_3C_CTRL_0411	–	RW	Gb3 Channel R Control Parameter 15
0x5D1C	XTC_3C_CTRL_0412	–	RW	Gb3 Channel R Control Parameter 16
0x5D1D	XTC_3C_CTRL_0413	–	RW	Gb3 Channel R Control Parameter 17
0x5D1E	XTC_3C_CTRL_0414	–	RW	Gb3 Channel R Control Parameter 18
0x5D1F	XTC_3C_CTRL_0415	–	RW	Gb3 Channel R Control Parameter 19
0x5D20	XTC_3C_CTRL_0416	–	RW	Gb3 Channel R Control Parameter 20
0x5D21	XTC_3C_CTRL_0417	–	RW	Gb3 Channel R Control Parameter 21
0x5D22	XTC_3C_CTRL_0418	–	RW	Gb3 Channel R Control Parameter 22
0x5D23	XTC_3C_CTRL_0419	–	RW	Gb3 Channel R Control Parameter 23
0x5D24	XTC_3C_CTRL_0420	–	RW	Gb3 Channel R Control Parameter 24
0x5D25	XTC_3C_CTRL_0421	–	RW	Gb3 Channel R Control Parameter 25
0x5D26	XTC_3C_CTRL_0422	–	RW	Gb3 Channel R Control Parameter 26
0x5D27	XTC_3C_CTRL_0423	–	RW	Gb3 Channel R Control Parameter 27
0x5D28	XTC_3C_CTRL_0424	–	RW	Gb3 Channel R Control Parameter 28
0x5D29	XTC_3C_CTRL_0425	–	RW	Gb3 Channel R Control Parameter 29
0x5D2A	XTC_3C_CTRL_0426	–	RW	Gb3 Channel R Control Parameter 30
0x5D2B	XTC_3C_CTRL_0427	–	RW	Gb3 Channel R Control Parameter 31
0x5D2C	XTC_3C_CTRL_0428	–	RW	Gb3 Channel R Control Parameter 32
0x5D2D	XTC_3C_CTRL_0429	–	RW	Gb3 Channel R Control Parameter 33

table 6-64 XTC_3C registers (sheet 16 of 30)

address	register name	default value	R/W	description
0x5D2E	XTC_3C_CTRL_0430	–	RW	Gb3 Channel R Control Parameter 34
0x5D2F	XTC_3C_CTRL_0431	–	RW	Gb3 Channel R Control Parameter 35
0x5D30	XTC_3C_CTRL_0432	–	RW	Gr0 Channel B Control Parameter 0
0x5D31	XTC_3C_CTRL_0433	–	RW	Gr0 Channel B Control Parameter 1
0x5D32	XTC_3C_CTRL_0434	–	RW	Gr0 Channel B Control Parameter 2
0x5D33	XTC_3C_CTRL_0435	–	RW	Gr0 Channel B Control Parameter 3
0x5D34	XTC_3C_CTRL_0436	–	RW	Gr0 Channel B Control Parameter 4
0x5D35	XTC_3C_CTRL_0437	–	RW	Gr0 Channel B Control Parameter 5
0x5D36	XTC_3C_CTRL_0438	–	RW	Gr0 Channel B Control Parameter 6
0x5D37	XTC_3C_CTRL_0439	–	RW	Gr0 Channel B Control Parameter 7
0x5D38	XTC_3C_CTRL_0440	–	RW	Gr0 Channel B Control Parameter 8
0x5D39	XTC_3C_CTRL_0441	–	RW	Gr0 Channel B Control Parameter 9
0x5D3A	XTC_3C_CTRL_0442	–	RW	Gr0 Channel B Control Parameter 10
0x5D3B	XTC_3C_CTRL_0443	–	RW	Gr0 Channel B Control Parameter 11
0x5D3C	XTC_3C_CTRL_0444	–	RW	Gr0 Channel B Control Parameter 12
0x5D3D	XTC_3C_CTRL_0445	–	RW	Gr0 Channel B Control Parameter 13
0x5D3E	XTC_3C_CTRL_0446	–	RW	Gr0 Channel B Control Parameter 14
0x5D3F	XTC_3C_CTRL_0447	–	RW	Gr0 Channel B Control Parameter 15
0x5D40	XTC_3C_CTRL_0448	–	RW	Gr0 Channel B Control Parameter 16
0x5D41	XTC_3C_CTRL_0449	–	RW	Gr0 Channel B Control Parameter 17
0x5D42	XTC_3C_CTRL_0450	–	RW	Gr0 Channel B Control Parameter 18
0x5D43	XTC_3C_CTRL_0451	–	RW	Gr0 Channel B Control Parameter 19
0x5D44	XTC_3C_CTRL_0452	–	RW	Gr0 Channel B Control Parameter 20
0x5D45	XTC_3C_CTRL_0453	–	RW	Gr0 Channel B Control Parameter 21
0x5D46	XTC_3C_CTRL_0454	–	RW	Gr0 Channel B Control Parameter 22
0x5D47	XTC_3C_CTRL_0455	–	RW	Gr0 Channel B Control Parameter 23
0x5D48	XTC_3C_CTRL_0456	–	RW	Gr0 Channel B Control Parameter 24
0x5D49	XTC_3C_CTRL_0457	–	RW	Gr0 Channel B Control Parameter 25
0x5D4A	XTC_3C_CTRL_0458	–	RW	Gr0 Channel B Control Parameter 26
0x5D4B	XTC_3C_CTRL_0459	–	RW	Gr0 Channel B Control Parameter 27

table 6-64 XTC_3C registers (sheet 17 of 30)

address	register name	default value	R/W	description
0x5D4C	XTC_3C_CTRL_0460	–	RW	Gr0 Channel B Control Parameter 28
0x5D4D	XTC_3C_CTRL_0461	–	RW	Gr0 Channel B Control Parameter 29
0x5D4E	XTC_3C_CTRL_0462	–	RW	Gr0 Channel B Control Parameter 30
0x5D4F	XTC_3C_CTRL_0463	–	RW	Gr0 Channel B Control Parameter 31
0x5D50	XTC_3C_CTRL_0464	–	RW	Gr0 Channel B Control Parameter 32
0x5D51	XTC_3C_CTRL_0465	–	RW	Gr0 Channel B Control Parameter 33
0x5D52	XTC_3C_CTRL_0466	–	RW	Gr0 Channel B Control Parameter 34
0x5D53	XTC_3C_CTRL_0467	–	RW	Gr0 Channel B Control Parameter 35
0x5D54	XTC_3C_CTRL_0468	–	RW	Gr0 Channel G Control Parameter 0
0x5D55	XTC_3C_CTRL_0469	–	RW	Gr0 Channel G Control Parameter 1
0x5D56	XTC_3C_CTRL_0470	–	RW	Gr0 Channel G Control Parameter 2
0x5D57	XTC_3C_CTRL_0471	–	RW	Gr0 Channel G Control Parameter 3
0x5D58	XTC_3C_CTRL_0472	–	RW	Gr0 Channel G Control Parameter 4
0x5D59	XTC_3C_CTRL_0473	–	RW	Gr0 Channel G Control Parameter 5
0x5D5A	XTC_3C_CTRL_0474	–	RW	Gr0 Channel G Control Parameter 6
0x5D5B	XTC_3C_CTRL_0475	–	RW	Gr0 Channel G Control Parameter 7
0x5D5C	XTC_3C_CTRL_0476	–	RW	Gr0 Channel G Control Parameter 8
0x5D5D	XTC_3C_CTRL_0477	–	RW	Gr0 Channel G Control Parameter 9
0x5D5E	XTC_3C_CTRL_0478	–	RW	Gr0 Channel G Control Parameter 10
0x5D5F	XTC_3C_CTRL_0479	–	RW	Gr0 Channel G Control Parameter 11
0x5D60	XTC_3C_CTRL_0480	–	RW	Gr0 Channel G Control Parameter 12
0x5D61	XTC_3C_CTRL_0481	–	RW	Gr0 Channel G Control Parameter 13
0x5D62	XTC_3C_CTRL_0482	–	RW	Gr0 Channel G Control Parameter 14
0x5D63	XTC_3C_CTRL_0483	–	RW	Gr0 Channel G Control Parameter 15
0x5D64	XTC_3C_CTRL_0484	–	RW	Gr0 Channel G Control Parameter 16
0x5D65	XTC_3C_CTRL_0485	–	RW	Gr0 Channel G Control Parameter 17
0x5D66	XTC_3C_CTRL_0486	–	RW	Gr0 Channel G Control Parameter 18
0x5D67	XTC_3C_CTRL_0487	–	RW	Gr0 Channel G Control Parameter 19
0x5D68	XTC_3C_CTRL_048	–	RW	Gr0 Channel G Control Parameter 20
0x5D69	XTC_3C_CTRL_0489	–	RW	Gr0 Channel G Control Parameter 21

table 6-64 XTC_3C registers (sheet 18 of 30)

address	register name	default value	R/W	description
0x5D6A	XTC_3C_CTRL_0490	–	RW	Gr0 Channel G Control Parameter 22
0x5D6B	XTC_3C_CTRL_0491	–	RW	Gr0 Channel G Control Parameter 23
0x5D6C	XTC_3C_CTRL_0492	–	RW	Gr0 Channel G Control Parameter 24
0x5D6D	XTC_3C_CTRL_0493	–	RW	Gr0 Channel G Control Parameter 25
0x5D6E	XTC_3C_CTRL_0494	–	RW	Gr0 Channel G Control Parameter 26
0x5D6F	XTC_3C_CTRL_0495	–	RW	Gr0 Channel G Control Parameter 27
0x5D70	XTC_3C_CTRL_0496	–	RW	Gr0 Channel G Control Parameter 28
0x5D71	XTC_3C_CTRL_0497	–	RW	Gr0 Channel G Control Parameter 29
0x5D72	XTC_3C_CTRL_0498	–	RW	Gr0 Channel G Control Parameter 30
0x5D73	XTC_3C_CTRL_0499	–	RW	Gr0 Channel G Control Parameter 31
0x5D74	XTC_3C_CTRL_0500	–	RW	Gr0 Channel G Control Parameter 32
0x5D75	XTC_3C_CTRL_0501	–	RW	Gr0 Channel G Control Parameter 33
0x5D76	XTC_3C_CTRL_0502	–	RW	Gr0 Channel G Control Parameter 34
0x5D77	XTC_3C_CTRL_0503	–	RW	Gr0 Channel G Control Parameter 35
0x5D78	XTC_3C_CTRL_0504	–	RW	Gr0 Channel R Control Parameter 0
0x5D79	XTC_3C_CTRL_0505	–	RW	Gr0 Channel R Control Parameter 1
0x5D7A	XTC_3C_CTRL_0506	–	RW	Gr0 Channel R Control Parameter 2
0x5D7B	XTC_3C_CTRL_0507	–	RW	Gr0 Channel R Control Parameter 3
0x5D7C	XTC_3C_CTRL_0508	–	RW	Gr0 Channel R Control Parameter 4
0x5D7D	XTC_3C_CTRL_0509	–	RW	Gr0 Channel R Control Parameter 5
0x5D7E	XTC_3C_CTRL_0510	–	RW	Gr0 Channel R Control Parameter 6
0x5D7F	XTC_3C_CTRL_0511	–	RW	Gr0 Channel R Control Parameter 7
0x5D80	XTC_3C_CTRL_0512	–	RW	Gr0 Channel R Control Parameter 8
0x5D81	XTC_3C_CTRL_0513	–	RW	Gr0 Channel R Control Parameter 9
0x5D82	XTC_3C_CTRL_0514	–	RW	Gr0 Channel R Control Parameter 10
0x5D83	XTC_3C_CTRL_0515	–	RW	Gr0 Channel R Control Parameter 11
0x5D84	XTC_3C_CTRL_0516	–	RW	Gr0 Channel R Control Parameter 12
0x5D85	XTC_3C_CTRL_0517	–	RW	Gr0 Channel R Control Parameter 13
0x5D86	XTC_3C_CTRL_0518	–	RW	Gr0 Channel R Control Parameter 14
0x5D87	XTC_3C_CTRL_0519	–	RW	Gr0 Channel R Control Parameter 15

table 6-64 XTC_3C registers (sheet 19 of 30)

address	register name	default value	R/W	description
0x5D88	XTC_3C_CTRL_0520	–	RW	Gr0 Channel R Control Parameter 16
0x5D89	XTC_3C_CTRL_0521	–	RW	Gr0 Channel R Control Parameter 17
0x5D8A	XTC_3C_CTRL_0522	–	RW	Gr0 Channel R Control Parameter 18
0x5D8B	XTC_3C_CTRL_0523	–	RW	Gr0 Channel R Control Parameter 19
0x5D8C	XTC_3C_CTRL_0524	–	RW	Gr0 Channel R Control Parameter 20
0x5D8D	XTC_3C_CTRL_0525	–	RW	Gr0 Channel R Control Parameter 21
0x5D8E	XTC_3C_CTRL_0526	–	RW	Gr0 Channel R Control Parameter 22
0x5D8F	XTC_3C_CTRL_0527	–	RW	Gr0 Channel R Control Parameter 23
0x5D90	XTC_3C_CTRL_0528	–	RW	Gr0 Channel R Control Parameter 24
0x5D91	XTC_3C_CTRL_0529	–	RW	Gr0 Channel R Control Parameter 25
0x5D92	XTC_3C_CTRL_0530	–	RW	Gr0 Channel R Control Parameter 26
0x5D93	XTC_3C_CTRL_0531	–	RW	Gr0 Channel R Control Parameter 27
0x5D94	XTC_3C_CTRL_0532	–	RW	Gr0 Channel R Control Parameter 28
0x5D95	XTC_3C_CTRL_0533	–	RW	Gr0 Channel R Control Parameter 29
0x5D96	XTC_3C_CTRL_0534	–	RW	Gr0 Channel R Control Parameter 30
0x5D97	XTC_3C_CTRL_0535	–	RW	Gr0 Channel R Control Parameter 31
0x5D98	XTC_3C_CTRL_0536	–	RW	Gr0 Channel R Control Parameter 32
0x5D99	XTC_3C_CTRL_0537	–	RW	Gr0 Channel R Control Parameter 33
0x5D9A	XTC_3C_CTRL_0538	–	RW	Gr0 Channel R Control Parameter 34
0x5D9B	XTC_3C_CTRL_0539	–	RW	Gr0 Channel R Control Parameter 35
0x5D9C	XTC_3C_CTRL_0540	–	RW	Gr1 Channel B Control Parameter 0
0x5D9D	XTC_3C_CTRL_0541	–	RW	Gr1 Channel B Control Parameter 1
0x5D9E	XTC_3C_CTRL_0542	–	RW	Gr1 Channel B Control Parameter 2
0x5D9F	XTC_3C_CTRL_0543	–	RW	Gr1 Channel B Control Parameter 3
0x5DA0	XTC_3C_CTRL_0544	–	RW	Gr1 Channel B Control Parameter 4
0x5DA1	XTC_3C_CTRL_0545	–	RW	Gr1 Channel B Control Parameter 5
0x5DA2	XTC_3C_CTRL_0546	–	RW	Gr1 Channel B Control Parameter 6
0x5DA3	XTC_3C_CTRL_0547	–	RW	Gr1 Channel B Control Parameter 7
0x5DA4	XTC_3C_CTRL_0548	–	RW	Gr1 Channel B Control Parameter 8
0x5DA5	XTC_3C_CTRL_0549	–	RW	Gr1 Channel B Control Parameter 9

table 6-64 XTC_3C registers (sheet 20 of 30)

address	register name	default value	R/W	description
0x5DA6	XTC_3C_CTRL_0550	–	RW	Gr1 Channel B Control Parameter 10
0x5DA7	XTC_3C_CTRL_0551	–	RW	Gr1 Channel B Control Parameter 11
0x5DA8	XTC_3C_CTRL_0552	–	RW	Gr1 Channel B Control Parameter 12
0x5DA9	XTC_3C_CTRL_0553	–	RW	Gr1 Channel B Control Parameter 13
0x5DAA	XTC_3C_CTRL_0554	–	RW	Gr1 Channel B Control Parameter 14
0x5DAB	XTC_3C_CTRL_0555	–	RW	Gr1 Channel B Control Parameter 15
0x5DAC	XTC_3C_CTRL_0556	–	RW	Gr1 Channel B Control Parameter 16
0x5DAD	XTC_3C_CTRL_0557	–	RW	Gr1 Channel B Control Parameter 17
0x5DAE	XTC_3C_CTRL_0558	–	RW	Gr1 Channel B Control Parameter 18
0x5DAF	XTC_3C_CTRL_0559	–	RW	Gr1 Channel B Control Parameter 19
0x5DB0	XTC_3C_CTRL_0560	–	RW	Gr1 Channel B Control Parameter 20
0x5DB1	XTC_3C_CTRL_0561	–	RW	Gr1 Channel B Control Parameter 21
0x5DB2	XTC_3C_CTRL_0562	–	RW	Gr1 Channel B Control Parameter 22
0x5DB3	XTC_3C_CTRL_0563	–	RW	Gr1 Channel B Control Parameter 23
0x5DB4	XTC_3C_CTRL_0564	–	RW	Gr1 Channel B Control Parameter 24
0x5DB5	XTC_3C_CTRL_0565	–	RW	Gr1 Channel B Control Parameter 25
0x5DB6	XTC_3C_CTRL_0566	–	RW	Gr1 Channel B Control Parameter 26
0x5DB7	XTC_3C_CTRL_0567	–	RW	Gr1 Channel B Control Parameter 27
0x5DB8	XTC_3C_CTRL_0568	–	RW	Gr1 Channel B Control Parameter 28
0x5DB9	XTC_3C_CTRL_0569	–	RW	Gr1 Channel B Control Parameter 29
0x5DBA	XTC_3C_CTRL_0570	–	RW	Gr1 Channel B Control Parameter 30
0x5DBB	XTC_3C_CTRL_0571	–	RW	Gr1 Channel B Control Parameter 31
0x5DBC	XTC_3C_CTRL_0572	–	RW	Gr1 Channel B Control Parameter 32
0x5DBD	XTC_3C_CTRL_0573	–	RW	Gr1 Channel B Control Parameter 33
0x5DBE	XTC_3C_CTRL_0574	–	RW	Gr1 Channel B Control Parameter 34
0x5DBF	XTC_3C_CTRL_0575	–	RW	Gr1 Channel B Control Parameter 35
0x5DC0	XTC_3C_CTRL_0576	–	RW	Gr1 Channel G Control Parameter 0
0x5DC1	XTC_3C_CTRL_0577	–	RW	Gr1 Channel G Control Parameter 1
0x5DC2	XTC_3C_CTRL_0578	–	RW	Gr1 Channel G Control Parameter 2
0x5DC3	XTC_3C_CTRL_0579	–	RW	Gr1 Channel G Control Parameter 3

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address	register name	default value	R/W	description
0x5DC4	XTC_3C_CTRL_0580	–	RW	Gr1 Channel G Control Parameter 4
0x5DC5	XTC_3C_CTRL_0581	–	RW	Gr1 Channel G Control Parameter 5
0x5DC6	XTC_3C_CTRL_0582	–	RW	Gr1 Channel G Control Parameter 6
0x5DC7	XTC_3C_CTRL_0583	–	RW	Gr1 Channel G Control Parameter 7
0x5DC8	XTC_3C_CTRL_0584	–	RW	Gr1 Channel G Control Parameter 8
0x5DC9	XTC_3C_CTRL_0585	–	RW	Gr1 Channel G Control Parameter 9
0x5DCA	XTC_3C_CTRL_0586	–	RW	Gr1 Channel G Control Parameter 10
0x5DCB	XTC_3C_CTRL_0587	–	RW	Gr1 Channel G Control Parameter 11
0x5DCC	XTC_3C_CTRL_058	–	RW	Gr1 Channel G Control Parameter 12
0x5DCD	XTC_3C_CTRL_0589	–	RW	Gr1 Channel G Control Parameter 13
0x5DCE	XTC_3C_CTRL_0590	–	RW	Gr1 Channel G Control Parameter 14
0x5DCF	XTC_3C_CTRL_0591	–	RW	Gr1 Channel G Control Parameter 15
0x5DD0	XTC_3C_CTRL_0592	–	RW	Gr1 Channel G Control Parameter 16
0x5DD1	XTC_3C_CTRL_0593	–	RW	Gr1 Channel G Control Parameter 17
0x5DD2	XTC_3C_CTRL_0594	–	RW	Gr1 Channel G Control Parameter 18
0x5DD3	XTC_3C_CTRL_0595	–	RW	Gr1 Channel G Control Parameter 19
0x5DD4	XTC_3C_CTRL_0596	–	RW	Gr1 Channel G Control Parameter 20
0x5DD5	XTC_3C_CTRL_0597	–	RW	Gr1 Channel G Control Parameter 21
0x5DD6	XTC_3C_CTRL_0598	–	RW	Gr1 Channel G Control Parameter 22
0x5DD7	XTC_3C_CTRL_0599	–	RW	Gr1 Channel G Control Parameter 23
0x5DD8	XTC_3C_CTRL_0600	–	RW	Gr1 Channel G Control Parameter 24
0x5DD9	XTC_3C_CTRL_0601	–	RW	Gr1 Channel G Control Parameter 25
0x5DDA	XTC_3C_CTRL_0602	–	RW	Gr1 Channel G Control Parameter 26
0x5DDB	XTC_3C_CTRL_0603	–	RW	Gr1 Channel G Control Parameter 27
0x5DDC	XTC_3C_CTRL_0604	–	RW	Gr1 Channel G Control Parameter 28
0x5DDD	XTC_3C_CTRL_0605	–	RW	Gr1 Channel G Control Parameter 29
0x5DDE	XTC_3C_CTRL_0606	–	RW	Gr1 Channel G Control Parameter 30
0x5DDF	XTC_3C_CTRL_0607	–	RW	Gr1 Channel G Control Parameter 31
0x5DE0	XTC_3C_CTRL_0608	–	RW	Gr1 Channel G Control Parameter 32
0x5DE1	XTC_3C_CTRL_0609	–	RW	Gr1 Channel G Control Parameter 33

table 6-64 XTC_3C registers (sheet 22 of 30)

address	register name	default value	R/W	description
0x5DE2	XTC_3C_CTRL_0610	–	RW	Gr1 Channel G Control Parameter 34
0x5DE3	XTC_3C_CTRL_0611	–	RW	Gr1 Channel G Control Parameter 35
0x5DE4	XTC_3C_CTRL_0612	–	RW	Gr1 Channel R Control Parameter 0
0x5DE5	XTC_3C_CTRL_0613	–	RW	Gr1 Channel R Control Parameter 1
0x5DE6	XTC_3C_CTRL_0614	–	RW	Gr1 Channel R Control Parameter 2
0x5DE7	XTC_3C_CTRL_0615	–	RW	Gr1 Channel R Control Parameter 3
0x5DE8	XTC_3C_CTRL_0616	–	RW	Gr1 Channel R Control Parameter 4
0x5DE9	XTC_3C_CTRL_0617	–	RW	Gr1 Channel R Control Parameter 5
0x5DEA	XTC_3C_CTRL_0618	–	RW	Gr1 Channel R Control Parameter 6
0x5DEB	XTC_3C_CTRL_0619	–	RW	Gr1 Channel R Control Parameter 7
0x5DEC	XTC_3C_CTRL_0620	–	RW	Gr1 Channel R Control Parameter 8
0x5DED	XTC_3C_CTRL_0621	–	RW	Gr1 Channel R Control Parameter 9
0x5DEE	XTC_3C_CTRL_0622	–	RW	Gr1 Channel R Control Parameter 10
0x5DEF	XTC_3C_CTRL_0623	–	RW	Gr1 Channel R Control Parameter 11
0x5DF0	XTC_3C_CTRL_0624	–	RW	Gr1 Channel R Control Parameter 12
0x5DF1	XTC_3C_CTRL_0625	–	RW	Gr1 Channel R Control Parameter 13
0x5DF2	XTC_3C_CTRL_0626	–	RW	Gr1 Channel R Control Parameter 14
0x5DF3	XTC_3C_CTRL_0627	–	RW	Gr1 Channel R Control Parameter 15
0x5DF4	XTC_3C_CTRL_0628	–	RW	Gr1 Channel R Control Parameter 16
0x5DF5	XTC_3C_CTRL_0629	–	RW	Gr1 Channel R Control Parameter 17
0x5DF6	XTC_3C_CTRL_0630	–	RW	Gr1 Channel R Control Parameter 18
0x5DF7	XTC_3C_CTRL_0631	–	RW	Gr1 Channel R Control Parameter 19
0x5DF8	XTC_3C_CTRL_0632	–	RW	Gr1 Channel R Control Parameter 20
0x5DF9	XTC_3C_CTRL_0633	–	RW	Gr1 Channel R Control Parameter 21
0x5DFA	XTC_3C_CTRL_0634	–	RW	Gr1 Channel R Control Parameter 22
0x5DFB	XTC_3C_CTRL_0635	–	RW	Gr1 Channel R Control Parameter 23
0x5DFC	XTC_3C_CTRL_0636	–	RW	Gr1 Channel R Control Parameter 24
0x5DFD	XTC_3C_CTRL_0637	–	RW	Gr1 Channel R Control Parameter 25
0x5DFE	XTC_3C_CTRL_0638	–	RW	Gr1 Channel R Control Parameter 26
0x5DFF	XTC_3C_CTRL_0639	–	RW	Gr1 Channel R Control Parameter 27

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address	register name	default value	R/W	description
0x5E00	XTC_3C_CTRL_0640	–	RW	Gr1 Channel R Control Parameter 28
0x5E01	XTC_3C_CTRL_0641	–	RW	Gr1 Channel R Control Parameter 29
0x5E02	XTC_3C_CTRL_0642	–	RW	Gr1 Channel R Control Parameter 30
0x5E03	XTC_3C_CTRL_0643	–	RW	Gr1 Channel R Control Parameter 31
0x5E04	XTC_3C_CTRL_0644	–	RW	Gr1 Channel R Control Parameter 32
0x5E05	XTC_3C_CTRL_0645	–	RW	Gr1 Channel R Control Parameter 33
0x5E06	XTC_3C_CTRL_0646	–	RW	Gr1 Channel R Control Parameter 34
0x5E07	XTC_3C_CTRL_0647	–	RW	Gr1 Channel R Control Parameter 35
0x5E08	XTC_3C_CTRL_0648	–	RW	Gr2 Channel B Control Parameter 0
0x5E09	XTC_3C_CTRL_0649	–	RW	Gr2 Channel B Control Parameter 1
0x5E0A	XTC_3C_CTRL_0650	–	RW	Gr2 Channel B Control Parameter 2
0x5E0B	XTC_3C_CTRL_0651	–	RW	Gr2 Channel B Control Parameter 3
0x5E0C	XTC_3C_CTRL_0652	–	RW	Gr2 Channel B Control Parameter 4
0x5E0D	XTC_3C_CTRL_0653	–	RW	Gr2 Channel B Control Parameter 5
0x5E0E	XTC_3C_CTRL_0654	–	RW	Gr2 Channel B Control Parameter 6
0x5E0F	XTC_3C_CTRL_0655	–	RW	Gr2 Channel B Control Parameter 7
0x5E10	XTC_3C_CTRL_0656	–	RW	Gr2 Channel B Control Parameter 8
0x5E11	XTC_3C_CTRL_0657	–	RW	Gr2 Channel B Control Parameter 9
0x5E12	XTC_3C_CTRL_0658	–	RW	Gr2 Channel B Control Parameter 10
0x5E13	XTC_3C_CTRL_0659	–	RW	Gr2 Channel B Control Parameter 11
0x5E14	XTC_3C_CTRL_0660	–	RW	Gr2 Channel B Control Parameter 12
0x5E15	XTC_3C_CTRL_0661	–	RW	Gr2 Channel B Control Parameter 13
0x5E16	XTC_3C_CTRL_0662	–	RW	Gr2 Channel B Control Parameter 14
0x5E17	XTC_3C_CTRL_0663	–	RW	Gr2 Channel B Control Parameter 15
0x5E18	XTC_3C_CTRL_0664	–	RW	Gr2 Channel B Control Parameter 16
0x5E19	XTC_3C_CTRL_0665	–	RW	Gr2 Channel B Control Parameter 17
0x5E1A	XTC_3C_CTRL_0666	–	RW	Gr2 Channel B Control Parameter 18
0x5E1B	XTC_3C_CTRL_0667	–	RW	Gr2 Channel B Control Parameter 19
0x5E1C	XTC_3C_CTRL_0668	–	RW	Gr2 Channel B Control Parameter 20
0x5E1D	XTC_3C_CTRL_0669	–	RW	Gr2 Channel B Control Parameter 21

table 6-64 XTC_3C registers (sheet 24 of 30)

address	register name	default value	R/W	description
0x5E1E	XTC_3C_CTRL_0670	–	RW	Gr2 Channel B Control Parameter 22
0x5E1F	XTC_3C_CTRL_0671	–	RW	Gr2 Channel B Control Parameter 23
0x5E20	XTC_3C_CTRL_0672	–	RW	Gr2 Channel B Control Parameter 24
0x5E21	XTC_3C_CTRL_0673	–	RW	Gr2 Channel B Control Parameter 25
0x5E22	XTC_3C_CTRL_0674	–	RW	Gr2 Channel B Control Parameter 26
0x5E23	XTC_3C_CTRL_0675	–	RW	Gr2 Channel B Control Parameter 27
0x5E24	XTC_3C_CTRL_0676	–	RW	Gr2 Channel B Control Parameter 28
0x5E25	XTC_3C_CTRL_0677	–	RW	Gr2 Channel B Control Parameter 29
0x5E26	XTC_3C_CTRL_0678	–	RW	Gr2 Channel B Control Parameter 30
0x5E27	XTC_3C_CTRL_0679	–	RW	Gr2 Channel B Control Parameter 31
0x5E28	XTC_3C_CTRL_0680	–	RW	Gr2 Channel B Control Parameter 32
0x5E29	XTC_3C_CTRL_0681	–	RW	Gr2 Channel B Control Parameter 33
0x5E2A	XTC_3C_CTRL_0682	–	RW	Gr2 Channel B Control Parameter 34
0x5E2B	XTC_3C_CTRL_0683	–	RW	Gr2 Channel B Control Parameter 35
0x5E2C	XTC_3C_CTRL_0684	–	RW	Gr2 Channel G Control Parameter 0
0x5E2D	XTC_3C_CTRL_0685	–	RW	Gr2 Channel G Control Parameter 1
0x5E2E	XTC_3C_CTRL_0686	–	RW	Gr2 Channel G Control Parameter 2
0x5E2F	XTC_3C_CTRL_0687	–	RW	Gr2 Channel G Control Parameter 3
0x5E30	XTC_3C_CTRL_068	–	RW	Gr2 Channel G Control Parameter 4
0x5E31	XTC_3C_CTRL_0689	–	RW	Gr2 Channel G Control Parameter 5
0x5E32	XTC_3C_CTRL_0690	–	RW	Gr2 Channel G Control Parameter 6
0x5E33	XTC_3C_CTRL_0691	–	RW	Gr2 Channel G Control Parameter 7
0x5E34	XTC_3C_CTRL_0692	–	RW	Gr2 Channel G Control Parameter 8
0x5E35	XTC_3C_CTRL_0693	–	RW	Gr2 Channel G Control Parameter 9
0x5E36	XTC_3C_CTRL_0694	–	RW	Gr2 Channel G Control Parameter 10
0x5E37	XTC_3C_CTRL_0695	–	RW	Gr2 Channel G Control Parameter 11
0x5E38	XTC_3C_CTRL_0696	–	RW	Gr2 Channel G Control Parameter 12
0x5E39	XTC_3C_CTRL_0697	–	RW	Gr2 Channel G Control Parameter 13
0x5E3A	XTC_3C_CTRL_0698	–	RW	Gr2 Channel G Control Parameter 14
0x5E3B	XTC_3C_CTRL_0699	–	RW	Gr2 Channel G Control Parameter 15

table 6-64 XTC_3C registers (sheet 25 of 30)

address	register name	default value	R/W	description
0x5E3C	XTC_3C_CTRL_0700	–	RW	Gr2 Channel G Control Parameter 16
0x5E3D	XTC_3C_CTRL_0701	–	RW	Gr2 Channel G Control Parameter 17
0x5E3E	XTC_3C_CTRL_0702	–	RW	Gr2 Channel G Control Parameter 18
0x5E3F	XTC_3C_CTRL_0703	–	RW	Gr2 Channel G Control Parameter 19
0x5E40	XTC_3C_CTRL_0704	–	RW	Gr2 Channel G Control Parameter 20
0x5E41	XTC_3C_CTRL_0705	–	RW	Gr2 Channel G Control Parameter 21
0x5E42	XTC_3C_CTRL_0706	–	RW	Gr2 Channel G Control Parameter 22
0x5E43	XTC_3C_CTRL_0707	–	RW	Gr2 Channel G Control Parameter 23
0x5E44	XTC_3C_CTRL_0708	–	RW	Gr2 Channel G Control Parameter 24
0x5E45	XTC_3C_CTRL_0709	–	RW	Gr2 Channel G Control Parameter 25
0x5E46	XTC_3C_CTRL_0710	–	RW	Gr2 Channel G Control Parameter 26
0x5E47	XTC_3C_CTRL_0711	–	RW	Gr2 Channel G Control Parameter 27
0x5E48	XTC_3C_CTRL_0712	–	RW	Gr2 Channel G Control Parameter 28
0x5E49	XTC_3C_CTRL_0713	–	RW	Gr2 Channel G Control Parameter 29
0x5E4A	XTC_3C_CTRL_0714	–	RW	Gr2 Channel G Control Parameter 30
0x5E4B	XTC_3C_CTRL_0715	–	RW	Gr2 Channel G Control Parameter 31
0x5E4C	XTC_3C_CTRL_0716	–	RW	Gr2 Channel G Control Parameter 32
0x5E4D	XTC_3C_CTRL_0717	–	RW	Gr2 Channel G Control Parameter 33
0x5E4E	XTC_3C_CTRL_0718	–	RW	Gr2 Channel G Control Parameter 34
0x5E4F	XTC_3C_CTRL_0719	–	RW	Gr2 Channel G Control Parameter 35
0x5E50	XTC_3C_CTRL_0720	–	RW	Gr2 Channel R Control Parameter 0
0x5E51	XTC_3C_CTRL_0721	–	RW	Gr2 Channel R Control Parameter 1
0x5E52	XTC_3C_CTRL_0722	–	RW	Gr2 Channel R Control Parameter 2
0x5E53	XTC_3C_CTRL_0723	–	RW	Gr2 Channel R Control Parameter 3
0x5E54	XTC_3C_CTRL_0724	–	RW	Gr2 Channel R Control Parameter 4
0x5E55	XTC_3C_CTRL_0725	–	RW	Gr2 Channel R Control Parameter 5
0x5E56	XTC_3C_CTRL_0726	–	RW	Gr2 Channel R Control Parameter 6
0x5E57	XTC_3C_CTRL_0727	–	RW	Gr2 Channel R Control Parameter 7
0x5E58	XTC_3C_CTRL_0728	–	RW	Gr2 Channel R Control Parameter 8
0x5E59	XTC_3C_CTRL_0729	–	RW	Gr2 Channel R Control Parameter 9

table 6-64 XTC_3C registers (sheet 26 of 30)

address	register name	default value	R/W	description
0x5E5A	XTC_3C_CTRL_0730	–	RW	Gr2 Channel R Control Parameter 10
0x5E5B	XTC_3C_CTRL_0731	–	RW	Gr2 Channel R Control Parameter 11
0x5E5C	XTC_3C_CTRL_0732	–	RW	Gr2 Channel R Control Parameter 12
0x5E5D	XTC_3C_CTRL_0733	–	RW	Gr2 Channel R Control Parameter 13
0x5E5E	XTC_3C_CTRL_0734	–	RW	Gr2 Channel R Control Parameter 14
0x5E5F	XTC_3C_CTRL_0735	–	RW	Gr2 Channel R Control Parameter 15
0x5E60	XTC_3C_CTRL_0736	–	RW	Gr2 Channel R Control Parameter 16
0x5E61	XTC_3C_CTRL_0737	–	RW	Gr2 Channel R Control Parameter 17
0x5E62	XTC_3C_CTRL_0738	–	RW	Gr2 Channel R Control Parameter 18
0x5E63	XTC_3C_CTRL_0739	–	RW	Gr2 Channel R Control Parameter 19
0x5E64	XTC_3C_CTRL_0740	–	RW	Gr2 Channel R Control Parameter 20
0x5E65	XTC_3C_CTRL_0741	–	RW	Gr2 Channel R Control Parameter 21
0x5E66	XTC_3C_CTRL_0742	–	RW	Gr2 Channel R Control Parameter 22
0x5E67	XTC_3C_CTRL_0743	–	RW	Gr2 Channel R Control Parameter 23
0x5E68	XTC_3C_CTRL_0744	–	RW	Gr2 Channel R Control Parameter 24
0x5E69	XTC_3C_CTRL_0745	–	RW	Gr2 Channel R Control Parameter 25
0x5E6A	XTC_3C_CTRL_0746	–	RW	Gr2 Channel R Control Parameter 26
0x5E6B	XTC_3C_CTRL_0747	–	RW	Gr2 Channel R Control Parameter 27
0x5E6C	XTC_3C_CTRL_0748	–	RW	Gr2 Channel R Control Parameter 28
0x5E6D	XTC_3C_CTRL_0749	–	RW	Gr2 Channel R Control Parameter 29
0x5E6E	XTC_3C_CTRL_0750	–	RW	Gr2 Channel R Control Parameter 30
0x5E6F	XTC_3C_CTRL_0751	–	RW	Gr2 Channel R Control Parameter 31
0x5E70	XTC_3C_CTRL_0752	–	RW	Gr2 Channel R Control Parameter 32
0x5E71	XTC_3C_CTRL_0753	–	RW	Gr2 Channel R Control Parameter 33
0x5E72	XTC_3C_CTRL_0754	–	RW	Gr2 Channel R Control Parameter 34
0x5E73	XTC_3C_CTRL_0755	–	RW	Gr2 Channel R Control Parameter 35
0x5E74	XTC_3C_CTRL_0756	–	RW	Gr3 Channel B Control Parameter 0
0x5E75	XTC_3C_CTRL_0757	–	RW	Gr3 Channel B Control Parameter 1
0x5E76	XTC_3C_CTRL_0758	–	RW	Gr3 Channel B Control Parameter 2
0x5E77	XTC_3C_CTRL_0759	–	RW	Gr3 Channel B Control Parameter 3

table 6-64 XTC_3C registers (sheet 27 of 30)

address	register name	default value	R/W	description
0x5E78	XTC_3C_CTRL_0760	–	RW	Gr3 Channel B Control Parameter 4
0x5E79	XTC_3C_CTRL_0761	–	RW	Gr3 Channel B Control Parameter 5
0x5E7A	XTC_3C_CTRL_0762	–	RW	Gr3 Channel B Control Parameter 6
0x5E7B	XTC_3C_CTRL_0763	–	RW	Gr3 Channel B Control Parameter 7
0x5E7C	XTC_3C_CTRL_0764	–	RW	Gr3 Channel B Control Parameter 8
0x5E7D	XTC_3C_CTRL_0765	–	RW	Gr3 Channel B Control Parameter 9
0x5E7E	XTC_3C_CTRL_0766	–	RW	Gr3 Channel B Control Parameter 10
0x5E7F	XTC_3C_CTRL_0767	–	RW	Gr3 Channel B Control Parameter 11
0x5E80	XTC_3C_CTRL_0768	–	RW	Gr3 Channel B Control Parameter 12
0x5E81	XTC_3C_CTRL_0769	–	RW	Gr3 Channel B Control Parameter 13
0x5E82	XTC_3C_CTRL_0770	–	RW	Gr3 Channel B Control Parameter 14
0x5E83	XTC_3C_CTRL_0771	–	RW	Gr3 Channel B Control Parameter 15
0x5E84	XTC_3C_CTRL_0772	–	RW	Gr3 Channel B Control Parameter 16
0x5E85	XTC_3C_CTRL_0773	–	RW	Gr3 Channel B Control Parameter 17
0x5E86	XTC_3C_CTRL_0774	–	RW	Gr3 Channel B Control Parameter 18
0x5E87	XTC_3C_CTRL_0775	–	RW	Gr3 Channel B Control Parameter 19
0x5E88	XTC_3C_CTRL_0776	–	RW	Gr3 Channel B Control Parameter 20
0x5E89	XTC_3C_CTRL_0777	–	RW	Gr3 Channel B Control Parameter 21
0x5E8A	XTC_3C_CTRL_0778	–	RW	Gr3 Channel B Control Parameter 22
0x5E8B	XTC_3C_CTRL_0779	–	RW	Gr3 Channel B Control Parameter 23
0x5E8C	XTC_3C_CTRL_0780	–	RW	Gr3 Channel B Control Parameter 24
0x5E8D	XTC_3C_CTRL_0781	–	RW	Gr3 Channel B Control Parameter 25
0x5E8E	XTC_3C_CTRL_0782	–	RW	Gr3 Channel B Control Parameter 26
0x5E8F	XTC_3C_CTRL_0783	–	RW	Gr3 Channel B Control Parameter 27
0x5E90	XTC_3C_CTRL_0784	–	RW	Gr3 Channel B Control Parameter 28
0x5E91	XTC_3C_CTRL_0785	–	RW	Gr3 Channel B Control Parameter 29
0x5E92	XTC_3C_CTRL_0786	–	RW	Gr3 Channel B Control Parameter 30
0x5E93	XTC_3C_CTRL_0787	–	RW	Gr3 Channel B Control Parameter 31
0x5E94	XTC_3C_CTRL_078	–	RW	Gr3 Channel B Control Parameter 32
0x5E95	XTC_3C_CTRL_0789	–	RW	Gr3 Channel B Control Parameter 33

table 6-64 XTC_3C registers (sheet 28 of 30)

address	register name	default value	R/W	description
0x5E96	XTC_3C_CTRL_0790	–	RW	Gr3 Channel B Control Parameter 34
0x5E97	XTC_3C_CTRL_0791	–	RW	Gr3 Channel B Control Parameter 35
0x5E98	XTC_3C_CTRL_0792	–	RW	Gr3 Channel G Control Parameter 0
0x5E99	XTC_3C_CTRL_0793	–	RW	Gr3 Channel G Control Parameter 1
0x5E9A	XTC_3C_CTRL_0794	–	RW	Gr3 Channel G Control Parameter 2
0x5E9B	XTC_3C_CTRL_0795	–	RW	Gr3 Channel G Control Parameter 3
0x5E9C	XTC_3C_CTRL_0796	–	RW	Gr3 Channel G Control Parameter 4
0x5E9D	XTC_3C_CTRL_0797	–	RW	Gr3 Channel G Control Parameter 5
0x5E9E	XTC_3C_CTRL_0798	–	RW	Gr3 Channel G Control Parameter 6
0x5E9F	XTC_3C_CTRL_0799	–	RW	Gr3 Channel G Control Parameter 7
0x5EA0	XTC_3C_CTRL_0800	–	RW	Gr3 Channel G Control Parameter 8
0x5EA1	XTC_3C_CTRL_0801	–	RW	Gr3 Channel G Control Parameter 9
0x5EA2	XTC_3C_CTRL_0802	–	RW	Gr3 Channel G Control Parameter 10
0x5EA3	XTC_3C_CTRL_0803	–	RW	Gr3 Channel G Control Parameter 11
0x5EA4	XTC_3C_CTRL_0804	–	RW	Gr3 Channel G Control Parameter 12
0x5EA5	XTC_3C_CTRL_0805	–	RW	Gr3 Channel G Control Parameter 13
0x5EA6	XTC_3C_CTRL_0806	–	RW	Gr3 Channel G Control Parameter 14
0x5EA7	XTC_3C_CTRL_0807	–	RW	Gr3 Channel G Control Parameter 15
0x5EA8	XTC_3C_CTRL_0808	–	RW	Gr3 Channel G Control Parameter 16
0x5EA9	XTC_3C_CTRL_0809	–	RW	Gr3 Channel G Control Parameter 17
0x5EAA	XTC_3C_CTRL_0810	–	RW	Gr3 Channel G Control Parameter 18
0x5EAB	XTC_3C_CTRL_0811	–	RW	Gr3 Channel G Control Parameter 19
0x5EAC	XTC_3C_CTRL_0812	–	RW	Gr3 Channel G Control Parameter 20
0x5EAD	XTC_3C_CTRL_0813	–	RW	Gr3 Channel G Control Parameter 21
0x5EAE	XTC_3C_CTRL_0814	–	RW	Gr3 Channel G Control Parameter 22
0x5EAF	XTC_3C_CTRL_0815	–	RW	Gr3 Channel G Control Parameter 23
0x5EB0	XTC_3C_CTRL_0816	–	RW	Gr3 Channel G Control Parameter 24
0x5EB1	XTC_3C_CTRL_0817	–	RW	Gr3 Channel G Control Parameter 25
0x5EB2	XTC_3C_CTRL_0818	–	RW	Gr3 Channel G Control Parameter 26
0x5EB3	XTC_3C_CTRL_0819	–	RW	Gr3 Channel G Control Parameter 27

table 6-64 XTC_3C registers (sheet 29 of 30)

address	register name	default value	R/W	description
0x5EB4	XTC_3C_CTRL_0820	–	RW	Gr3 Channel G Control Parameter 28
0x5EB5	XTC_3C_CTRL_0821	–	RW	Gr3 Channel G Control Parameter 29
0x5EB6	XTC_3C_CTRL_0822	–	RW	Gr3 Channel G Control Parameter 30
0x5EB7	XTC_3C_CTRL_0823	–	RW	Gr3 Channel G Control Parameter 31
0x5EB8	XTC_3C_CTRL_0824	–	RW	Gr3 Channel G Control Parameter 32
0x5EB9	XTC_3C_CTRL_0825	–	RW	Gr3 Channel G Control Parameter 33
0x5EBA	XTC_3C_CTRL_0826	–	RW	Gr3 Channel G Control Parameter 34
0x5EBB	XTC_3C_CTRL_0827	–	RW	Gr3 Channel G Control Parameter 35
0x5EBC	XTC_3C_CTRL_0828	–	RW	Gr3 Channel R Control Parameter 0
0x5EBD	XTC_3C_CTRL_0829	–	RW	Gr3 Channel R Control Parameter 1
0x5EBE	XTC_3C_CTRL_0830	–	RW	Gr3 Channel R Control Parameter 2
0x5EBF	XTC_3C_CTRL_0831	–	RW	Gr3 Channel R Control Parameter 3
0x5EC0	XTC_3C_CTRL_0832	–	RW	Gr3 Channel R Control Parameter 4
0x5EC1	XTC_3C_CTRL_0833	–	RW	Gr3 Channel R Control Parameter 5
0x5EC2	XTC_3C_CTRL_0834	–	RW	Gr3 Channel R Control Parameter 6
0x5EC3	XTC_3C_CTRL_0835	–	RW	Gr3 Channel R Control Parameter 7
0x5EC4	XTC_3C_CTRL_0836	–	RW	Gr3 Channel R Control Parameter 8
0x5EC5	XTC_3C_CTRL_0837	–	RW	Gr3 Channel R Control Parameter 9
0x5EC6	XTC_3C_CTRL_0838	–	RW	Gr3 Channel R Control Parameter 10
0x5EC7	XTC_3C_CTRL_0839	–	RW	Gr3 Channel R Control Parameter 11
0x5EC8	XTC_3C_CTRL_0840	–	RW	Gr3 Channel R Control Parameter 12
0x5EC9	XTC_3C_CTRL_0841	–	RW	Gr3 Channel R Control Parameter 13
0x5ECA	XTC_3C_CTRL_0842	–	RW	Gr3 Channel R Control Parameter 14
0x5ECB	XTC_3C_CTRL_0843	–	RW	Gr3 Channel R Control Parameter 15
0x5ECC	XTC_3C_CTRL_0844	–	RW	Gr3 Channel R Control Parameter 16
0x5ECD	XTC_3C_CTRL_0845	–	RW	Gr3 Channel R Control Parameter 17
0x5ECE	XTC_3C_CTRL_0846	–	RW	Gr3 Channel R Control Parameter 18
0x5ECF	XTC_3C_CTRL_0847	–	RW	Gr3 Channel R Control Parameter 19
0x5ED0	XTC_3C_CTRL_0848	–	RW	Gr3 Channel R Control Parameter 20
0x5ED1	XTC_3C_CTRL_0849	–	RW	Gr3 Channel R Control Parameter 21

table 6-64 XTC_3C registers (sheet 30 of 30)

address	register name	default value	R/W	description
0x5ED2	XTC_3C_CTRL_0850	–	RW	Gr3 Channel R Control Parameter 22
0x5ED3	XTC_3C_CTRL_0851	–	RW	Gr3 Channel R Control Parameter 23
0x5ED4	XTC_3C_CTRL_0852	–	RW	Gr3 Channel R Control Parameter 24
0x5ED5	XTC_3C_CTRL_0853	–	RW	Gr3 Channel R Control Parameter 25
0x5ED6	XTC_3C_CTRL_0854	–	RW	Gr3 Channel R Control Parameter 26
0x5ED7	XTC_3C_CTRL_0855	–	RW	Gr3 Channel R Control Parameter 27
0x5ED8	XTC_3C_CTRL_0856	–	RW	Gr3 Channel R Control Parameter 28
0x5ED9	XTC_3C_CTRL_0857	–	RW	Gr3 Channel R Control Parameter 29
0x5EDA	XTC_3C_CTRL_0858	–	RW	Gr3 Channel R Control Parameter 30
0x5EDB	XTC_3C_CTRL_0859	–	RW	Gr3 Channel R Control Parameter 31
0x5EDC	XTC_3C_CTRL_0860	–	RW	Gr3 Channel R Control Parameter 32
0x5EDD	XTC_3C_CTRL_0861	–	RW	Gr3 Channel R Control Parameter 33
0x5EDE	XTC_3C_CTRL_0862	–	RW	Gr3 Channel R Control Parameter 34
0x5EDF	XTC_3C_CTRL_0863	–	RW	Gr3 Channel R Control Parameter 35

6.65 PDF_33 [0x5F00 - 0x5F43]

table 6-65 PDF_33 registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5F00	PDF_3345_D2V2_TOP_0	0x21	RW	Bit[7:6]: Not used Bit[5]: Enable PD correction or not Range is [0:1] Bit[4]: Enable single defect pixel removal Range is [0:1] Bit[3]: single_detect_4c_enable Range is [0:1] Bit[2]: Use corner information enable Range is [0:1] Bit[1]: Use chromatic information enable Range is [0:1] Bit[0]: Is ML 2x2 pattern or not Range is [0:1]

table 6-65 PDF_33 registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5F01	PDF_3345_D2V2_TOP_1	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Weight C Range is [0:16]
0x5F02	PDF_3345_D2V2_TOP_2	0x04	RW	Bit[7:3]: Not used Bit[2:1]: Direction based method PD correction method enable Range is [0:2] Bit[0]: m_bPDDebugMode_ Range is [0:1]
0x5F03	PDF_3345_D2V2_TOP_3	0x05	RW	Bit[7:6]: Not used Bit[5:4]: G diag option Range is [0:3] Bit[3]: Single defect pixel removal option Range is [0:1] Bit[2:0]: Single defect pixel removal shift bit Range is [0:7]
0x5F04	PDF_3345_D2V2_TOP_4	0x20	RW	Bit[7:0]: Single defect pixel threshold Range is [0:255]
0x5F05	PDF_3345_D2V2_TOP_5	0x19	RW	Bit[7:6]: m_ nDirWeightScaleBit Range is [0:3] Bit[5:4]: m_nDirWeightCurveNum Range is [0:3] Bit[3:2]: m_nBilWeightScaleBit Range is [0:3] Bit[1:0]: m_nBilWeightCurveNum Range is [0:3]
0x5F06	PDF_3345_D2V2_TOP_6	0x10	RW	Bit[7:6]: Not used Bit[5:0]: PD X cycle Range is [1:64]
0x5F07	PDF_3345_D2V2_TOP_7	0x20	RW	Bit[7:6]: Not used Bit[5:0]: PD Y cycle Range is [1:64]
0x5F08	PDF_3345_D2V2_TOP_8	0x04	RW	Bit[7:5]: Not used Bit[4:0]: PD X1 start Range is [0:31]
0x5F09	PDF_3345_D2V2_TOP_9	0x04	RW	Bit[7:5]: Not used Bit[4:0]: PD X2 start Range is [0:31]
0x5F0A	PDF_3345_D2V2_TOP_A	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: PD X3 start Range is [0:31]

table 6-65 PDF_33 registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5F0B	PDF_3345_D2V2_TOP_B	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: PD X4 start Range is [0:31]
0x5F0C	PDF_3345_D2V2_TOP_C	0x04	RW	Bit[7:5]: Not used Bit[4:0]: PD Y1 start Range is [0:31]
0x5F0D	PDF_3345_D2V2_TOP_D	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: PD Y2 start Range is [0:31]
0x5F0E	PDF_3345_D2V2_TOP_E	0x14	RW	Bit[7:5]: Not used Bit[4:0]: PD Y3 start Range is [0:31]
0x5F0F	PDF_3345_D2V2_TOP_F	0x1C	RW	Bit[7:5]: Not used Bit[4:0]: PD Y4 start Range is [0:31]
0x5F10	PDF_3345_D2V2_TOP_10	0x01	RW	Bit[7:5]: Not used Bit[4:0]: PD X skip Range is [0:31]
0x5F11	PDF_3345_D2V2_TOP_11	0x01	RW	Bit[7:5]: Not used Bit[4:0]: PD Y skip Range is [0:31]
0x5F12	PDF_3345_D2V2_TOP_12	0x00	RW	Bit[7:0]: 1x noise level for PD correction Range is [0:255]
0x5F13	PDF_3345_D2V2_TOP_13	0x00	RW	Bit[7:0]: 4x noise level for PD correction Range is [0:255]
0x5F14	PDF_3345_D2V2_TOP_14	0x00	RW	Bit[7:0]: 8x noise level for PD correction Range is [0:255]
0x5F15	PDF_3345_D2V2_TOP_15	0xAA	RW	Bit[7:6]: PD ch 1 Range is [0:3] Bit[5:4]: PD ch 2 Range is [0:3] Bit[3:2]: PD ch 3 Range is [0:3] Bit[1:0]: PD ch 4 Range is [0:3]
0x5F16	PDF_3345_D2V2_TOP_16	0x00	RW	Bit[7:0]: Flat threshold Range is [0:255]
0x5F17	PDF_3345_D2V2_TOP_17	0x00	RW	Bit[7:0]: Inte threshold Range is [0:255]

table 6-65 PDF_33 registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x5F18	PDF_3345_D2V2_TOP_18	0x24	RW	Bit[7:6]: Not used Bit[5:0]: Image width[13:8] Range is [0:16383]
0x5F19	PDF_3345_D2V2_TOP_19	0x40	RW	Bit[7:0]: Image width[7:0] Range is [0:16383]
0x5F1A	PDF_3345_D2V2_TOP_1A	0x1B	RW	Bit[7:5]: Not used Bit[4:0]: Image height[12:8] Range is [0:8191]
0x5F1B	PDF_3345_D2V2_TOP_1B	0x40	RW	Bit[7:0]: Image height[7:0] Range is [0:8191]
0x5F1C	PDF_3345_D2V2_TOP_1C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Window start X[13:8] Range is [0:16383]
0x5F1D	PDF_3345_D2V2_TOP_1D	0x20	RW	Bit[7:0]: Window start X[7:0] Range is [0:16383]
0x5F1E	PDF_3345_D2V2_TOP_1E	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Window start Y[12:8] Range is [0:8191]
0x5F1F	PDF_3345_D2V2_TOP_1F	0x20	RW	Bit[7:0]: Window start Y[7:0] Range is [0:8191]
0x5F20	PDF_3345_D2V2_TOP_20	0x24	RW	Bit[7:6]: Not used Bit[5:0]: Window width[13:8] Range is [0:16383]
0x5F21	PDF_3345_D2V2_TOP_21	0x00	RW	Bit[7:0]: Window width[7:0] Range is [0:16383]
0x5F22	PDF_3345_D2V2_TOP_22	0x1B	RW	Bit[7:5]: Not used Bit[4:0]: Window height[12:8] Range is [0:8191]
0x5F23	PDF_3345_D2V2_TOP_23	0x00	RW	Bit[7:0]: Window height[7:0] Range is [0:8191]
0x5F24	PDF_3345_D2V2_TOP_24	0x00	RW	Bit[7:4]: Not used Bit[3]: vcnt_out_en Bit[2]: hcnt_out_en Bit[1]: fix_ptn_mode Bit[0]: fix_ptn_en

table 6-65 PDF_33 registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5F25	PDF_3345_D2V2_TOP_25	0x08	RW	Bit[7]: Not used Bit[6]: r_lowpower_gate_dis_2 Bit[5]: r_lowpower_gate_dis_1 Bit[4]: r_lowpower_gate_dis_0 Bit[3]: pd_cnt_clr_man_en Bit[2]: pd_win_man_en Bit[1]: xoffset_man_en Bit[0]: yoffset_man_en
0x5F26	PDF_3345_D2V2_TOP_26	0x00	RW	Bit[7:0]: r_gate_dis[7:0]
0x5F27	PDF_3345_D2V2_TOP_27	0x00	RW	Bit[7:0]: r_gate_dis[15:8]
0x5F28	PDF_3345_D2V2_TOP_28	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Xoffset[13:8] Range is [0:16383]
0x5F29	PDF_3345_D2V2_TOP_29	0x00	RW	Bit[7:0]: Xoffset[7:0] Range is [0:16383]
0x5F2A	PDF_3345_D2V2_TOP_2A	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Yoffset[12:8] Range is [0:8191]
0x5F2B	PDF_3345_D2V2_TOP_2B	0x00	RW	Bit[7:0]: Yoffset[7:0] Range is [0:8191]
0x5F2C	PDF_3345_D2V2_TOP_2C	0x08	RW	Bit[7:5]: Not used Bit[4:0]: result_combine_weight Range is [0:16]
0x5F2D	PDF_3345_D2V2_TOP_2D	0x40	RW	Bit[7:0]: pddpc_white_thre Range is [0:255]
0x5F2E	PDF_3345_D2V2_TOP_2E	0x40	RW	Bit[7:0]: pddpc_black_thre Range is [0:255]
0x5F2F	PDF_3345_D2V2_TOP_2F	0x27	RW	Bit[7:0]: ba_threshold Range is [0:255]
0x5F30	PDF_3345_D2V2_TOP_30	0x0D	RW	Bit[7:6]: Not used Bit[5:4]: r_2x1pd Range is [0:2] Bit[3]: r_2x1simple Range is [0:1] Bit[2:1]: fine_tune Range is [0:3] Bit[0]: clip_maxmin Range is [0:1]

table 6-65 PDF_33 registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x5F31	PDF_3345_D2V2_TOP_31	0x3C	RW	Bit[7:6]: Not used Bit[5]: Improveb4 Range is [0:1] Bit[4]: smart_selection Range is [0:1] Bit[3]: if_addhf Range is [0:1] Bit[2:0]: throw_num Range is [0:6]
0x5F32	PDF_3345_D2V2_TOP_32	0x20	RW	Bit[7:0]: improve_lowthre Range is [0:255]
0x5F33	PDF_3345_D2V2_TOP_33	0x10	RW	Bit[7:0]: improve_highthre Range is [0:255]
0x5F34	PDF_3345_D2V2_TOP_34	0x20	RW	Bit[7:0]: improve_lowratio Range is [0:255]
0x5F35	PDF_3345_D2V2_TOP_35	0x10	RW	Bit[7:0]: improve_highratio Range is [0:255]
0x5F36	PDF_3345_D2V2_TOP_36	0x20	RW	Bit[7:0]: hfratio_bhv Range is [0:255]
0x5F37	PDF_3345_D2V2_TOP_37	0x20	RW	Bit[7:0]: hfratio_bdiag Range is [0:255]
0x5F38	PDF_3345_D2V2_TOP_38	0x20	RW	Bit[7:0]: hfratio_r Range is [0:255]
0x5F39	PDF_3345_D2V2_TOP_39	0x20	RW	Bit[7:0]: hfratio_g Range is [0:255]
0x5F3A	PDF_3345_D2V2_TOP_3A	0x20	RW	Bit[7:0]: hfratio_gdiag Range is [0:255]
0x5F3B	PDF_3345_D2V2_TOP_3B	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Xoffset1[13:8] Range is [0:16383]
0x5F3C~ 0x5F3E	NOT USED	–	–	Not Used
0x5F3F	PDF_3345_D2V2_TOP_3F	0x00	RW	Bit[7:0]: Xoffset1[7:0] Range is [0:16383]
0x5F40~ 0x5F41	NOT USED	–	–	Not Used
0x5F42	PDF_3345_D2V2_TOP_42	–	R	Bit[7:0]: Version[15:8]
0x5F43	PDF_3345_D2V2_TOP_43	–	R	Bit[7:0]: Version[7:0]

6.66 PDC_FD_LIST [0x5F80 - 0x651F]

table 6-66 PDC_FD_LIST registers

address	register name	default value	R/W	description
0x5F80	PDC_FDLIST_0	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[0][0]
0x5F81	PDC_FDLIST_1	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[0][1]
0x5F82	PDC_FDLIST_2	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[0][2]
0x5F83	PDC_FDLIST_3	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[0][3]
0x5F84	PDC_FDLIST_4	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[0][4]
0x5F85	PDC_FDLIST_5	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[0][5]
0x5F86	PDC_FDLIST_6	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[0][6]
0x5F87	PDC_FDLIST_7	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[0][7]
0x5F88	PDC_FDLIST_8	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[0][8]
0x5F89~ 0x651F	PDC_FDLIST_9~ PDC_FDLIST_59F	0x00	RW	Bit[7:0]: m_pPDFadinglist_opt[1][0]~ m_pPDFadinglist_opt[159][8]

6.67 DPD [0x6520 - 0x652F]

table 6-67 DPD registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x6520	DPD_1225_TOP_0	0x10	RW	Bit[7]: Not used Bit[6:0]: Coefficient of B Range is [0:64]
0x6521	DPD_1225_TOP_1	0x10	RW	Bit[7]: Not used Bit[6:0]: Coefficient of Gb Range is [0:64]
0x6522	DPD_1225_TOP_2	0x10	RW	Bit[7]: Not used Bit[6:0]: Coefficient of Gr Range is [0:64]
0x6523	DPD_1225_TOP_3	0x10	RW	Bit[7]: Not used Bit[6:0]: Coefficient of R Range is [0:64]

table 6-67 DPD registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x6524	DPD_1225_TOP_4	0x00	RW	Bit[7]: Not used Bit[6:5]: Output select 00: Output Y 01: Output G 10: Output all 11: Not defined Bit[4]: Enable saturation process Bit[3]: Bin method Bit[2]: Enable swap option Bit[1:0]: Select L/M/S to do DPD
0x6525	DPD_1225_TOP_5	0x00	RW	Bit[7:5]: Enable V skip 4 001: Choose first 010: Choose second 011: Choose third 100: Choose fourth Others: Not defined Bit[4:3]: Enable V skip 2 00: Not defined 01: Choose first 10: Choose second 11: Not defined Bit[2:1]: Enable H skip 2 00: Not defined 01: Choose first 10: Choose second 11: Not defined Bit[0]: Enable YVbin Range is [0:1]
0x6526	DPD_1225_TOP_6	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Saturation threshold[9:8]
0x6527	DPD_1225_TOP_7	0xFF	RW	Bit[7:0]: Saturation threshold[7:0]
0x6528	NOT USED	–	–	Not Used
0x6529	DPD_1225_TOP_9	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Saturation value[9:8]
0x652A	DPD_1225_TOP_A	0xFF	RW	Bit[7:0]: Saturation value[7:0]
0x652B	RSVD	–	–	Reserved
0x652C~ 0x652D	NOT USED	–	–	Not Used
0x652E	DPD_1225_TOP_E	–	R	Bit[7:0]: Version[15:8]
0x652F	DPD_1225_TOP_F	–	R	Bit[7:0]: Version[7:0]

7 operating specifications

7.1 absolute maximum ratings

table 7-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	3V
	V_{DD-IO}	4.5V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 functional temperature

table 7-2 functional temperature

parameter	range
operating temperature (for applications up to 15 fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

7.3 DC characteristics

note Power consumption shown are target values. These values are subject to change based on real measurements.

table 7-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.7	2.8	2.9	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	1.9	V
V_{DD-D}	supply voltage (digital core)	1.05	1.10	1.18	V
I_{DD-A}	active (operating) current[a]		66	80	mA
I_{DD-IO}			0.3	1	mA
I_{DD-D}			420	600	mA
$I_{DDS-XSHUTDOWN}$	XSHUTDOWN current[b]		10		µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.10V, DOVDD = 1.8V, EVDD = 1.10V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.62			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}	SCL and SDA	-0.5	0	0.54	V
V_{IH}	SCL and SDA	1.28	1.8	3.0	V

a. power consumption is RMS value measured under typical conditions, full resolution, full speed with ISP function on; for high speed mode, AVDD may go up to 104 mA as typical and 128 mA as maximum; please contact FAE for detailed power consumption data under different modes

b. XSHUTDOWN current is measured at room temperature

7.4 timing characteristics

figure 7-1 reference clock input timing diagram

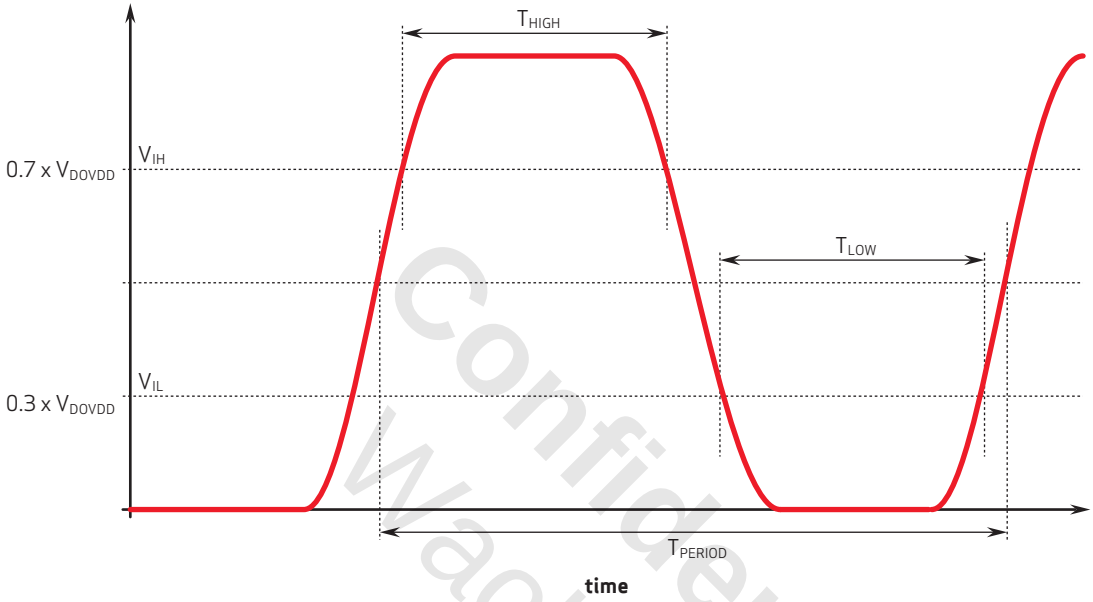


table 7-4 timing characteristics

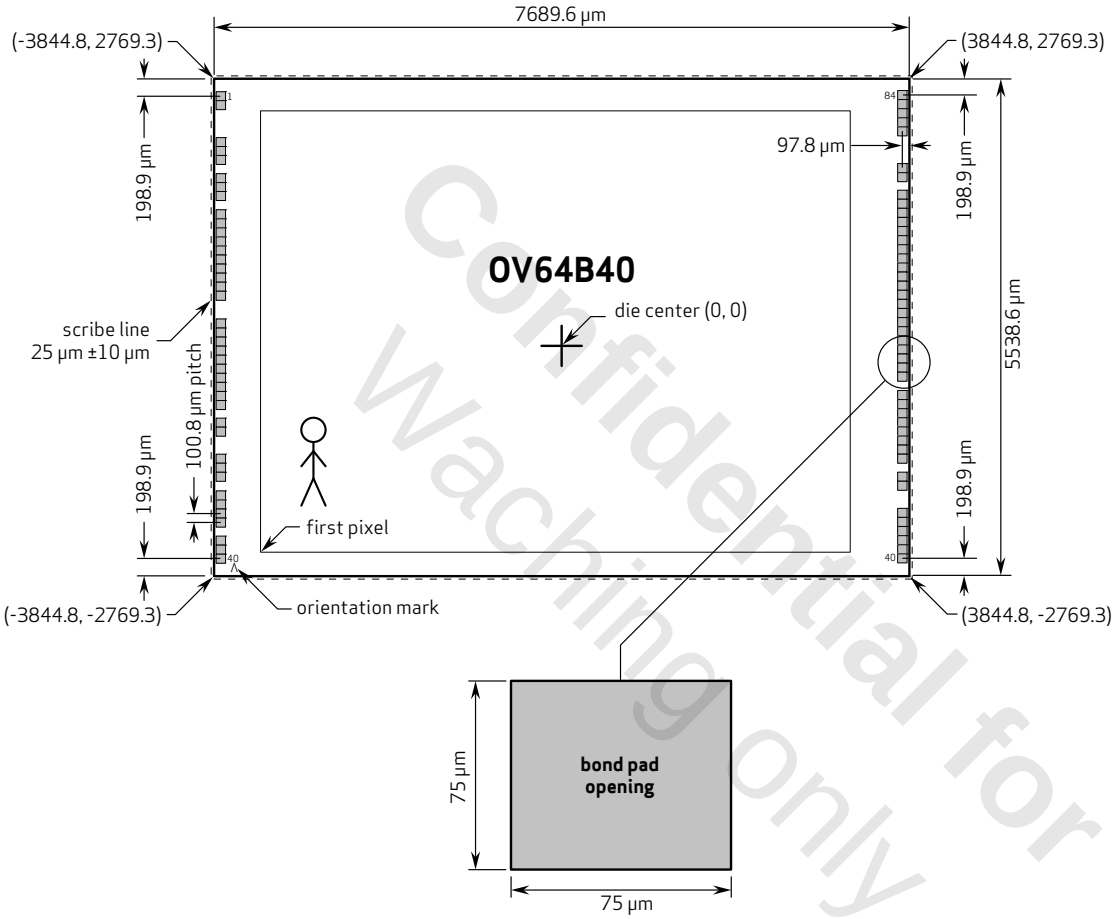
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{XVCLK}	frequency (XVCLK)[a]	6	24	27	MHz
T_{PERIOD}	period (XVCLK)	37.0	41.7	166.7	ns
T_{LOW}	low level width (XVCLK)	$0.35 \times T_{PERIOD}$		$0.65 \times T_{PERIOD}$	ns
T_{HIGH}	high level width (XVCLK)	$0.35 \times T_{PERIOD}$		$0.65 \times T_{PERIOD}$	ns

a. for input clock range 6~27 MHz, OV64B40 can tolerate input clock period jitter up to 600 ps peak-to-peak

8 mechanical specifications

8.1 COB physical specifications

figure 8-1 COB die specifications



note all dimensions and coordinates are in microns unless otherwise specified

table 8-1 pad location coordinates (sheet 1 of 3)

pad number	pad name	x coordinate	y coordinate	bond pad opening size
1	AGND	-3747	2570.4	75x75
2	AVDD	-3747	2469.6	75x75
3	DOVDD	-3747	2066.4	75x75
4	DVDD	-3747	1965.6	75x75
5	DOGND	-3747	1864.8	75x75
6	NC	-3747	1663.2	75x75
7	DOGND	-3747	1562.4	75x75
8	DVDD	-3747	1461.6	75x75
9	EVDD	-3747	1260.0	75x75
10	EGND	-3747	1159.2	75x75
11	MDP2	-3747	1058.4	75x75
12	MDN2/MC0A	-3747	957.6	75x75
13	MDP0/MC0B	-3747	856.8	75x75
14	MDN0/MC0C	-3747	756.0	75x75
15	DOGND	-3747	655.2	75x75
16	DVDD	-3747	554.4	75x75
17	EVDD	-3747	453.6	75x75
18	EGND	-3747	352.8	75x75
19	MCP/MC1A	-3747	50.4	75x75
20	MCN/MC1B	-3747	-50.4	75x75
21	MDP1/MC1C	-3747	-151.2	75x75
22	MDN1/MC2A	-3747	-252.0	75x75
23	MDP3/MC2B	-3747	-352.8	75x75
24	MDN3/MC2C	-3747	-453.6	75x75
25	EGND	-3747	-554.4	75x75
26	EVDD	-3747	-655.2	75x75
27	DVDD	-3747	-756.0	75x75
28	DOGND	-3747	-856.8	75x75
29	DOGND	-3747	-1058.4	75x75
30	AVDD	-3747	-1159.2	75x75

table 8-1 pad location coordinates (sheet 2 of 3)

pad number	pad name	x coordinate	y coordinate	bond pad opening size
31	DVDD	-3747	-1461.6	75x75
32	DOGND	-3747	-1562.4	75x75
33	NC	-3747	-1663.2	75x75
34	DOGND	-3747	-1864.8	75x75
35	DVDD	-3747	-1965.6	75x75
36	DOGND	-3747	-2066.4	75x75
37	XVCLK	-3747	-2167.2	75x75
38	DOVDD	-3747	-2368.8	75x75
39	AVDD	-3747	-2469.6	75x75
40	AGND	-3747	-2570.4	75x75
41	AGND	3747	-2570.4	75x75
42	AVDD	3747	-2469.6	75x75
43	DOGND	3747	-2368.8	75x75
44	SCL	3747	-2268.0	75x75
45	SDA	3747	-2167.2	75x75
46	DOVDD	3747	-2066.4	75x75
47	DVDD	3747	-1764.0	75x75
48	DOGND	3747	-1663.2	75x75
49	DVDD	3747	-1461.6	75x75
50	DOGND	3747	-1360.8	75x75
51	NC	3747	-1260.0	75x75
52	AVDD	3747	-1159.2	75x75
53	AGND	3747	-1058.4	75x75
54	NC	3747	-957.6	75x75
55	GPIO1	3747	-856.8	75x75
56	GPIO0	3747	-756.0	75x75
57	TM	3747	-554.4	75x75
58	PWDNB	3747	-453.6	75x75
59	XSHUTDOWN	3747	-352.8	75x75
60	DOGND	3747	-252.0	75x75

table 8-1 pad location coordinates (sheet 3 of 3)

pad number	pad name	x coordinate	y coordinate	bond pad opening size
61	VN1	3747	-151.2	75x75
62	VN2	3747	-50.4	75x75
63	VH2	3747	50.4	75x75
64	VH11	3747	151.2	75x75
65	DOGND	3747	252.0	75x75
66	VSYNC	3747	352.8	75x75
67	HREF	3747	453.6	75x75
68	STROBE	3747	554.4	75x75
69	DOVDD	3747	655.2	75x75
70	FSIN	3747	756.0	75x75
71	NC	3747	856.8	75x75
72	ATEST	3747	957.6	75x75
73	AGND	3747	1058.4	75x75
74	AVDD	3747	1159.2	75x75
75	NC	3747	1260.0	75x75
76	DOGND	3747	1360.8	75x75
77	DVDD	3747	1461.6	75x75
78	DOGND	3747	1663.2	75x75
79	DVDD	3747	1764.0	75x75
80	SID2	3747	2167.2	75x75
81	SID	3747	2268.0	75x75
82	DOGND	3747	2368.8	75x75
83	AVDD	3747	2469.6	75x75
84	AGND	3747	2570.4	75x75

8.2 reconstructed wafer (RW) physical specifications

- maximum total die count: 599
- film frame: Compact Disco Stainless SUS420
- carrier tape: UV tape

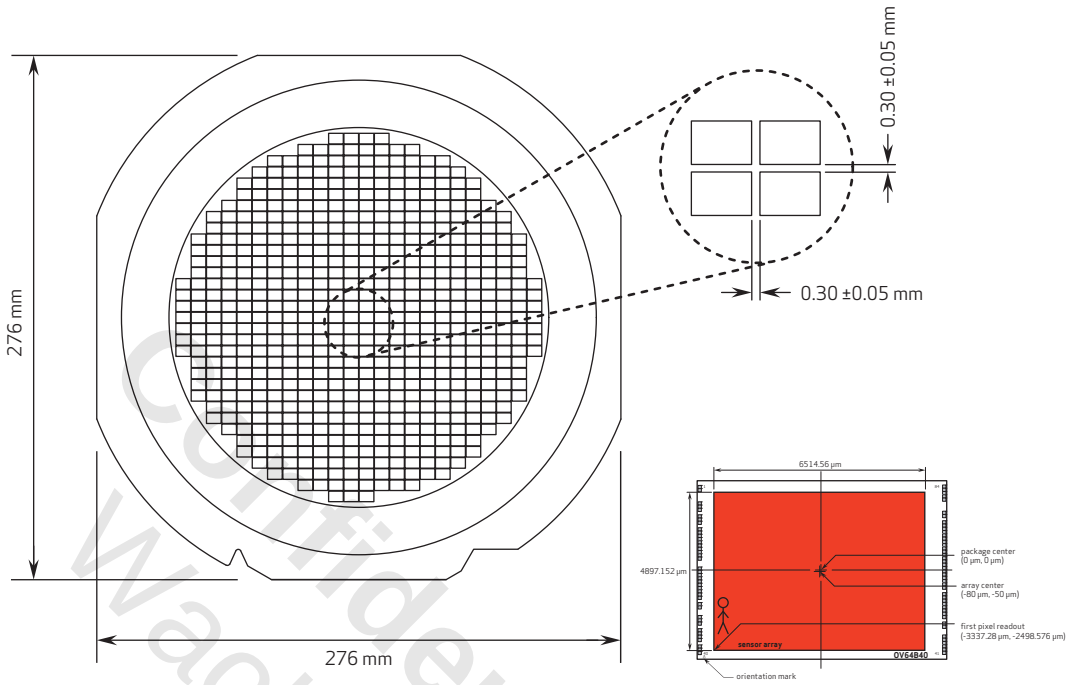
table 8-2 RW physical dimensions

feature	dimensions
RW physical dimensions	8" RW on 12" frame
wafer thickness (OVXXXXX-ABCD)	
C=5	150 µm ± 7 µm (5.9 mil ± 0.3 mil)
reconstructed wafer street width	300 µm ± 50 µm (11.8 mil ± 2 mil)
placement accuracy x, y, theta	± 50 µm (± 2 mil), <1 degree
singulated die size	
width	7739.6 µm ± 20 µm (304.7 mil ± 0.8 mil)
length	5588.6 µm ± 20 µm (220.0 mil ± 0.8 mil)
bond pad size	96 µm × 79 µm (3.8 mil × 3.1 mil)
minimum bond pad pitch	100.8 µm (3.9 mil)
bond pad opening size	75 µm × 75 µm (3.0 mil × 3.0 mil)
optical array	
die center	(0, 0)
optical center from die center[a]	(-80, -50)

a. based on die orientation on frame with notch facing down position

note
Actual die count varies and the absent die may be less than 10% of the maximum total die count (excluding the last frame of the wafer lot).

figure 8-2 OV64B40 RW physical diagram

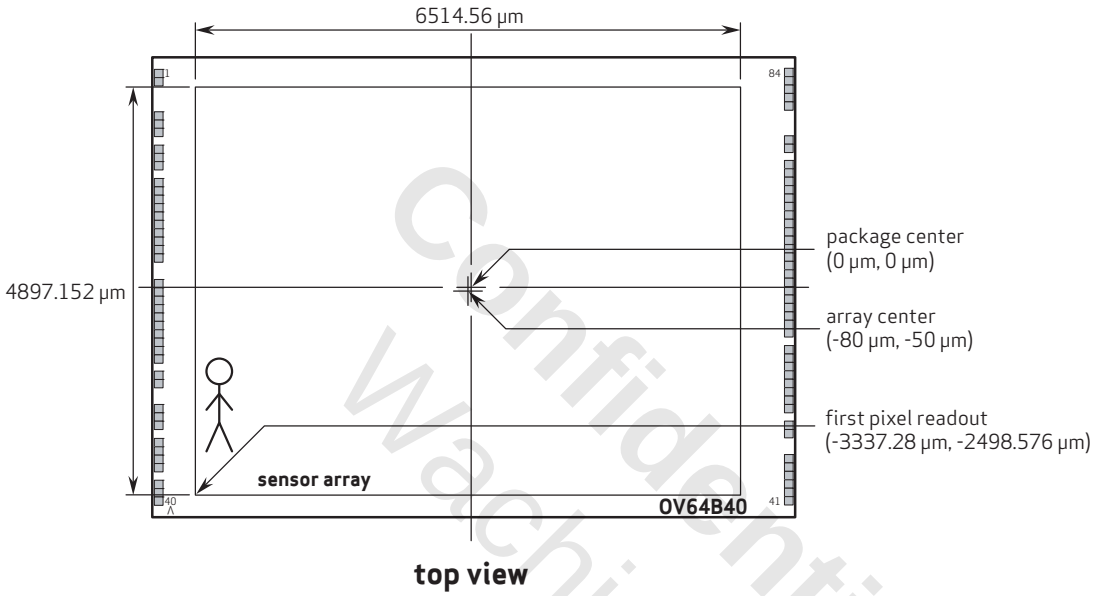


note keep-out-of-contact areas are highlighted in red color for related process fixtures/tools (e.g., nozzle, collets, etc.)

9 optical specifications

9.1 sensor array center

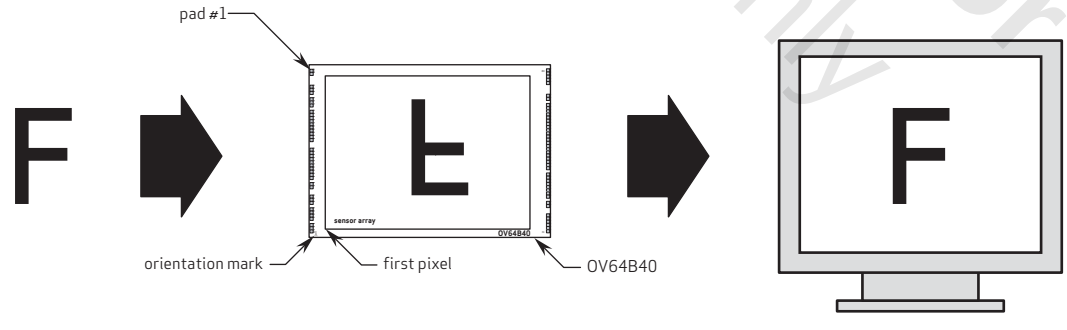
figure 9-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies flip the image, the chip is typically mounted as above with first pixel at bottom-left corner.

figure 9-2 final image output



9.2 lens chief ray angle (CRA)

figure 9-3 chief ray angle (CRA)

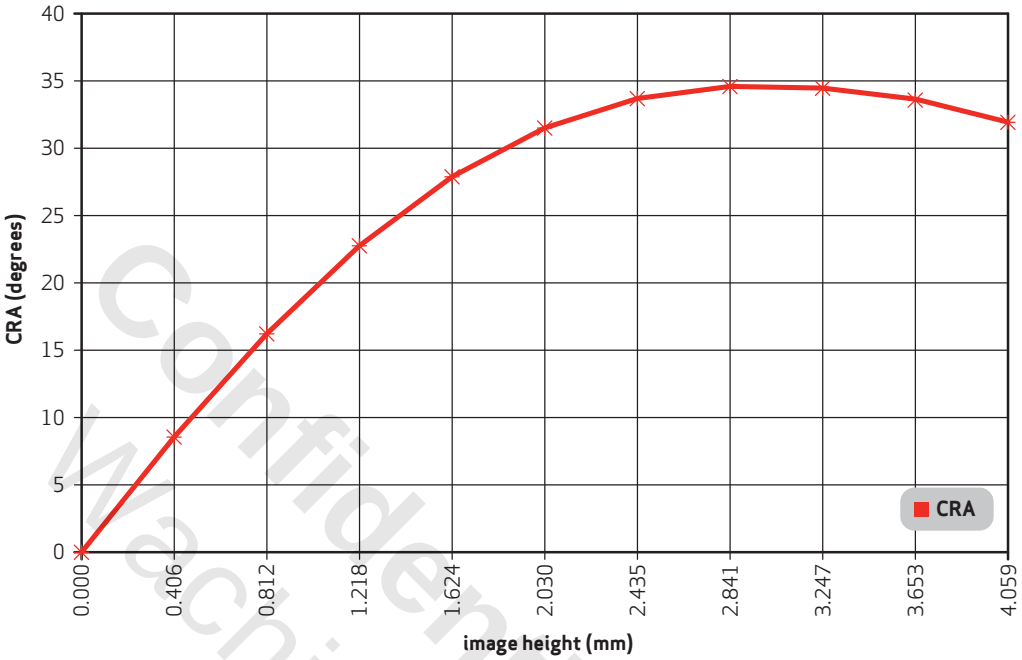


table 9-1 CRA versus image height plot

field (%)	image height (mm)	CRA (degrees)
0	0.000	0.00
0.1	0.406	8.53
0.2	0.812	16.20
0.3	1.218	22.72
0.4	1.624	27.86
0.5	2.030	31.49
0.6	2.435	33.66
0.7	2.841	34.55
0.8	3.247	34.43
0.9	3.653	33.54
1	4.059	31.92

appendix A handling of RW devices

A.1 ESD /EOS prevention

1. Ensure that there is 500V ESD control in all work areas.
2. Use ESD safety shoes, ground strap, and static control smocks in test areas.
3. Use grounded work carts and tables in inspection areas.
4. OmniVision recommends the use of ionized air in all work areas.

A.2 particles and cleanliness of environment

1. All production, inspection and packaging areas should meet Class10 environment requirements.
2. Use optical microscopes with 50X and 100X magnifications for particle inspection.
3. Ensure that there is good cassette sealing for particle protection during storage.
4. OmniVision recommends water cleaning to remove removable particles.
5. RW die should be stored in nitrogen gas purged cabinets with temperature less than 30°C and relative humidity of 60% before assembly.

A.3 other requirements

1. Reliability assurance of RW or COB bare die is certified by product reliability of the bare die in a CLCC, CSP, or QFP package form factor. Precautions should be taken if the packaging form factor of the bare die is other than these specified.
2. Avoid exposure to strong sunlight for extended periods of time as the color filter of the image sensor may become discolored.
3. Avoid direct exposure of the sensor bare die to high temperature and/or humidity environment as sensor characteristics will be affected. Extra precautions should be exercised if the bare die experiences temperatures exceeding 260°C for more than 75 seconds.

revision history

version 1.0 03.17.2020

- initial release

version 1.1 05.19.2020

- in section 2.10, changed first sentence of second paragraph to "In the OV64B40, the SCCB ID is controlled by two SID pins and can be programmable."
- in section 3.6, completely changed figure 3-5
- in table 6-1, changed address range for AWBG_L to "0x50F0~0x5107", changed address range for AWBG_M to "0x53F0~0x5407", and changed address range for AWBG_S to "0x56F0~0x5707
- in table 6-3, changed default values for registers 0x300A, 0x300B, 0x300C to 0x56, 0x64, 0x42, respectively, changed register description title of register 0x3026 to "PSV Mode Clock Gating Disable", changed description of register bits 0x3026[7:5] to "Reserved", changed description of register bit 0x3026[4] to "mask_mipi_clk_gating", changed description of register bit 0x3026[3] to "mask_vfifo_clk_gating", changed description of register bit 0x3026[2] to "mask_pdfifo_clk_gating", changed description of register bit 0x3026[1] to "Reserved", changed description of register bit 0x3026[0] to "mask_psram_clk_gating", changed register description title of register 0x3027 to "PSV Mode Clock Gating Disable", changed description of register bit 0x3027[7] to "mask_testmode_clk_gating", changed description of register bit 0x3027[6] to "mask_ispfc_clk_gating", changed description of register bit 0x3027[5] to "Mask clock gating for sync_fifo, BLC, band_eav", changed description of register bit 0x3027[4] to "Reserved", changed description of register bit 0x3027[3] to "mask_clk_gating_mipi_sclk", changed description of register bit 0x3027[2] to "mask_clk_gating_vfifo_sclk", changed description of register bit 0x3027[1] to "Mask clock gating for ISP, lr_pipe, lr_pd", and changed description of register bit 0x3027[0] to "Mask clock gating for pdfifo_sclk"
- in table 6-4, changed default value for register 0x3107 to 0x86
- in table 6-5, changed default value for registers 0x3220 and 0x3221 to 0x11 and 0x30, respectively
- in table 6-6, changed register name, default value, R/W, and register description title of register 0x3421 to "PSV_CTRL_13_33", "0x15", "RW", and "r_asp_pd[7:0]", changed description of register bit 0x3421[7] to "Control VDAC PD", changed description of register bit 0x3421[6] to "Control VREF PD", changed description of register bit 0x3421[5] to "Control V2I PD", changed description of register bit 0x3421[4] to "Control XDEC PD", changed description of register bit 0x3421[3] to "Control CBAR PD", changed description of register bit 0x3421[2] to "Control VLN PD", changed description of register bit 0x3421[1] to "Control DCPM PD", changed description of register bit 0x3421[0] to "Control SRAM PD", changed register name, default value, R/W, and description of register 0x3423 to "RSVD", "–", "–", and "Reserved", respectively, changed binary value selection 00 description to "Controlled by register", changed binary value selection 01 description to "Power down in vertical blanking", changed binary value selection 10 description to "Power down in pre-change vertical blanking", changed binary value selection 11 description to "Power down in common vertical blanking of pre-change and streaming" for register bits 0x3424[7:6], 0x3424[5:4], 0x3424[3:2], 0x3424[1:0], 0x3425[7:6], 0x3425[5:4], 0x3425[3:2], 0x3425[1:0], 0x3426[5:4], 0x3426[1:0], 0x3427[5:4], and 0x3427[3:2], changed description of register bits 0x3425[7:6] to "asp_pd_sig7_timing_option for DAC", changed description of register bits 0x3425[5:4] to "asp_pd_sig6_timing_option for VREF", changed description of register bits 0x3425[3:2] to "asp_pd_sig5_timing_option for V2I", changed description of register bits 0x3425[1:0] to "asp_pd_sig4_timing_option for XDEC", changed description of register bits 0x3426[7:6] to "Reserved", changed description of register bits 0x3426[5:4] to "asp_pd_sig10_timing_option for

RAMPBUF", changed description of register bits 0x3426[3:2] to "Reserved", changed description of register bits 0x3426[1:0] to "asp_pd_sig8_timing_option for PUMP", changed description of register bits 0x3427[7:6] to "Reserved", changed description of register bits 0x3427[5:4] to "asp_pd_sig14_timing_option for FDC", changed description of register bits 0x3427[3:2] to "asp_pd_sig13_timing_option for PUMP_CLK", changed description of register bits 0x3427[1:0] to "Reserved", and changed register name, default value, R/W, and description of registers 0x3428~0x3429 to "RSVD", "–", "–", and "Reserved", respectively

- in section 6.35, changed title to "AWBG_L [0x50F0 ~ 0x5107]"
- in table 6-35, changed register name, default value, R/W, and description of registers 0x50F8~0x50FF to "RSVD", "–", "–", and "Reserved", respectively, and added rows for registers 0x5100~0x5107
- in table 6-41, changed description of register bit 0x5253[0] to "man_pd_location_en"
- in section 6.44, changed title to "AWBG_M [0x53F0 ~ 0x5407]"
- in table 6-44, changed register name, default value, R/W, and description of registers 0x53F8~0x53FF to "RSVD", "–", "–", and "Reserved", respectively, and added rows for registers 0x5400~0x5407
- in section 6.53, changed title to "AWBG_S [0x56F0 ~ 0x5707]"
- in table 6-53, changed register name, default value, R/W, and description of registers 0x56F8~0x56FF to "RSVD", "–", "–", and "Reserved", respectively, and added rows for registers 0x5700~0x5707
- in table 6-67, changed register name, default value, R/W, and description of register 0x652B to "RSVD", "–", "–", and "Reserved", respectively

version 1.11 06.17.2020

- in figure 2-2, changed trace connection from pad 40 to AGND and changed note 6 to "DVDD is 1.1V (1.05~1.18V)..."
- in figure 2-3, changed trace connection from pad 40 to AGND and changed note 6 to "DVDD is 1.1V (1.05~1.18V)..."
- in table 7-3, changed max value for supply symbol V_{DD-D} to 1.18V

version 1.12 07.09.2020

- in table 6-13, changed description of register bit 0x383F[3] to "SOF from rend enable", changed description of register bit 0x383F[2] to "DPD mode", changed description of register bits 0x384C[7:0] to "...total horizontal...", and changed description of register bits 0x384D[7:0] to "...total horizontal..."
- in table 6-41, added rows for registers 0x5335 and 0x5336

version 2.0 08.19.2020

- changed datasheet from Preliminary Specification to Product Specification
- in ordering information, removed "-Z" from ordering part number
- in key specifications, changed active power requirements specification to 647 mW (64 MP @ 15 fps), changed maximum exposure specification to "VTS - 24 for full resolution, VTS - 12 for downsample mode", changed minimum exposure specification to "8 for full resolution or 4 for

downsample mode", changed sensitivity specification to 1550 e-/Lux-sec (1C), 6200 e-/Lux-sec (4C), changed max S/N ratio specification to 34.64 dB (1C), 39.06 (4C), and changed dynamic range specification to 71.48 dB (1C), 77.13 dB (4C)

- in section 3.5.1, changed third sentence of section description to "Register bits 0x3699[5:0] is the data..."
- in table 3-3, added "Option to swap PD data upper/lower row" to bit description of register 0x3684[6], added "Option to swap PD data left/right pixel" to bit description of register 0x3684[5], added "Option to output low 8 bits PD data" to bit description of register 0x3684[4], added "PD DT mode enable" to bit description of register 0x3684[3], added "PD VC mode enable" to bit description of register 0x3684[2], added "PD data output enable" to bit description of register 0x3684[1], and added "MIPI align enable" to bit description of register 0x3684[0]
- in table 4-7, completely replaced table
- in section 5.1, removed fifth and sixth sentences of third paragraph
- in section 6.16, changed section title to "... [0x3D80 ~ 0x3D98, 0x3DA4, 0x3DAA ~ 0x3DAF]"
- in table 6-16, completely replaced table
- in table 7-3, changed typ and max values for supply symbol I_{DD-A} to 66 mA and 80 mA, respectively, changed typ and max values for supply symbol I_{DD-IO} to 0.03 mA and 1 mA, respectively, changed typ and max values for supply symbol I_{DD-D} to 420 mA and 600 mA, and added new table footnote a to active (operating) current

version 2.1 10.05.2020

- in key specifications, changed "standby" power requirement to "XSHUTDOWN"
- in section 2.1.1, changed last sentence to "Then, verify that register 0x7001 = 0x64, register 0x7002 = 0x0B, register 0x7003 = 0x04, register 0x7004 = 0x22, and register bits 0x700E[7:6] = 2'b00"
- in figure 2-2, corrected pin for DGND of U3 to pin B1 and updated note 10 completely
- in figure 2-3, corrected pin for DGND of U3 to pin B1 and updated note 11 completely
- in section 2.11.2.1, changed second line of example settings to "6C 3208 E2 quick manual launch group 2"
- in section 2.11.2.3, changed last paragraph of section description to "In this example, the sensor will quick launch group 0, stay at group 0 for 4 frames, and then return to group 10."
- in section 2.11.2.5, changed fifth line of example settings to "6C 320C 00 skip group 3" and changed eighth line of example settings to "6C 323C 08 stay 8 frames in group 13"
- in section 2.11.2.7, changed first sentence of section description to "By default, during sleep mode, delay manual launch command..."
- in section 3.1, changed sidebar note to "Maximum exposure = VTS - 24 lines for full resolution (VTS - 12 lines for downsample mode), minimum exposure = 8 rows for full resolution and 4 rows for downsample mode"
- in section 3.2, changed the last three sentences of first paragraph to "One binning type is four adjacent same-color pixels that are summed in array. The other binning type is two adjacent same-color pixels that are summed in array in the vertical direction, then passed to the sensor ISP block to perform sum/average in the horizontal direction."
- in section 3.5.1, changed second sentence of section description to "...0x3684[3] to 1 to enable PD output timing under MIPI data type mode."
- in section 3.5.2, changed fourth sentence of section description to "PDAF data outputs through MIPI virtual channel 1."

- in table 3-3, removed rows for registers 0x480E and 0x4814 and added row for register 0x3699
- in section 4.5, changed second paragraph to "OTP loading data can be triggered when powering up or when writing 0x01 to register 0x3D81. Power up loading data is enabled by register bit 0x3D85[3], which by default is on. Auto mode and manual mode can be chosen by setting register bit 0x3D84[6] to 0 and 1, respectively, and by default, it is in auto mode. In auto mode, all data in the OTP will be loaded to the OTP buffer. While in manual mode, part of the data, which is defined by start address ({0x3D88, 0x3D89}) and end address ({0x3D8A, 0x3D8B})." and changed third paragraph to "...supports two consecutive sections of OTP_DPC clusters programmed in OTP memory. If OTP memory is in that case, the sorting function should be enabled by register bit 0x3D85[7], which by default is off. The first section of the OTP_DPC cluster start address {0x3DAA, 0x3DAB}, second section of the OTP_DPC cluster start address {0x3DAC, 0x3DAD}, and also the OTP_DPC cluster end address {0x3DAE, 0x3DAF} should be configured."
- in figure 5-1, removed RAW DNS block
- in figure 5-2, removed RAW DNS block
- in section 5.5, changed last sentence of second paragraph to "Manual mode configuration is in registers 0x5100~0x5107 for L, 0x5400~0x5407 for M, and 0x5700~0x5707 for S."
- in table 5-1, completely updated gain registers in all rows
- in table 6-30, changed description of register bit 0x480E[3] to "Not used"
- in table 7-1, corrected "V_{DD-O}" supply voltage to "V_{DD-D}"
- in table 7-3, changed parameter for supply symbol $I_{DDS-XSHUTDOWN}$ to "XSHUTDOWN current", changed table footnote a to "power consumption is RMS value measured under typical conditions, at full resolution, full speed...", and changed table footnote b to "XSHUTDOWN current is measured at room temperature"

version 2.11 11.25.2020

- in section 3.6, changed second paragraph to "... 4C ML PD, the full size PD pattern is an area of 16x16,..."

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